Technology Assessment of Si and III-V FinFETs and III-V Tunnel FETs from Soft Error Rate Perspective

Huichu Liu, Matthew Cotter*, Suman Datta, Vijay Narayanan*
Department of Electrical Engineering, *Department of Computer Science Engineering,
The Pennsylvania State University, University Park, PA-16802, USA;
Contact: Email: hxl249@psu.edu, Tel: (814) 753-0026

Abstract

Sea-level soft error performance has been investigated for Si FinFET, III-V FinFET and III-V Heterojunction Tunnel FET in this paper. Transient error generation and transient current profiles in these devices have been evaluated using device simulation. Based on the critical charge extraction for each emerging device-based circuit, the electrical and latching window masking effects have been studied. Below 0.5V, III-V FinFET logic shows reduced soft error rate (SER) compared to Si FinFET. HTFET shows reduced SER for both SRAM and logic compared to Si and III-V FinFET over the evaluated voltage range of 0.3V-0.6V.

Introduction

Radiation induced single-event upsets (SEU) have become a key challenge for cloud computing [1] (Fig. 1(a)) with growing numbers of processors in data centers. Significant increase in soft error rate (SER) with node charge reduction may prevent voltage scaling in future technologies [2] (Fig. 1(b)). With the proposed introduction of low bandgap materials (Ge, III-Vs) as channel replacement for MOSFETs and steep switching Tunnel FETs for low voltage application (Fig. 2(a)), charge generation from sea-level neutron radiation needs to be evaluated due to their low ionization energy [3] (Fig. 2(b)). In this paper, the soft error generation and propagation in Si FinFET, III-V FinFET and III-V Hetero-junction Tunnel FET (HTFET) are systematically investigated using device and circuit simulation. SER performance of these devices for SRAM and logic with voltage scaling is evaluated for ultra-low power application.

Transient Error Generation in Emerging Devices

A heavy ion model [4] is used to perform radiation induced transient current analysis. Linear energy transfer (LET) describes the charge deposition per length along the ion track. A study of fin width scaling (Fig. 3) reveals an effective reduction in sensitive area and collected charge to node charge ratio, which improves the radiation resilience. A fin width of 8nm is used as the baseline in double-gate structure with 20nm channel length for Si FinFET, InAs FinFET and GaSb-InAs HTFET. DC characteristics (Fig. 4) have been calibrated with experimental data (MOSFETs) [5] and atomistic NEGF simulation (HTFET) [6]. Significant reduction in bipolar gain is observed in HTFET compared to MOSFET. In nMOSFET, the generated holes are stored in the body (Fig. 5-6) due to the source barrier, which increases the channel potential. Additional electrons flow into channel and further increase the drain node charge collection (bipolar gain [7]) (Fig. 7). Because of the asymmetric S/D doping in HTFET, both electrons and holes can be collected through the ambipolar transport, which greatly reduces the body charge storage induced bipolar gain and further reduces the collected charge and the transient time. The transient current profile comparison is shown in Fig. 8. At LET=0.1pC/μm, HTFET shows 80% reduction in transient duration and 90% reduction in collected charge compared to Si FinFET. III-V FinFET shows higher collected charge at 1ns after strike due to high channel carrier mobility.

SER Evaluation Methodology

The sea-level neutron induced charge deposition in InAs and Si is obtained from Monte Carlo simulation (Geant4 [8]) using the neutron spectrum [9]. A lookup table based Verilog-A model and transient current library generated from Sentaurus [4] are used to perform Spectre [10] circuit analysis for SRAM cell bit-flip study, as well as for combinational logic electrical and latching window masking effect study [11] (Fig. 9(a)). A technology-adaptable empirical model, [12] validated on previous CMOS technology nodes, is applied in SER calculation for each emerging device-based circuit (Fig. 9(b)).

SRAM Critical LET Extraction

SRAM cell schematic is shown in Fig. 10 with the neutron strike at the bit node. The bit-flip comparison is shown in Fig. 11 for Si, III-V FinFET and HTFET 10T SRAM cells. (10T HTFET cell can achieve desirable noise margin [6].) Extracted critical LET for 6T (except HTFET) and iso-area 10T SRAM cell is plotted with voltage scaling (Fig. 11(d)). Above 0.5V, Si FinFET cell shows higher critical LET compared to III-V FinFET due to lower charge collection. Below 0.5V, however, the critical LET for Si FinFET cell decreases due to the low drive current near the threshold, where III-V FinFET shows the cross-over. HTFET shows 4.5x (V_{DD}=0.5V) and 7x (V_{DD}=0.3V) improvement in critical LET, and 50% recovery time reduction compared to Si FinFET. Besides the short transient duration and the reduced charge collection, the enhanced on-state Miller capacitance effect [13] in HTFET assists the node recovery process (Fig. 12), similar to the metal-insulator-metal (MIM) coupling capacitance employed for traditional backend SRAM hardening [14].

Combinational Logic Critical LET Extraction

The electrical masking of error propagation is evaluated using FO1 inverter chain (Fig. 13(a)). The critical LET causing

propagated voltage pulse (V_{pulse}) exceeding $0.5V_{DD}$ is extracted at the strike node and the 4th stage of the FO1 inverter chain (Fig. 13(b)). The increase in critical LET between the strike node and the 4th stage shows the masking efficiency. HTFET has superior masking effect due to the reduced transient duration (reduced bipolar gain effect) and enhanced Miller capacitance. Error occurs in the state element when the V_{pulse} width, *d*, exceeds the latch window, *w*, (Fig. 14), which determines the latching window critical LET. The probability of latching an error is proportional to the ratio, *w/c*, of the latch window, *w*, to the clock cycle, *c*. *d* is extracted after the V_{pulse} propagated through 4 stages of the inverter chain (Fig. 15). NAND based D flip-flop (DFF) is used in *w* extraction, which shows HTFET DFF can outperform Si and III-V FinFET DFF below 0.6V and 0.4V, respectively (Fig. 16). With 4 stages of electrical masking, the latching window critical LET is extracted. HTFET shows 8x improvement at 0.3V compared to Si FinFET. III-V FinFET outperforms Si FinFET below 0.5V due to high drive current.

SER Evaluation

Based on 10000 events per neutron energy simulation, 2x enhancement of charge deposition is observed in InAs vs. Si (Fig. 17). SER for SRAM cell and logic are shown in Fig. 18(a) and Fig. 18(b), respectively. HTFET shows superior soft error resilience for all voltages studied for both SRAM and logic. III-V FinFET SRAM shows overall high SER due to charge deposition enhancement, but with a shallower slope with voltage scaling than Si FinFET. III-V FinFET logic shows lower SER below 0.5V compared to Si FinFET due to the reduction in the error latching probability.

Conclusion

Sea-level radiation-induced soft errors have been evaluated for Si FinFET, III-V (InAs) FinFET and III-V (GaSb Source/InAs Channel-Drain) HTFET for SRAM and logic. *Si vs. III-V FinFET:* III-V FinFET shows increased charge deposition due to low ionization energy, which increases the SER for SRAM cell for all V_{DD} compared to Si FinFET. For logic, III-V FinFET shows reduced SER compared to Si FinFET below 0.5V due to improved latching window masking. *Si FinFET vs. III-V HTFET:* HTFET shows superior radiation resilience compared to both Si and III-V FinFET over the voltage range of 0.3V-0.6V for both SRAM and logic. This fundamental advantage stems from bipolar gain reduction, on-state enhanced Miller capacitance effect, and improved latching window masking, which makes HTFET desirable for radiation-resilient ultra-low power application.

Acknowledgement

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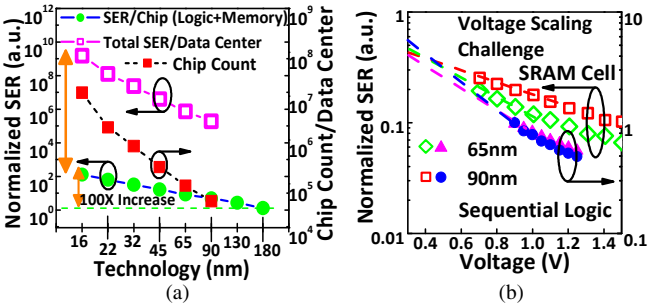
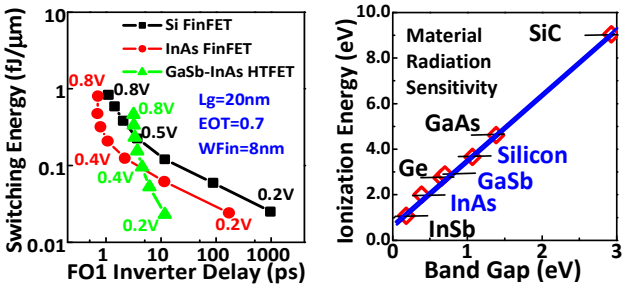
Motivation



(a) (b)

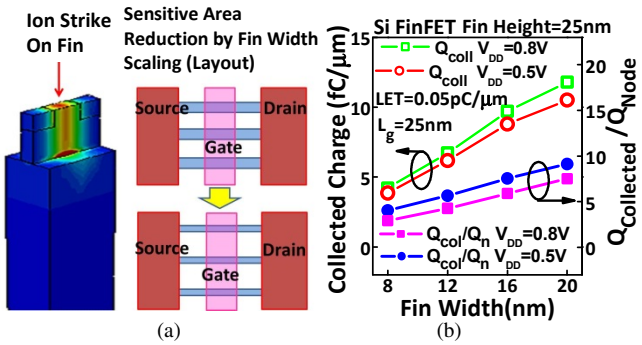
Fig. 1 (a) SER per chip [1] and total SER trend per data center with technology scaling and chip count increase. (b) SER of SRAM cell and sequential logic with voltage scaling for 65nm and 90nm technology [2].



(a) (b)

Fig. 2 (a) Switching energy vs. delay performance for Si FinFET, III-V FinFET and HTFET. HTFET shows superior energy efficiency below 0.4V. (b) Radiation ionization energy with band gap for different materials [3]. InAs is more subjective to radiation.

Transient Error Generation in Emerging Devices



(a) (b)

Fig. 3 (a) Ion strike on the middle of the fin and sensitive area reduction with fin width scaling. (b) Collected charge (Q_{coll}) and collected charge vs. node charge ratio (Q_{col}/Q_n) reduction with fin width scaling at V_{DD}=0.8V and 0.5V due to bulk collection reduction. Ion strike (LET=0.05 pC/μm) at Si FinFET with L_g=25nm and fin height of 25nm.

Table I Device (n-type) Parameters

Gate Length (L_g)	20 nm
EOT (HfO_2)	0.7
Fin Width (t_{Body})	8 nm
InAs FinFET S/D Doping	$4\times10^{19}cm^{-3}$
Si FinFET S/D Doping	1×10^{20} cm^{-3}
HTFET S (GaSb) Doping	4×10^{19} cm^{-3}
HTFET D (InAs) Doping	2×10^{17} cm^{-3}
HTFET: $E_{g,GaSb}$=0.804eV, $E_{g,InAs}$=0.44eV, ΔE_c=0.796eV	

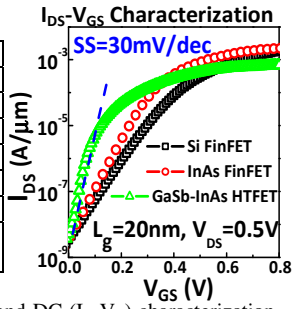


Fig. 4 Simulation parameters (Table I) and DC (I_{ds}-V_{gs}) characterization of Si FinFET, InAs FinFET and GaSb-InAs HTFET at V_{DS}=0.5V. Average subthreshold slope (SS) of 30mV/dec over 2 orders of I_{DS} change is achieved in HTFET.

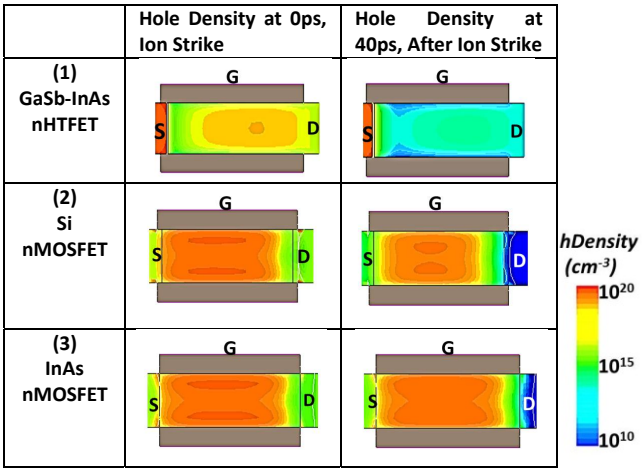


Fig. 5 Time evolution of hole density in n-type device channel region. Hole density decreases fast in (1) nHTFET due to ambipolar transport. Hole storage due to radiation induced charge deposition is observed in (2) Si and (3) InAs nMOSFETs, which induces the bipolar gain effect.

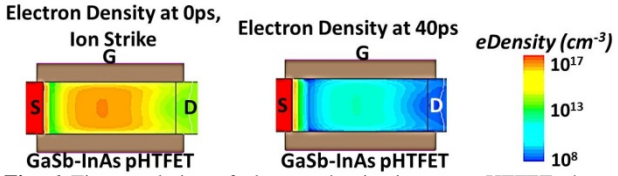


Fig. 6 Time evolution of electron density in p-type HTFET channel region. Similarly, electron density decreases fast in pHTFET.

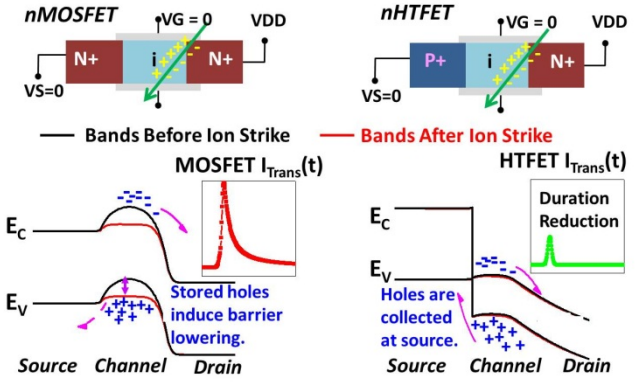
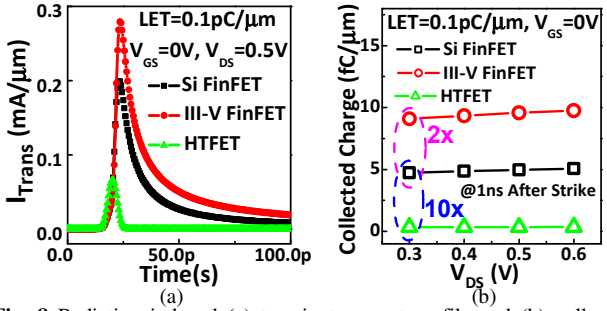
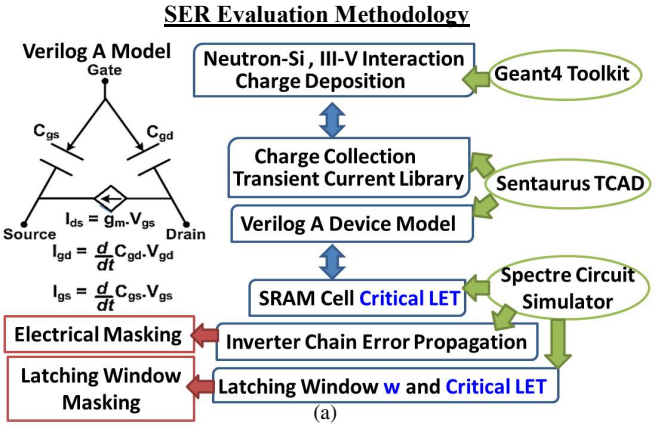


Fig. 7 Band diagram of nMOSFET and nHTFET before/after ion strike. Hole storage induces barrier lowering and additional charge collection (bipolar gain) in nMOSFET. For nHTFET, holes and electrons can be collected at the source and drain respectively, which reduces the bipolar gain effect and transient current (I_{Trans}) magnitude and transient duration.



(a) (b)

Fig. 8 Radiation induced (a) transient current profile and (b) collected charge at 1ns (LET=0.1pC/μm) for each emerging device. HTFET shows reduced current magnitude and 10x charge collection reduction compared to Si FinFET with voltage scaling due to bipolar gain reduction. 2x charge collection enhancement is observed in III-V FinFET compared to Si FinFET due to high carrier mobility.



(a)

Technology Adaptable Empirical Model [12]

$$SER_{SRAM}(LET_{critical}) \sim A * < Flux > * exp\left(-\frac{Q_{critical}}{< Q_s >}\right) \sim exp\left(-\frac{LET_{critical}}{< LET_s >}\right)$$

$$SER_{Logic}(LET_{critical}) \sim w/c * SER_{SRAM}(LET_{critical})$$

$$Q_{critical} = t_{Body} * LET_{critical} \quad [5]$$

<Flux>: average neutron flux. A: sensitive area. $Q_{critical}$: critical charge, converted to critical LET. <Q_s>: charge collection coefficient (neutron induced charge deposition), converted to <LET_s> for Si and III-V. w/c: latch window w to clock cycle c ratio. (<LET_s> = 50fC/μm for Si at sea-level [15]. <LET_s> for InAs is obtained from Geant4.)

(b)

Fig. 9 (a) SER evaluation methodology. (b) Technology adaptable empirical model for critical charge based SER evaluation.

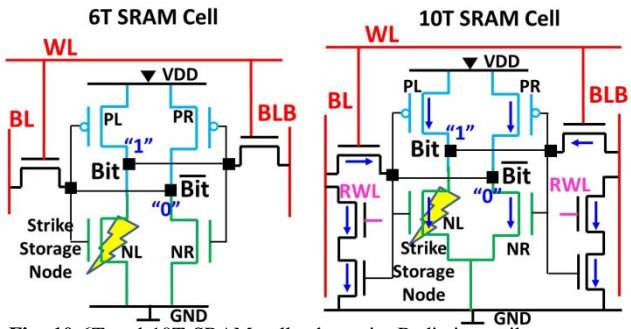


Fig. 10 6T and 10T SRAM cell schematic. Radiation strike on storage node induced charge exceeding node charge can cause an error (bit-flip). HTFET unidirectional current flow is illustrated in 10T cell.

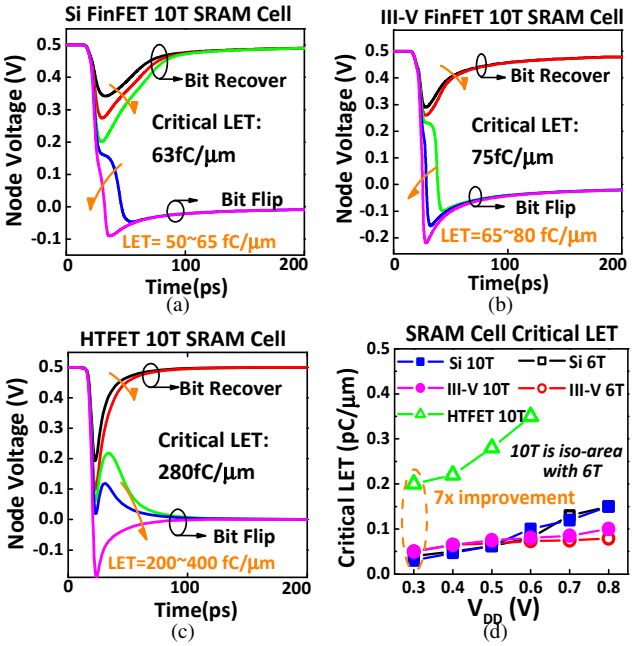


Fig. 11 10T SRAM cell critical LET extraction (node bit-flip) for (a) Si FinFET, (b) III-V FinFET and (c) HTFET at V_{DD}=0.5V. HTFET shows high critical LET and short recovery time. (d) Critical LET for 6T and iso-area 10T SRAM cell with voltage scaling. HTFET shows 7x critical LET improvement compared to Si FinFET at 0.3V. III-V shows cross-over below 0.5V compared to Si FinFET due to high drive current.

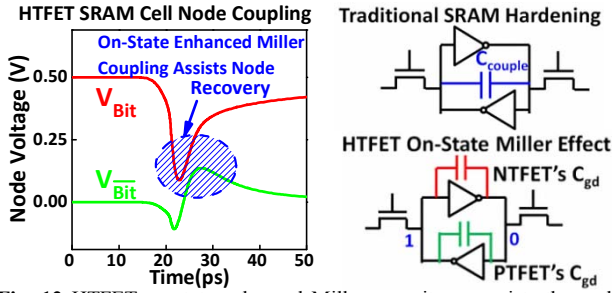


Fig. 12 HTFET on-state enhanced Miller capacitance assists the node recovery with *bit* and $\overline{bit}$ node coupling. Traditional SRAM is hardened by adding coupling capacitance between *bit* and $\overline{bit}$ node, which is comparable to HTFET enhanced on-state Miller capacitance (C_{gd}).

Combinational Logic Critical LET Extraction

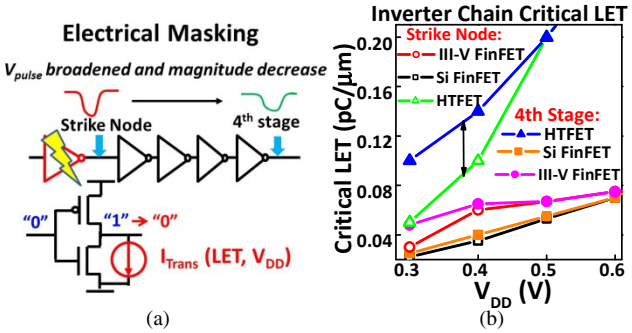
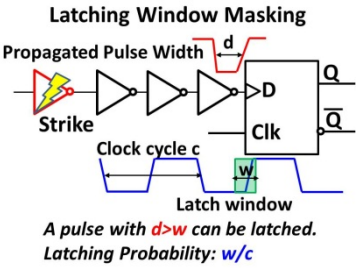


Fig. 13 (a) FO1 inverter chain electrical masking schematic. The propagated V_{pulse} magnitude decreases and its width is widened. (b) Inverter chain critical LET (causing V_{pulse}>0.5V_{DD}) with voltage scaling at the strike node and the 4th inverter stage. HTFET shows improved electrical masking compared to Si and III-V FinFET at reduced V_{DD}.

Fig. 14 (Right) DFF latching window masking schematic. Voltage pulse is propagated to the DFF input port D. The pulse width *d* exceeding latch window *w* can be latched with the probability of *w/c*.



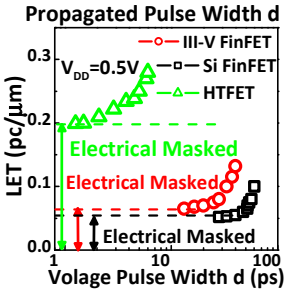


Fig. 15 (Left) Voltage pulse width *d* characterization at 0.5V for each emerging device. HTFET shows reduced pulse width at the same radiation strength (LET) and higher threshold LET which can be electrical masked.

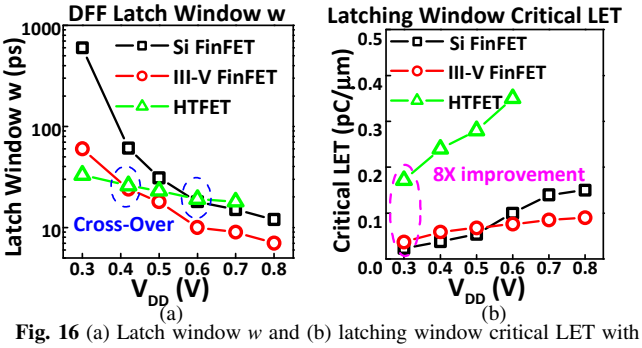


Fig. 16 (a) Latch window *w* and (b) latching window critical LET with voltage scaling for each emerging device. Latching window critical LET is extracted at *w=d* using Fig. 15. HTFET shows 8x critical LET improvement compared to Si FinFET at 0.3V. III-V FinFET shows cross-over at 0.5V due to reduced *w/c* (reduced latch window *w* at low voltage).

SER Evaluation

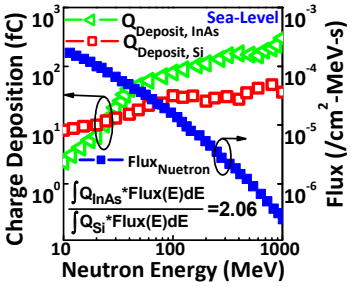


Fig. 17 (Left) Monte Carlo simulation of neutron induced charge deposition on Si and InAs and the neutron flux [9] vs. neutron energy. With the sea-level neutron spectrum integration, 2x charge deposition enhancement is observed in InAs due to the lower ionization energy compared to Si.

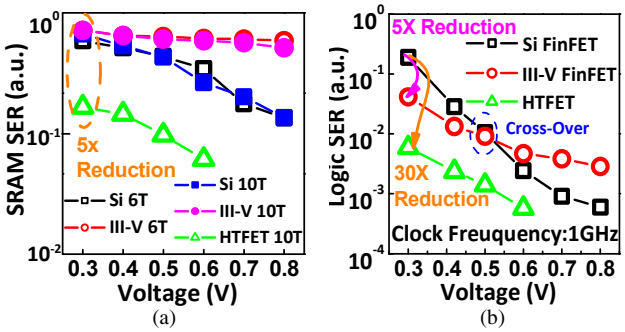


Fig. 18 Relative SER for (a) SRAM and (b) Logic with voltage scaling. HTFET has superior soft error resilience for both SRAM and logic. III-V FinFET logic shows lower SER below 0.5V over Si FinFET.