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Structural, morphological, and defect properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type tunnel field effect transistor structure grown by molecular beam epitaxy

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Structural properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type tunnel field effect transistor (TFET) structure grown by molecular beam epitaxy were comprehensively investigated. High resolution x-ray diffraction revealed symmetric strain relaxation and pseudomorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers with respect to the $In_{0.7}Al_{0.3}As$ buffer, indicating a low dislocation density within the active region. The surface morphology of this structure exhibited a typical two-dimensional cross-hatch pattern with a low root-mean-square roughness of 2.58 nm. Cross-sectional transmission electron microscopy demonstrated a low threading dislocation density within the active region, suggesting high crystalline quality of this p-type TFET structure. Dynamic secondary ion mass spectrometry exhibited an abrupt doping profile over the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ source/channel junction as well as minimal level of intermixing between As and Sb atoms. Thus, these structural properties showed high quality of this structure and provided critical guidance for the fabrication of As/Sb based staggered gap complementary TFETs for ultra-low standby power and energy efficient logic applications.
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I. INTRODUCTION

Power dissipation is a critical bottleneck for further scaling of metal-oxide-semiconductor field-effect-transistors (MOSFETs) to nanoscale. Reducing the supply voltage of transistors is one of the most promising approaches to lower power dissipation while preserving high device performances.[1] However, the limitation of MOSFETs to a minimum subthreshold slope (SS) of 60 mV/dec at room temperature (RT) becomes a major obstacle to further reduce the supply voltage while maintaining high ON/OFF-ratio.[1,2] Tunnel field-effect-transistors (TFETs)[1–11] would exhibit steep (<60 mV/dec at RT) subthreshold characteristics due to the tunneling injection of carriers from source to channel, rather than by thermionic emission. Recently, with the demonstration of sub-60 mV/dec SS (Ref. 3) and MOSFET-like ON-current at RT,[4,5] III-V TFETs have attracted significant interest as low supply voltage transistors for future low power logic applications.[6–11] Among all III-V materials,[3–16] type-II staggered gap $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures have been demonstrated to simplify the design approach and tailor the device performance for applications over a wide range via material composition modulation.[4–16] In recent years, great efforts have been devoted to investigate and upgrade the structural properties and device performances of n-type $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered gap TFETs.[4–14] It is equally important to study high-quality p-type TFET structures within the same material system to achieve complementary energy efficient logic circuits.[16,17] In this work, a comprehensive study was carried out on the structural properties of a metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type staggered gap TFET structure grown by molecular beam epitaxy (MBE). The experimental results demonstrated high material quality of this TFET structure.

II. EXPERIMENT

The $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type staggered gap TFET structure was grown by solid source MBE on semi-insulating (100) InP substrate and the schematic layer structure is shown in Fig. 1. The source (S), channel (C) and drain (D) regions are labeled in this figure and the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface is denoted in a box. As shown in Fig. 1, there is 1.2% lattice mismatch between active layers ($In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$) and the InP substrate. To accommodate this lattice mismatch, 1 μm linearly graded $In_xAl_{1-x}As$ buffer layer was grown with indium (In) composition increasing from 52% to 70% and aluminum (Al) composition decreasing from 48% to 30% so that the top of the buffer layer (100 nm $In_{0.7}Al_{0.3}As$) is internally lattice matched to the $GaAs_{0.35}Sb_{0.65}$ channel/drain layers. The active region of this p-type TFET structure consists of 200 nm n^+ $In_{0.7}Ga_{0.3}As$ source layer with silicon (Si) doping of $8 \times 10^{18}/cm^3$, 150 nm intrinsic $GaAs_{0.35}Sb_{0.65}$ channel layer and 300 nm p^+ $GaAs_{0.35}Sb_{0.65}$ drain layer with carbon (C) doping of $1 \times 10^{19}/cm^3$. The linearly graded $In_xAl_{1-x}As$ buffer, the $GaAs_{0.35}Sb_{0.65}$ channel and drain layers and the

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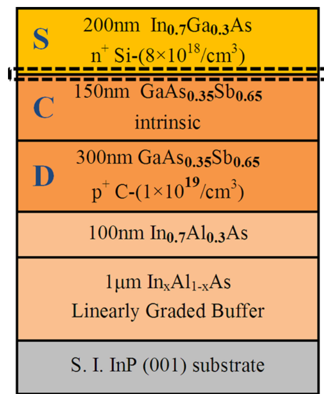

FIG. 1. (Color online) Schematic diagram of the metamorphic $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ p-type TFET layer structure. The source (S), channel (C), and drain (D) regions are labeled in this figure and the $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ heterointerface is denoted in a box.

$In_{0.7}Ga_{0.3}As$ source layer were grown with an optical pyrometer temperature of 500 °C. The active region of this p-type TFET structure was grown with a uniform growth rate of 2.5 Å/s. The n^+ $In_{0.7}Ga_{0.3}As$ source and the gated intrinsic $GaAs_{0.35}Sb_{0.65}$ channel formed the tunnel junction, which is essential for the operation of p-type TFET. Engineering an abrupt $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ heterointerface is critical for the staggered gap TFET structure. However, the abrupt switching from mixed-anion $GaAs_{0.35}Sb_{0.65}$ to mixed-cation $In_{0.7}Ga_{0.3}As$ is a significant growth challenge due to different surface sticking coefficients of arsenic (As) and antimony (Sb) at the specific growth temperature.[13] Earlier studies[12,13] have demonstrated that two surface terminations, i.e., (a) GaAs-like and (b) InAs-like can be formed from Sb rich $GaAs_{0.35}Sb_{0.65}$ to As rich $In_{0.7}Ga_{0.3}As$. Besides, the $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ TFET structure with InAs-like heterointerface shows much more superior material quality and device performances compared with the GaAs-like interface structure in an n-type TFET.[12] As a result, the same switching sequence and interface engineering method[12] as the n-type TFET structure with InAs-like interface was used during the growth of this p-type TFET structure to achieve an InAs-like heterointerface at $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ junction. The staggered source/channel band alignment with a valence band offset (ΔE_V) value of 0.37 eV of this structure was confirmed by x-ray photoelectron spectroscopy.[16] The schematic band alignment of the p-type $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ TFET structure is shown in Fig. 2. The measured valence band offset, calculated conduction band offset and effective tunneling barrier height (E_{beff}) were also labeled in this figure.

The strain relaxation and defect properties of the p-type TFET structure were characterized by high-resolution x-ray diffraction (XRD) and cross-sectional transmission electron microscopy (TEM), respectively. Both XRD rocking curve ($\omega/2\theta$ scan) and reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 as x-ray source. TEM samples were prepared using conventional mechanical thinning procedure followed by Ar^+ ion milling. Contact mode atomic force microscopy (AFM) was used to characterize the surface morphology of the TFET structure. Dynamic secondary ion mass spectrometry (SIMS) using Cameca IMS-7f GEO with Cs^+ as primary ion beam was used to determine the compositional profiles, doping concentration and the atomic intermixing.

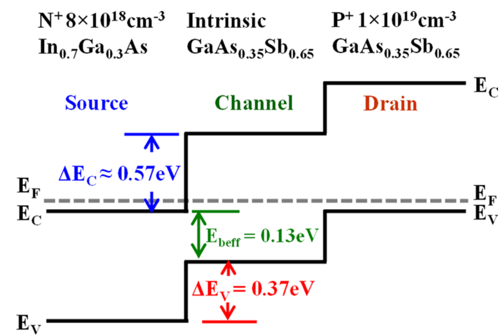

FIG. 2. (Color online) Schematic band diagram of the metamorphic $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ p-type TFET structure. The measured valence band offset, calculated conduction band offset, and effective tunneling barrier height (E_{beff}) were also labeled in this figure.

III. RESULTS AND DISCUSSION

A. Strain relaxation properties

The symmetric (004) XRD rocking curve of this p-channel TFET structure is shown in Fig. 3. Each layer was labeled to its corresponding peak based on wet chemical etching experiments.[12] According to the epilayer structure as shown in Fig. 1, the $In_{0.7}Al_{0.3}As$ buffer layer, the $GaAs_{0.35}Sb_{0.65}$ channel/drain layer and the $In_{0.7}Ga_{0.3}As$ source layer were designed to be internally lattice matched. However, due to the residual strain within the $In_{0.7}Al_{0.3}As$ buffer layer,[18] as well as heavily carbon (C) doping induced lattice contraction[12] in the $GaAs_{0.35}Sb_{0.65}$ layer, these three layers appear as three separate peaks in the XRD rocking curve spectrum as shown in Fig. 3. The distinct XRD peak positions suggest different lattice constants within each epilayer, which indicates different strain relaxation states of the epilayers. The detailed strain relaxation states and residual

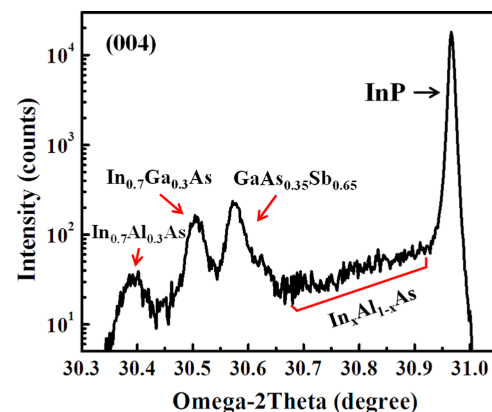

FIG. 3. (Color online) Symmetric (004) x-ray rocking curve of the metamorphic $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ p-type TFET structure. Each layer was labeled to its corresponding peak based on early performed wet chemical etching experiments.

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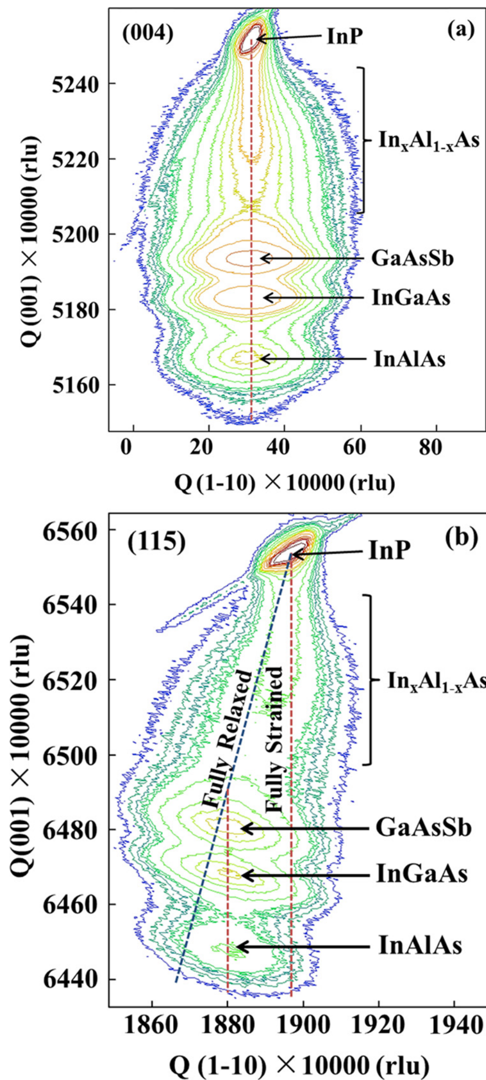

Fig. 4. (Color online) (a) Symmetric (004) and (b) asymmetric (115) RSMs of the p-type TFET structure with the incident x-ray beam along [1$\bar{1}$0] direction. The RSMs together with the extracted lattice parameters confirmed the pseudomorphic nature of the active layers ($In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$) respect to the $In_{0.7}Al_{0.3}As$ buffer, which indicates that low dislocation density should be expected within the active layers.

strain of each epilayer were analyzed from symmetric (004) and asymmetric (115) RSMs. Figures 4(a) and 4(b) show the symmetric (004) and asymmetric (115) RSMs of the p-type TFET structure with incident x-ray beam along [1$\bar{1}$0] direction. Four distinct reciprocal lattice points (RLPs) were found in RSMs of this structure, corresponding to (1) the InP substrate, (2) $GaAs_{0.35}Sb_{0.65}$ channel/drain layer, (3) $In_{0.7}Ga_{0.3}As$ source layer and (4) 100 nm $In_{0.7}Al_{0.3}As$, the uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. From RSMs, the lattice constant in the out-of-plane, *c* (from the symmetric 004 reflection), and the lattice constant in the growth plane, *a* (from the asymmetric 115 reflection), were determined. The relaxed lattice constant a_r and strain relaxation values were also extracted from RSMs. Table I summarized the in-plane and out-of-plane lattice constants, relaxed lattice constants, strain relaxation values, residual strain and alloy composition of each epilayer with the projection of x-ray beam along [1$\bar{1}$0] direction. Using the extracted lattice constant values in Table I, it can be seen that the active layers ($In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$) are pseudomorphic to the $In_{0.7}Al_{0.3}As$ buffer, which indicates that low dislocation density should be expected within the active layers. Besides, the low dislocation density within the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers can be further supported by the relatively short elongation of RLPs of these two layers along Q (1–10) direction as shown in Figs. 4(a) and 4(b). Smaller dislocation density in [110] (or [1$\bar{1}$0]) direction leads to less diffuse scattering of x-ray in its orthogonal [1$\bar{1}$0] (or [110]) direction, resulting in the shorter elongation of RLPs along Q (1–10) [or Q (110)] in RSMs. Furthermore, it can be found from the asymmetric (115) RSM as shown in Fig. 4(b) that, the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers are aligned in a vertical line [fully strained line, red dashed line in Fig. 4(b)] with respect to the $In_{0.7}Al_{0.3}As$ buffer, which additionally confirmed the pseudomorphic nature of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers.[19] Although the in-plane lattice constants of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ are slightly smaller than that of $In_{0.7}Al_{0.3}As$ in this p-type TFET structure, the small difference in lattice constant does not generate strain relaxation of these two layers due to the critical layer thickness consideration, which lead to the pseudomorphic nature and low dislocation density within these two layers.

For metamorphic zinc-blende semiconductor structures, the lattice mismatch between substrate and epilayers can be accommodated by dislocation glide. However, asymmetric strain relaxation will lead to different dislocation densities along two orthogonal ⟨110⟩ directions, which will in turn result in different lattice constants along [110] and [1$\bar{1}$0] directions.[20] As a result, the anisotropy in strain relaxation states of the TFET structure can be determined by aligning

Table I. Summary of strain relaxation properties of the p-channel TEFT structure with incident x-ray beam along [1$\bar{1}$0] and [110] directions.

Incident beam direction	Layers	Lattice constant (Å)			Composition (%)	Relaxation (%)	Tilt (arcsec)	Strain (%)
		c	a	a_r				
1$\bar{1}$0	GaAsSb	5.9347	5.9127	5.9237	Sb: 62	80	−19	0.94
	InGaAs	5.9468	5.9162	5.9314	In: 69	76	−38	1.07
	InAlAs	5.9649	5.9202	5.9426	In: 71	70	−58	1.26
[110]	GaAsSb	5.9343	5.9132	5.9237	Sb: 62	81	56	0.94
	InGaAs	5.9465	5.9146	5.9304	In: 68	74	35	1.05
	InAlAs	5.9648	5.9226	5.9437	In: 71	72	35	1.28

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the projection of the incident x-ray beams along two orthogonal ⟨110⟩ directions. Therefore, x-ray RSMs were recorded once again on this structure with the incident x-ray beam along [110] direction and Figs. 5(a) and 5(b) show the symmetric (004) and asymmetric (115) RSMs from this measurement, respectively. The lattice parameters and strain relaxation values extracted from Figs. 5(a) and 5(b) were also summarized in Table I. One can find from Table I that the strain relaxation values of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the $In_{0.7}Al_{0.3}As$ buffer are almost identical along two orthogonal ⟨110⟩ directions, which indicates symmetric strain relaxation of this structure. The symmetric strain relaxation of these layers suggests that the total length of misfit dislocations in each ⟨110⟩ direction is approximately the same. Besides, the lattice tilt amplitude observed from (004) RSMs was less than 200 *arc sec* from each epilayers in both measurements, indicating nearly equal amount of α and β dislocations participated during the relaxation process. The small lattice tilt also supports the observed symmetric strain relaxation of the lineally graded $In_xAl_{1-x}As$ buffer, $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers. The symmetric strain relaxation properties not only indicate the homogeneity and effectiveness of the graded buffer on the relaxation of mismatch induced strain, but also provide more flexibility for the alignment of channel direction during the device fabrication with side-wall architecture.[3] As a result, the pseudomorphic nature of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the symmetric strain relaxation of the structure provide a "virtually" defect free and isotropic active region for the p-type TFET structure, which is desirable for improving the performance of TFET devices with low OFF-state leakage and high ON/OFF-ratio.

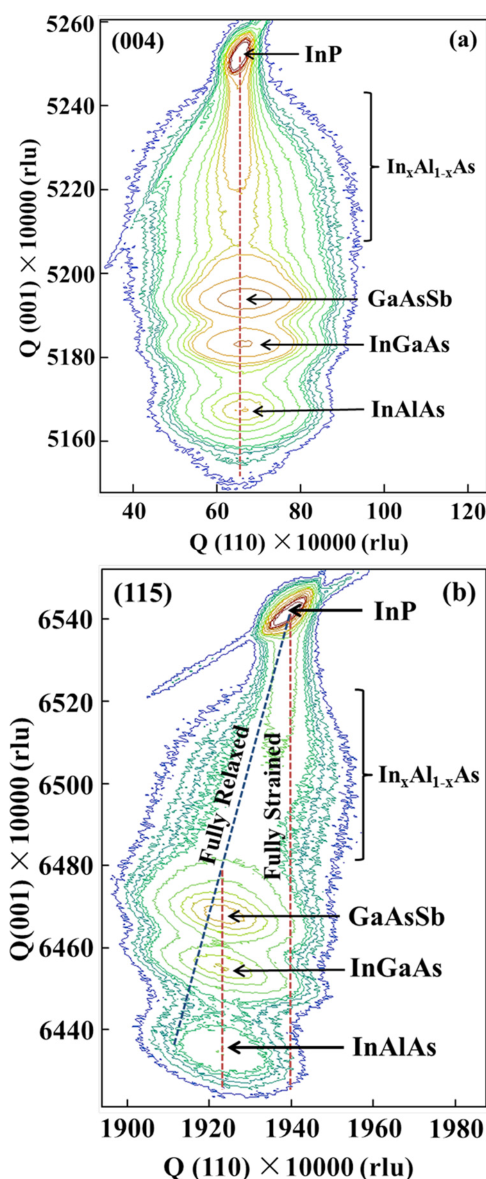

FIG. 5. (Color online) (a) Symmetric (004) and (b) asymmetric (115) RSMs of the p-type TFET structure with the incident x-ray beam along [110] direction. The strain relaxation values of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the $In_{0.7}Al_{0.3}As$ buffer are almost identical along two orthogonal ⟨110⟩ directions, which indicate symmetric strain relaxation of this structure.

B. Surface morphology

Strain within the linearly graded buffer was primarily relaxed by formation of 60° *a*/2 ⟨110⟩ {111} misfit dislocations at epilayer/substrate interface.[20] These dislocations can glide along {111} planes[21] and thread toward the surface at 60° angle within ⟨110⟩ directions,[20,21] which results in a cross-hatch pattern on the sample surface. As a result, characterization of the surface morphology is an important metric for the metamorphic TFET structure as it directly relates to the strain relaxation properties. Figure 6 shows the $10\mu m \times 10\mu m$ AFM micrograph of the TFET structure, which displays the anticipated two-dimensional cross-hatch surface morphology. The two-dimensional cross-hatch pattern is well developed and quite uniform with ridges and grooves parallel to [110] and [$1\bar{1}0$] directions, as labeled in the figure. The line profiles in the two orthogonal ⟨110⟩ directions are also included in this figure. The uniform distribution of the cross-hatch pattern along [110] and [$1\bar{1}0$] directions suggest a symmetric strain relaxation of the linearly graded buffer layer, which is in agreement with the XRD results. Besides, the AFM measurement shows a smooth surface with a root-mean-square (*rms*) roughness of 2.58 nm. The well maintained two-dimensional cross-hatch pattern and low surface *rms* roughness also indicates the low dislocation density of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers; otherwise, the two-dimensional cross-hatch pattern developed by the graded buffer will be sheltered by high density dislocations and a grainy texture with much higher surface roughness will be expected.[12]

C. Dislocation and defects

The crystalline quality of the p-type TFET structure was further characterized by cross-sectional TEM. Figure 7(a) shows the bright field cross-sectional TEM micrograph of the TFET structure. All layers were labeled in this figure and the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface was denoted by an arrow. It can be seen from this figure that the linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates

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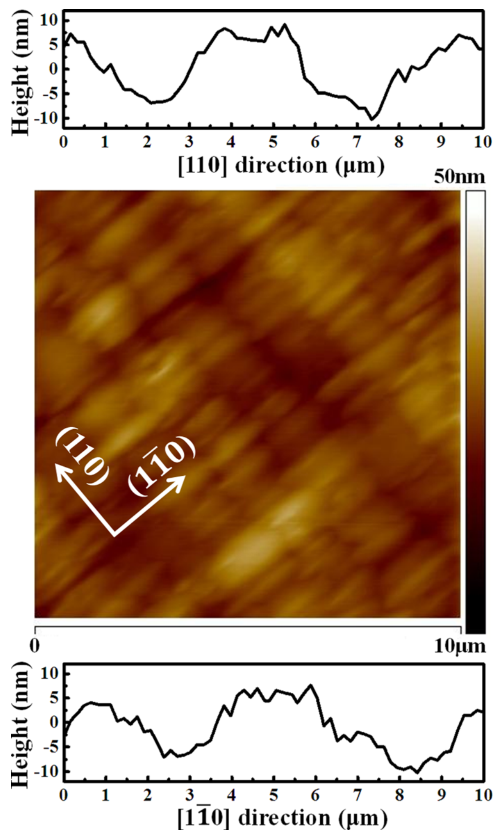

FIG. 6. (Color online) $10\mu m \times 10\mu m$ AFM micrograph of the p-type metamorphic TFET structure. The line profiles in the two orthogonal $\langle 110 \rangle$ directions are also included. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggests a symmetric strain relaxation of the linearly graded buffer layer. The AFM measurement shows a smooth surface morphology of the TFET structure with a root-mean-square (*rms*) roughness of 2.58 nm.

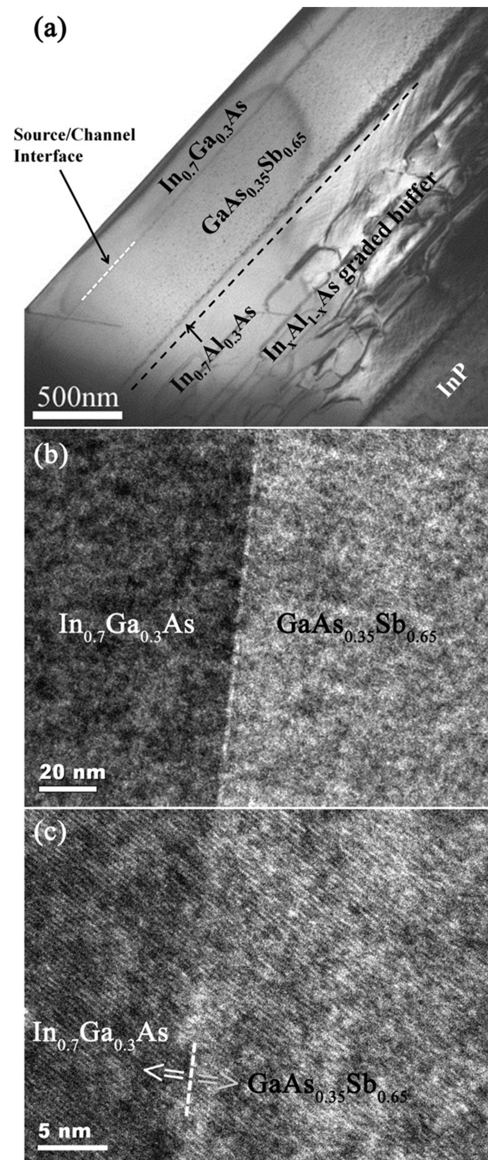

FIG. 7. (a) Cross-sectional TEM micrograph of the p-type metamorphic TFET structure. The linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch between $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the InP substrate. Only one threading dislocation was observed in the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers at this magnification, indicating high crystalline quality of the p-type TFET structure. (b) and (c) cross-sectional TEM micrograph of the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface with high magnification. A sharp heterointerface with high crystalline quality was observed.

the lattice mismatch by the formation of dislocations between $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the InP substrate. Most of the dislocations were confined within the graded $In_xAl_{1-x}As$ buffer and the upper region of the graded buffer with a thickness of ~200 nm has a minimal dislocation density which cannot be detected at this magnification. As the linearly graded buffer relaxed most of lattice mismatch induced strain, the residual strain within the top of the graded buffer layer is small. No further relaxation took place in this region, leaving a strained and dislocation-free region on the top of the graded buffer, providing a high-quality virtual substrate for the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers of the TFET structure. Besides, only one threading dislocation was observed in the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers at this magnification, indicating a threading dislocation density in these layers on the order of $\sim 10^7/cm^2$. Figures 7(b) and 7(c) shows the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface of this p-type TFET structure with high magnification. High contrast at the heterointerface indicates a sharp interface between n^+ $In_{0.7}Ga_{0.3}As$ source and intrinsic $GaAs_{0.35}Sb_{0.65}$ channel, which is benefited to reduce the effective tunneling barrier width and increase in tunneling current of the TFET device.[22] Besides, no dislocations were observed at the heterointerface from the TEM micrographs with high magnification. The low dislocation density within active layers and the heterointerface suggests high crystalline quality of the p-type TFET structure, which is indispensable for high device performance in fabricated TFETs.

D. SIMS profiles

The abruptness of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction as well as the sharpness of Si doping profile is critical to the performance of TFET devices as they directly determine the tunneling barrier width for carrier to transport from source to channel,[22] which directly relates to the ON-

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state current of TFETs. Besides, the intermixing of As and Sb at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ interface will result in uncontrolled layer composition, which will lead to unintended band alignment and may introduce high dislocation density due to compositional mismatch. In order to determine the atomic intermixing of As and Sb as well as the sharpness of Si doping at the source/channel interface, dynamic SIMS measurements were performed to characterize the compositional profiles of As, Sb, and Si in the source and channel regions. Figure 8(a) shows the As, Sb, and Si depth profiles of the p-type TFET structure. The concentration of different elements was not quantified due to the lack of corresponding standards for SIMS measurement. An abrupt $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface was also found in this structure. The transition from As rich $In_{0.7}Ga_{0.3}As$ to Sb rich $GaAs_{0.35}Sb_{0.65}$ is less than 10 nm, within the sputter induced broadening of the ion beam, depicting a minimum intermixing between As and Sb at the heterointerface. Figure 8(b) shows the calibrated Si doping profile of the p-type TFET structure. The fluctuation of Si doping profile in the source region may due to the secondary ion beam signal variability in the sputtering process. The dopant abruptness is less than 2 nm/decade from n^+ $In_{0.7}Ga_{0.3}As$ source to intrinsic $GaAs_{0.35}Sb_{0.65}$ channel, which is less than the critical dopant abruptness (4 nm/decade)[23] of TFET devices to maximize the junction electric fields and thus enable high ON-state current. The well controlled interface transition with minimum As/Sb intermixing assured the anticipated staggered band alignment with desired effective tunneling barrier height; the abrupt dopant change reduced the carrier tunneling distance and maximized the junction electric field, both of which enhanced high ON-state current.

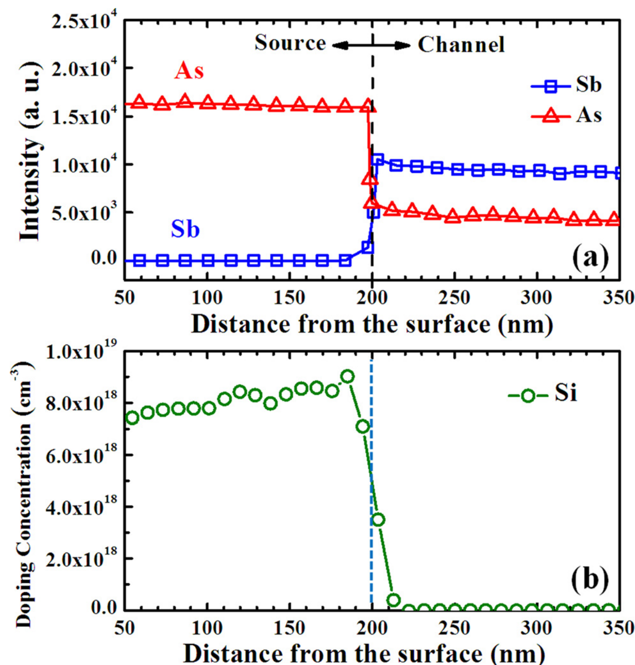

FIG. 8. (Color online) (a) Dynamic SIMS depth profiles of As, Sb from the p-type TFET structure. As abrupt As/Sb change with a transition less than 10 nm was confirmed, indicating low level intermixing between As and Sb at the interface. (b) Si doping profile of the p-type TFET structure. An abrupt Si doping profile with the dopant abruptness less than 2 nm/decade suggests a steep junction formed at the source/channel interface.

E. OFF-state performance and comparison with n-type TFET device structure

Due to the great challenge of MBE growth of mixed As/Sb $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures for p-type staggered gap TFET applications,[12–14] systematically investigation of the structural properties of this heterostructure is essential prior to device fabrication. Studies of growth parameters and optimization of shutter sequences are indispensable for this structure in order to engineer an abrupt change from Sb-rich $GaAs_ySb_{1-y}$ to As-rich $In_xGa_{1-x}As$ layer. Otherwise, improper change of group-V fluxes at the $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterointerface will form a GaAs-like heterointerface, which will in turn produce higher dislocation density at the heterointerface and within the $In_xGa_{1-x}As$ layer.[12,13] These dislocations will introduce fixed charges and change the band alignment from staggered gap to broken gap, resulting in high leakage current of TFET devices.[12] In order to investigate the OFF-state performance of the p-type TFETs, n^+-i-p^+ diodes were fabricated from this structure. As the OFF-state current of p-type TFETs is governed by the leakage current of the reverse-biased n^+-i-p^+ diode,[12,22] current–voltage (I-V) characteristics of the n^+-i-p^+ diode were measured. Figure 9(a) shows the room temperature I-V characteristic of the reverse-biased n^+-i-p^+ diode. The room-temperature I-V characteristic of the reverse-biased p^+-i-n^+ diode fabricated from the n-type $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure with both (b) InAs-like heterointerface and (c) GaAs-like heterointerface

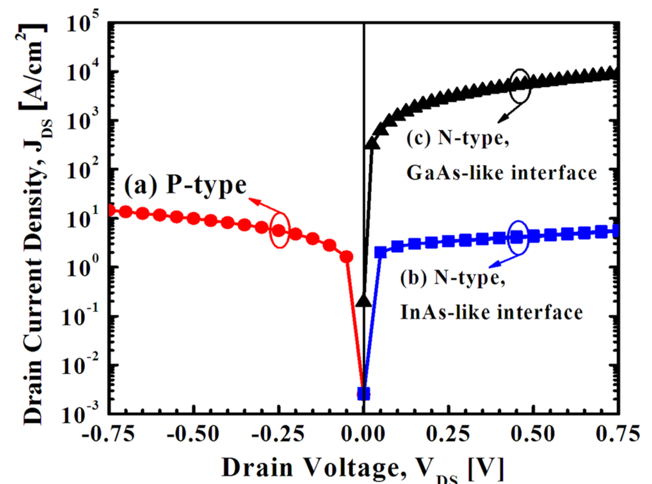

FIG. 9. (Color online) (a) Room-temperature I-V characteristic of the reverse-biased n^+-i-p^+ diode fabricated from the p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFET structure. The room-temperature I-V characteristic of the reverse-biased p^+-i-n^+ diode fabricated from the n-type $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure with both (b) InAs-like heterointerface and (c) GaAs-like heterointerface are also used for comparison. Similar leakage current level of the p-type TFET as that of the N-type TFET with a InAs-like heterointerface indicates that the InAs-like heterointerface with high crystalline quality was formed at source/channel interface of the p-type TFET structure.

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are also used for comparison.[12] Similar leakage current level was observed from the p-type TFET as that from the n-type TFET with an InAs-like heterointerface, indicating that an InAs-like interface with high crystalline quality was formed at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface in the p-type TFET structure. Besides, due to superior material quality, $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFETs with an InAs-like heterointerface exhibits 3 orders of magnitude lower leakage current compared with TFETs with a GaAs-like heterointerface [as shown in Fig. 9(c)]. The relatively low leakage current of the p-type TFET supports our structural analysis presented here.

This study demonstrated preferable strain relaxation properties and high crystalline quality of the p-type TFET structure together with minimum ad-atom intermixing at the heterointerface, all of which are necessary for high performance devices. Earlier studies showed that the type-II staggered band alignment with an effective tunneling barrier height ($E_{beff} = E_G^{InGaAs} - \Delta E_V$) of 0.13 eV was formed at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface.[16] This effective tunneling barrier height plays a significant role in the performance of either n-channel[13] or p-channel TFET devices, which not only determines the ON-state band-to-band tunneling current but also sets the blocking barrier for the OFF-state leakage. It has also been reported that high ON-state current of $135\mu A/\mu m$ with recorded high I_{ON}/I_{OFF} ratio of 2.7×10^4 was achieved in an n-type TFET device using similar $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterostructure.[5,11] OFF-state performance studies also confirmed similar leakage current level of this n-type TFET with the p-type TFET structure using in this study. As a result, promising device performance is expected to be achieved in the structure used in this study for complementary p-type TFET applications.

IV. CONCLUSION

A comprehensive experimental study of the structural properties of a metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type tunnel field effect transistor (TFET) structure grown by molecular beam epitaxy was investigated. The experimental results demonstrated high structural quality of this structure. Symmetric (004) and asymmetric (115) x-ray reciprocal space maps revealed the pseudomorphic nature of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and symmetric strain relaxation along [110] and $[1\bar{1}0]$ directions of the structure. Contact mode atomic force microscopy measurement shows an anticipated two-dimensional cross-hatch surface morphology of this structure with a smooth surface root-mean-square roughness of 2.58 nm. Cross-sectional transmission electron microscopy demonstrated that the linearly graded $In_xAl_{1-x}As$ buffer effectively accommodate the lattice mismatch between $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the InP substrate. The threading dislocation density within the active region is on the order of $\sim 10^7/cm^2$, suggesting high crystalline quality of the p-type TFET structure. Dynamic secondary ion mass spectrometry measurement confirmed a low level intermixing between As and Sb atoms as well as an abrupt doping profile at the source/channel junction. The anticipated staggered band alignment with desired effective tunneling barrier height was well maintained due to the pseudomorphic nature of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ layers as well as the minimum intermixing between As and Sb atoms at the source/channel junction. The superior structural properties and low leakage current density suggest promising device performances of p-type TFETs for high-performance, low standby power, and complementary energy efficient logic application.

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