In Situ Process Control of Trilayer Gate-Stacks on p-Germanium With 0.85-nm EOT

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***Abstract*— *In situ* spectroscopic ellipsometry was utilized in an atomic-layer-deposition (ALD) reactor for rapid and rational gate stack process optimization of the trilayer dielectric $HfO_2/Al_2O_3/GeO_x$ on Ge. The benefit of this approach was demonstrated by developing an entire process *in situ*: 1) native oxide removal by hydrogen plasma; 2) controlled reoxidation for Ge surface passivation; and 3) deposition of Al_2O_3 and HfO_2 using thermal ALD. The low-*k* layer thicknesses were scaled down without losing their respective functions, i.e., GeO_x to form an electrically well behaved interface with Ge and Al_2O_3 to thermodynamically stabilize the GeO_x/Ge interface. Aggressive equivalent-oxide-thickness scaling of the trilayer stack down to 0.85 nm with a low gate leakage of 0.15 mA/cm^2 at V_{FB}–1 V was achieved, while preserving a high-quality dielectric-semiconductor interface.**

***Index Terms*— Ge, MOSCAP, trilayer, *in-situ* spectroscopic ellipsometry, interface, ALD, atomic hydrogen clean.**

I. Introduction

THE development of Germanium (Ge)-channel field effect devices requires the integration of a high permittivity dielectric that forms an electrically well behaved and thermodynamically stable interface with the underlying semiconductor. While a direct high-k/Ge interface showed a high interface state density (D_{it}) [1], GeO_x/Ge has been found promising in reducing D_{it} [2]. However, the equivalent-oxide-thickness (EOT) scaling is limited by the low dielectric constant of GeO_x (k∼6). To scale down EOT, a bilayer gate stack with high-k dielectric on ultrathin GeO_x has been demonstrated, albeit with high gate leakage and a high trap density at the interface [3], attributed to the high-k/GeO_x intermixing caused by the inherent thermodynamic instability of GeO_x/Ge interface [4], [5]. Although the utilization of an ultrathin Si layer to shift the dielectric-semiconductor (D-S) interface from Ge into Si has been successfully demonstrated [6], the introduction of a planar thin Si layer is incompatible with a 3D FinFET manufacturing process flow.

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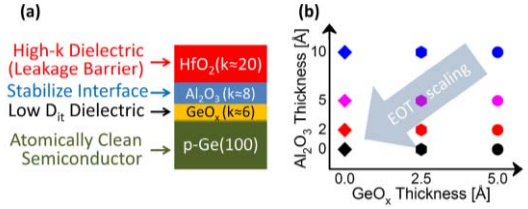

Fig. 1. (a) The design of the trilayer gate stack on p-Ge. (b) Parameter space for EOT scaling of the trilayer gate stacks, with HfO_2 kept constant to ∼24 Å.

The pronounced high-k/GeO_x intermixing can be effectively reduced by introducing an Al_2O_3 diffusion-control-layer (DCL) between HfO_2 and GeO_x [3]. Optimization of such a trilayer gate stack is time consuming and expensive. Immediate feedback during the deposition process and a direct correlation with device performance/characteristics is highly desirable, accelerating the development and rapid prototyping of an entire complex gate dielectric processes.

In this work, we present an *in-situ* controlled process flow to address this challenge for Ge MOSCAPs. Utilizing *in-situ* spectroscopic ellipsometry (SE), a $HfO_2/Al_2O_3/GeO_x$ trilayer gate stack on p-Ge(100) was developed [Fig. 1(a)], including (i) *in-situ* plasma clean to prepare atomically flat and pristine Ge surface, (ii) *in-situ* passivation with GeO_x to form a low D_{it} interface, (iii) Al_2O_3 ALD deposition to stabilize the interface, and (iv) high-k HfO_2 ALD deposition to suppress leakage current. This approach is not limited to Ge but may be also applicable to other semiconductors forming thermodynamically unstable but passivation-friendly interfaces with high-k dielectrics, such as compound semiconductors [7].

II. Experimental Method

The design of $HfO_2/Al_2O_3/GeO_x$/p-Ge gate stacks is shown in Fig. 1(b). The goal to scale down EOT while maintaining a superior D-S interface was tackled by varying the thicknesses of the low-k Al_2O_3 and GeO_x layers without losing their respective functions. The HfO_2 layer thickness was fixed (∼24 Å) to limit the number of experimental variables.

Fig. 2 shows an overview of the p-Ge MOSCAPs process flow using $HfO_2/Al_2O_3/GeO_x$ gate stacks. Details of the optimization of individual process steps will be discussed further below. First, p-Ge(100) substrates (Ga-doped, resistivity = 1.0-5.0 Ω/cm, by Umicore Electro-Optic Materials) were degreased with acetone, isopropyl-alcohol and de-ionized water rinses. The substrates were immediately transferred into the load-lock of ALD system (Kurt J. Lesker Company ALD-150LX). The following process steps in ALD chamber were monitored by *in-situ* SE (M-2000U,

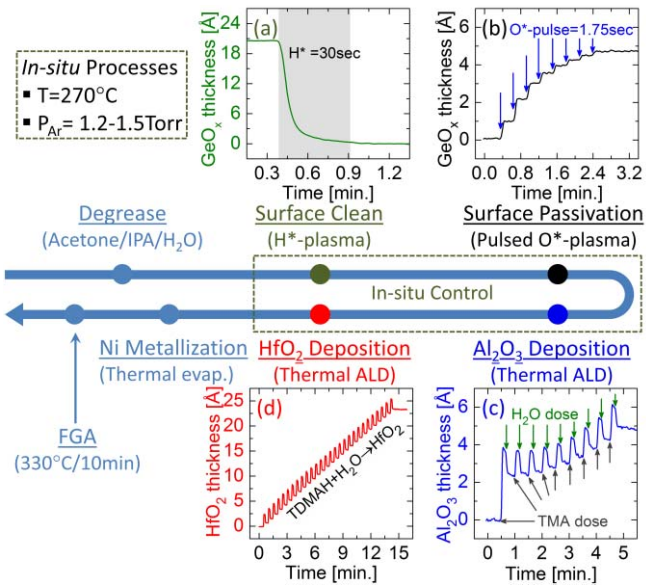

Fig. 2. *In-situ* SE monitoring of the fabrication process: (a) H*-plasma clean of native GeO_x, (b) Ge passivation by pulsed O*-plasma, (c) Al_2O_3 thermal ALD, and (d) HfO_2 thermal ALD, with all oxides described as Cauchy model.

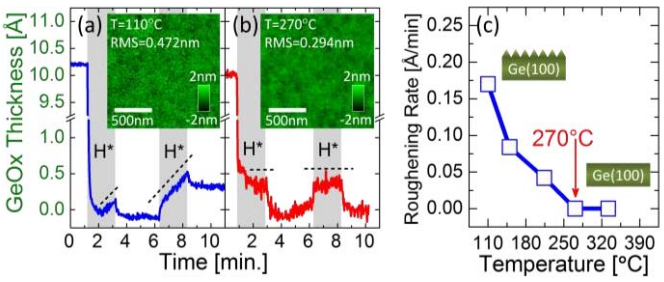

Fig. 3. *In-situ* SE for H*-plasma (shaded region) at (a) 110 °C and (b) 270 °C on Ge; the insets are corresponding *ex-situ* AFM images after H*-plasma. (c) Ge surface roughening rate by H*-plasma, extracted from *in-situ* SE using the nominal "GeO_x" thickness as measure for surface roughness.

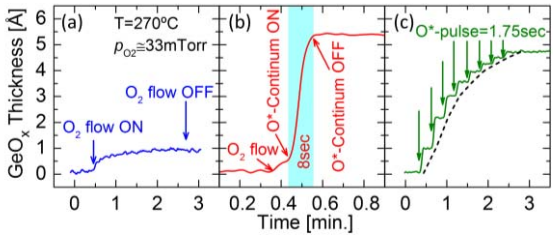

Fig. 4. *In-situ* SE for three GeO_x growth modes at 270 °C: (a) molecular O_2 ($p_{O2} \approx 33$ mTorr/2min), (b) continuous O*-plasma (8 sec), and (c) sequence of O*-plasma pulses (1.75 sec/pulse). Note the shorter time scale in (b).

J. A. Woollam), which monitors the dielectric function of samples, providing real-time information of surface modification like deposition and etching. Figs. 2(a)-(d) show an example of *in-situ* SE monitoring the trilayer gate stack development (270 °C, background p_{Ar} = 1.2-1.5 Torr). The residual native GeO_x was effectively removed by *in-situ* RF atomic hydrogen (H*) plasma (100 W, H_2: Ar = 3: 117 sccm, 30 sec) [Fig. 2(a)]. The GeO_x passivation layer was grown by oxygen (O*) plasma pulses (125 W, 1.75 sec/pulse, O_2:Ar = 3:117 sccm) [Fig. 2(b)]. The Al_2O_3 layer was deposited by thermal ALD with tri-methyl-aluminium (TMA) and H_2O [Fig. 2(c)]. The HfO_2 layer was deposited by thermal ALD using tetrakis-dimethyl-amino-hafnium (TDMAH) and H_2O [Fig. 2(d)]. Each layer thickness in the trilayer gate stacks was precisely controlled by *in-situ* SE. 60nm Ni was thermally evaporated as the gate metal on the samples, which were then annealed in forming gas (FGA, H_2:Ar = 20: 1050 sccm, 330 °C/10 min).

III. Results and Discussion

A. In-Situ Process Optimization

The Ge surface preparation by *in-situ* H*-plasma showed a strong temperature-dependence. At low temperatures [110 °C, Fig. 3(a)], H*-plasma over-exposure resulted in an unexpected increase in "GeO_x" thickness. *Ex-situ* atomic force microscopy (AFM) indicated that the surface was significantly and irreversibly roughened [Fig. 3(a) inset]. The increase in 'GeO_x' thickness was attributed to the optical contribution from increased surface roughness as a consequence of surface disordering [8]. A similar effect was also observed on Si surface [9]. The temperature was too low and pristine Ge surfaces were also etched in H*-plasma. In contrast, extra H* dose at high temperatures maintained a smooth surface [270 °C, Fig. 3(b) inset] (RMS = 0.294nm, as compared to 0.295nm for degreased substrate before H*-plasma), and caused a reversible increase of the nominal "GeO_x" thickness in SE [Fig. 3(b)], attributed to the local surface heating by plasma exposure. The critical temperature to avoid degradation of Ge surface in the H*-plasma was found to be at $T_C \approx 270$ °C, and hence fixed as the optimal temperature throughout the process.

The as-obtained pristine Ge surfaces were then passivated with GeO_x. Three oxidation modes were evaluated: (i) O_2 gas, (ii) continuous O*-plasma, and (iii) O*-plasma pulses, as shown in Fig. 4. Exposing the Ge surface to O_2 resulted in a slow and limited formation of sub-monolayer GeO_x (~1 Å) [Fig. 4(a)], while the continuous O*-plasma [Fig. 4(b)] caused rapid Ge oxide formation (~0.7 Å/sec), not suitable for precise control of the targeted GeO_x thickness. A pulsed O*-plasma mode was used [Fig. 4(c)], allowing a precise adjustment of GeO_x thicknesses up to ~5 Å (≈1 monolayer). The self-limited behaviour was interpreted as a result of the mild oxidation conditions enabled by the short pulses, suggesting that the top-most monolayer of GeO_x acted as an oxygen protection layer.

B. Electrical Characterization of Trilayer Gate Stacks

Equipped with the precise thickness information for each dielectric layer from *in-situ* SE, we investigated their effects on the electrical properties of $HfO_2/Al_2O_3/GeO_x$ MOSCAPs. The role of GeO_x was first investigated using p-Ge MOSCAPs of HfO_2(24 Å)/Al_2O_3(10 Å)/GeO_x stack with various GeO_x thicknesses. The *C-V* characteristics in Fig. 5 show that the sample with ~5 Å GeO_x passivation showed a small frequency dispersion in accumulation ($\Delta C/C_{max}$ = 2.3%), indicating an improved D-S interface

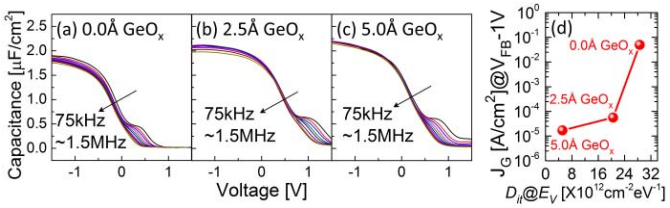

Fig. 5. *C-V* characteristics of HfO_2(24 Å)/Al_2O_3(10 Å)/GeO_x/p-Ge(100) MOSCAPs with varying GeO_x thickness: (a) 0.0, (b) 2.5, and (c) 5.0 Å. (d) The effect of GeO_x thickness on MOSCAP performance. V_{FB} is the flat-band voltage, and E_V is the valence band edge. D_{it} @ E_v were extracted using Castagne-Vapaille method [11].

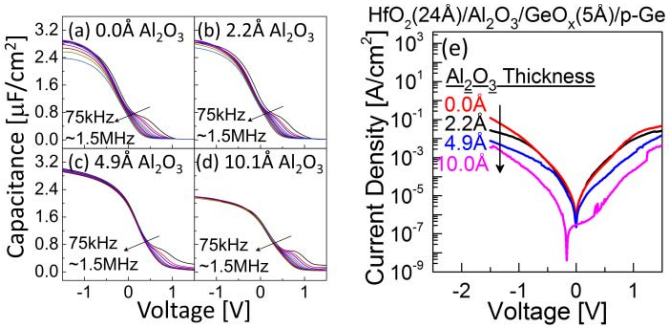

Fig. 6. *C-V* of HfO_2(24 Å)/Al_2O_3/GeO_x(5 Å)/p-Ge MOSCAPs with (a) 0.0, (b) 2.2, (c) 4.9, and (d) 10.1 Å Al_2O_3; (e) the corresponding gate leakages.

quality (D_{it} @ $E_v \approx 5.1 \times 10^{12}$ $cm^{-2}eV^{-1}$), while an insufficient GeO_x passivation (0.0 and 2.5 Å) resulted in not only a larger frequency dispersion at accumulation, but also a higher gate leakage (J_G) [Fig. 5(d)]. Thus, we concluded that a minimum GeO_x thickness of ~5 Å was necessary to create a high-quality interface and to maintain a low gate leakage. The physical mechanism behind this is attributed to that the GeO_x passivation increased the conformity of Al_2O_3 ALD nucleation (AFM results not shown here), and therefore formed a better quality of the dielectric-Ge interface and reduced defects in the dielectrics.

The effectiveness of the Al_2O_3 as DCL was also studied combining *in-situ* SE and electrical characteristics. Figure 6 shows the *C-V* characteristics for HfO_2(24 Å)/Al_2O_3/GeO_x(5 Å) gate stacks with various Al_2O_3 thicknesses. As expected, a direct contact between HfO_2 and GeO_x resulted in an inferior D-S interface [Fig. 6(a)]; the HfO_2/GeO_x intermixing may result in Hf-Ge bond formation [5], contributing to the interface and border trap states [3], [5]. In contrast, a use of ~5 Å Al_2O_3 DCL well preserved the GeO_x/Ge interface quality [Fig. 6(c)], while no further improvement was found for thicker Al_2O_3 [~10 Å, Fig. 6(d)]. Another consequence of introducing Al_2O_3 DCL is the suppression of gate leakage [J_G-V in Fig. 6(a)], attributed to the suppression of HfO_2/GeO_x intermixing and therefore the reduction of electrically active defects in HfO_2 [3], [10]. Fig. 7 compiles the characteristics of various gate stacks on Ge to benchmark the trilayer gate stacks. The Ge p-MOSCAP using the HfO_2(24 Å)/Al_2O_3(5 Å)/GeO_x(5 Å) gate stack showed the optimum performance, with a sub-nm EOT (~0.85 nm) and low gate leakage ($J_G = 0.15$ mA/cm^2 at V_{FB}-1V). We observed that for very thin Al_2O_3 layers, both EOT and J_G decreased; this can be attributed to an

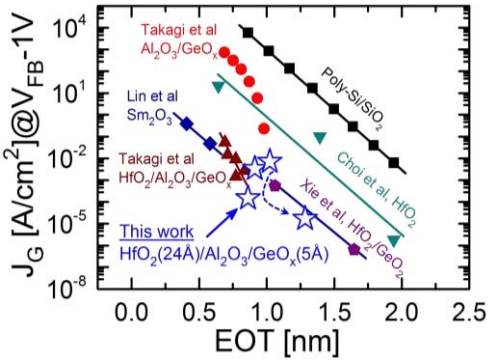

Fig. 7. Gate leakage (J_G@V_{FB}-1V) vs. EOT benchmark of Ge MOSCAPs using HfO_2(24 Å)/Al_2O_3/GeO_x(5 Å) gate stacks with 0.0, 2.2, 4.9, and 10.1 Å Al_2O_3 (indicated by dash arrow). EOT is calculated using C_{max} @ 1.5 MHz.

Al_2O_3/GeO_x intermixing, which maintained a low thickness of the inter-layer between HfO_2 and Ge, but slightly contributed to the increase of its effective permittivity.

IV. Conclusion

A combination of *in-situ* surface process and *in-situ* control by spectroscopic ellipsometry was used for rapid prototyping of high-k gate stacks on the challenging Ge surface. Trilayer gate stacks of HfO_2/Al_2O_3/GeO_x/p-Ge were fabricated and the functionality of individual layer was explored in details. The optimized process resulted in a superior quality of dielectric-Germanium interface, sub-nm EOT (~0.85 nm) and low gate leakage ($J_G = 0.15$ mA/cm^2 at V_{FB}-1V) in p-Ge MOSCAP using the trilayer gate stack of HfO_2(24 Å)/Al_2O_3(5 Å)/GeO_x(5 Å).

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