Investigation of $In_xGa_{1-x}As$ FinFET Architecture with Varying Indium (x) Concentration and Quantum Confinement

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Abstract: $In_xGa_{1-x}As$ FinFETs with varying indium percentage, x, and vertical body thicknesses, are fabricated in a closely packed fin configuration (10 fins per micron of layout area) and their relative performance analyzed and benchmarked. $In_{0.7}Ga_{0.3}As$ quantum well FinFET (QWFF) exhibits peak field effect mobility of 3,000 cm^2/V-sec at a fin width of 38nm with highest performance. Short channel $In_{0.7}Ga_{0.3}As$ QWFF (L_g=120nm) exhibits I_{DSAT} of 1.16mA/μm at V_G-V_T=1V and extrinsic peak g_m=1.9mS/μm at V_{DS}=0.5V and I_{OFF}=30 nA/μm. Components of external resistance (R_{Ext}), side wall D_{IT}, fin profile are analyzed to investigate feasibility of $In_xGa_{1-x}As$ FinFET for beyond 10nm technology node.

Motivation: Higher I_{ON} and g_m with increasing indium percentage (In%) has been demonstrated in planar $In_xGa_{1-x}As$ HEMTs [1]. Yet, it is unclear how much of this benefit is retained in FF structures due to a) additional quantum confinement imposed by fin patterning and b) lack of conduction along the entire height of the fin. Here, we investigate in detail electron transport and electron density per fin in $In_xGa_{1-x}As$ FF structures. We show that, for narrow fins down to 38nm, higher In% QWFF provide higher drive current per fin. The schematic of the three different FF architectures explored are shown in Fig 1. QWFF show enhanced volume inversion (Fig 2a), albeit at the cost of reduced charge per fin compared to bulk FF. Further, increase in the In%, lowers the effective mass (Fig 2b) which aids mobility but impacts density of states. This work explores the fundamental trade-off between enhanced transport and reduced charge per fin for various $In_xGa_{1-x}As$ FF architecture.

Fabrication: $In_xGa_{1-x}As$ FFs are fabricated starting from MBE (Molecular Beam Epitaxy) grown epitaxial layer structures. Gate recess is performed on n++cap layer with citric acid based wet etch selective to InP to define raised source/drain regions. This is followed by chlorine based plasma dry etching to form fins following fin pattern formation using e-beam lithography. ALD deposition of 1nmAl_2O_3/3nmHfO_2 high-k dielectric and evaporation of palladium metal electrode forms a gate stack to wrap around fins. Device fabrication is completed via Ti/Au S/D ohmic contact formation. Fig 3a shows an SEM image of fin array with 100nm pitch, allowing 10 fins in 1μm of layout width. Fig 3b shows the corresponding TEM cross-section confirming the vertical fin etch and the tight fin pitch.

Characterization: The I_DV_G and I_DV_D characteristics for long channel FF devices (L_G=1μm) are shown Fig 4. Output characteristics show that, I_{ON} increases with increasing In% at the same V_G-V_T. The highest I_{ON} is obtained for $In_{0.7}Ga_{0.3}As$ QWFF at W_{Fin}=38nm. Fig 5a shows a representative SEM of the multi-fin split CV structure. Fig 5b shows the extracted carrier concentration using split CV measurements shown in inset. The experimental effective drift mobility extracted from the split CV data is summarized in Fig 6a. The $In_{0.7}Ga_{0.3}As$ QWFF provides the highest peak mobility of around 3,000cm^2/V-sec followed by the $In_{0.53}Ga_{0.47}As$ QWFF at 1,450cm^2/V-sec and $In_{0.53}Ga_{0.47}As$ Bulk FF at 1,000cm^2/V-sec. The measured device characteristics were calibrated to a modified drift-diffusion (DD) model with quantum correction. Fig 4 shows the simulated I_DV_G (symbols) after calibrating the field dependent mobility models to experiment. We extract the mobility via this inverse modeling technique for fabricated devices (Fig 6b). The trends are found to be consistent with the previous experimentally extracted mobility. The discrepancy in mobility values at lower n_s is attributed to a) slight overestimation of mobile charge in split CV technique due to contribution from sidewall D_{IT} b) absence of Coulomb scattering in mobility model used in DD. More importantly, a monotonic roll-off in extracted mobility is observed in both cases at higher n_s due to surface roughness induced scattering. Figs 7a,b show the experimental I_DV_G and I_DV_D characteristics, respectively, for short channel $In_{0.7}Ga_{0.3}As$ QWFFs (L_g=120nm, W_{Fin}=55nm). With layout density of 10 fins per μm width, we achieve I_{DSAT} of 1.16mA/μm at V_G-V_T=1V and extrinsic peak g_m=1.9mS/μm at V_{DS}=0.5V and I_{OFF}=30 nA/μm (SS=236mV/dec DIBL=119mV/V). Further enhancement in I_{DSAT} is obtained by optimizing R_{Ext}. For raised SD architecture in FF, sidewall electrons traverse a longer path to reach the drain in bulk FF than QWFF (Fig.8a). To gain detailed insight into the various components contributing to R_{Ext}, we examine the fin cross-section to extract n++cap/InP barrier interface resistance ($R_{n+/Barrier}$), InP barrier resistance ($R_{Barrier}$), and access resistance (R_{Access}) as shown in Fig 8b. Raised SD favors lower R_{Access} in QWFF (62Ω-μm and 34Ω-μm for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$) as indicated by lower R_{Ext} (Fig 8c).

Benchmarking: Projections for I_{ON} at W_{Fin}=8nm and Lg=10nm (V_{DD}=0.5V), using calibrated mobility models (long channel [present work], short channel [2] and influence of fin width [3]), are shown in Fig 9. The $In_{0.7}Ga_{0.3}As$ QWFF gives 1.5x and 1.3x higher I_{ON} over Si FF [4] and $In_{0.53}Ga_{0.47}As$ Bulk FF, respectively, at 0.5V V_{DD} and matched I_{OFF}=10 nA/μm. The inset in Fig 9 plots the injection velocity of $In_{0.7}Ga_{0.3}As$ QWFF (3.3× Si FF). Fig 10 summarizes the effect of increasing D_{IT} on the sub-threshold slope (SS) for the 3 structures at 90° and 77.6° fin taper. For typical D_{IT} numbers (4×10^{12}-$10^{13}cm^{-2}eV^{-1}$) reported for III-V high-k interfaces and observed in our fabricated FFs, the taper angle impacts SS in $In_{0.53}Ga_{0.47}As$ Bulk FF more than QWFF due to the larger sidewall area.

Conclusion: We show that, the enhanced mobility at higher indium percentage supports a higher drive current despite reduced sidewall area (n_s) for $In_{0.7}Ga_{0.3}As$ QWFF. R_{Ext} is also lowered in this device with raised S/D due to lower access resistance. Short channel $In_{0.7}Ga_{0.3}As$ QWFF in closely packed fin configuration (10 fins/μm) support I_{ON}=1.16mA/μm at V_G-V_T=1V, V_{DS}=0.5V and I_{OFF}=30 nA/μm. Calibrated model projects the I_{ON} for $In_{0.7}Ga_{0.3}As$ QWFF with W_{Fin}=8nm and L_G=10nm to be 1.5x higher than Si FF at matched I_{OFF}.

References

[1] D. H. Kim et al, IEDM 2010
[2] M. Radosavljevic et al, IEDM 2011
[3] Arun VT et al, Nanoletters 2014
[4] C. Auth et al, VLSI Symp 2012

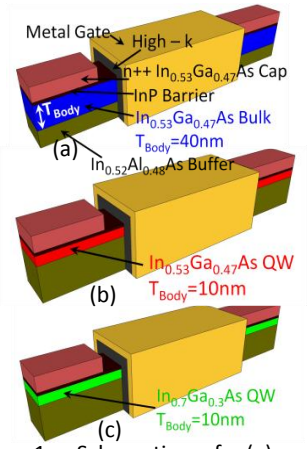
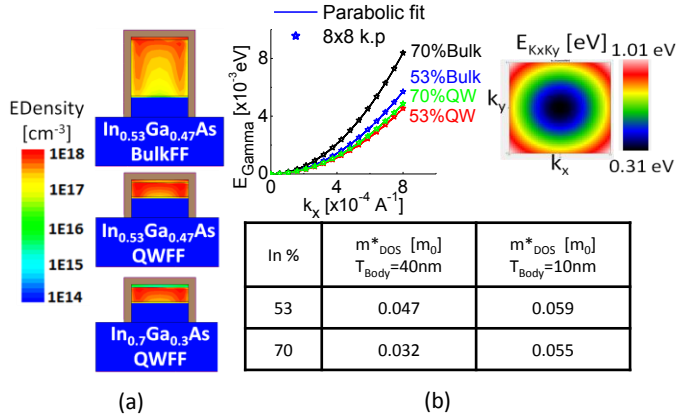


Fig 1: Schematic of (a) $In_{0.53}Ga_{0.47}As$ Bulk FF, (b) $In_{0.53}Ga_{0.47}As$ QW FF, and (c) $In_{0.7}Ga_{0.3}As$ QW FF.



In %	m^*_{DOS} [m_0] T_{Body}=40nm	m^*_{DOS} [m_0] T_{Body}=10nm
53	0.047	0.059
70	0.032	0.055

Fig 2: (a) Electron density profile in Fin x-section showing surface conduction for $In_{0.53}Ga_{0.47}As$ BulkFF vs. volume conduction for QW. (b) Parabolic fit of 8x8 k.p band structure gives lower effective electron mass, m_e^* (see Table) for $In_{0.7}Ga_{0.3}As$ QW than $In_{0.53}Ga_{0.47}As$ QW that ensures mobility enhancement in the former .

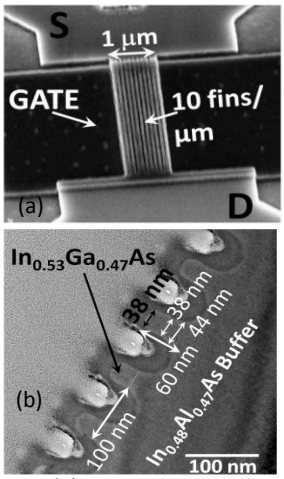


Fig 3:(a) SEM showing long channel FF with fin pitch of 100nm and W_{FIN}=38nm (b) TEM showing vertical fin profile and spacing.

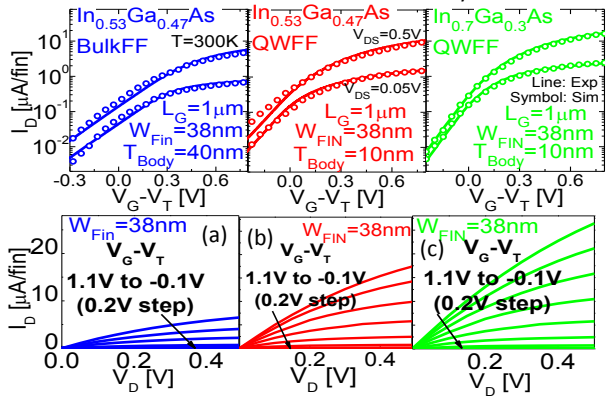
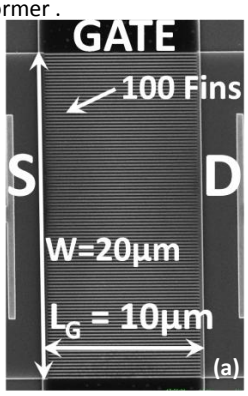


Fig 4: Experimental I_DV_G and I_DV_D characteristics per fin for long channel FFs: (a) $In_{0.53}Ga_{0.47}As$ Bulk FF, (b) $In_{0.53}Ga_{0.47}As$ QW FF, (c) $In_{0.7}Ga_{0.3}As$ QW FF. Symbols are calibrated simulation results using modified DD model.



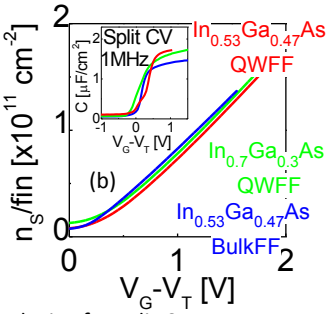


Fig 5: (a) SEM of multi (100)-fin device for split CV measurement fin pitch of 200nm and W_{FIN}=66nm. (b) Multi-fin split CV measurements at low temp. (inset) used to extract mobile charge concentration per fin in the three devices.

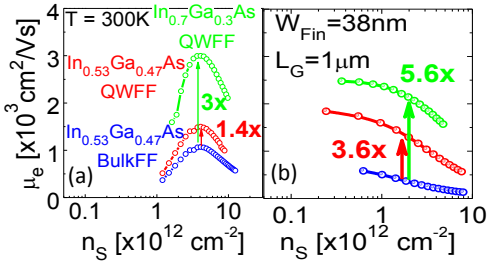
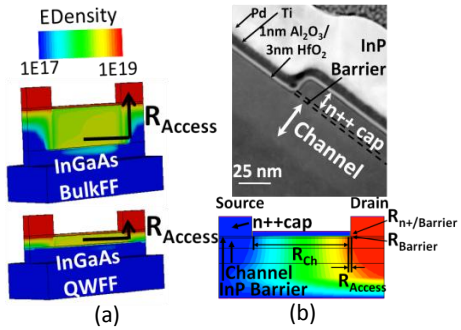


Fig 6: (a) Effective field effect mobility based on n_s from split CV measurements. (b) Drift mobility based on inverse modeling of fabricated FFs.



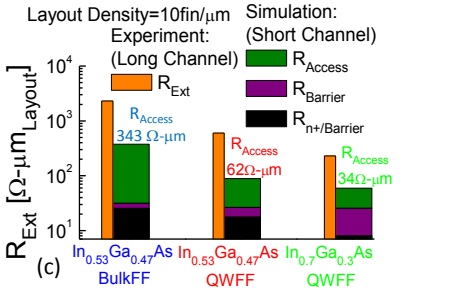


Fig 8: (a) Electrons traverse longer path to reach drain in Bulk FF vs QW FF. (b) TEM x-section and simulation set-up with R_{Ext} components: $R_{n+/Barrier}$, $R_{Barrier}$ and R_{Access}. (c) Raised SD favors QW architecture due to lower R_{Access} of 62 Ω-µm and 34 Ω-µm for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$, respectively. Lowest experimental/simulated R_{Ext} is obtained in $In_{0.7}Ga_{0.3}As$ QW FF. Higher In% lowers m* and reduces $R_{n+/Barrier}$.

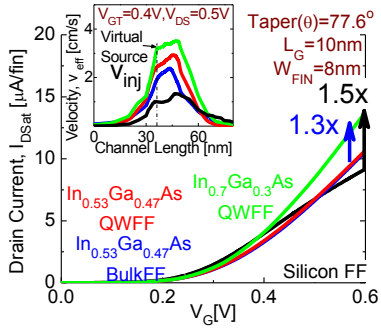


Fig 9: Simulated I_DV_G of L_G=10nm, W_{FIN}=8nm showing $In_{0.7}Ga_{0.3}As$ QW FF with 1.5x and 1.3x higher I_{ON} over Si FF [4] and $In_{0.53}Ga_{0.47}As$ BulkFF [2], respectively, at 0.5V V_{DD} and I_{OFF} = 10 nA/µm. Inset shows the v_{inj} of $In_{0.7}Ga_{0.3}As$ QW FF being 3.3 times higher than Si FF.

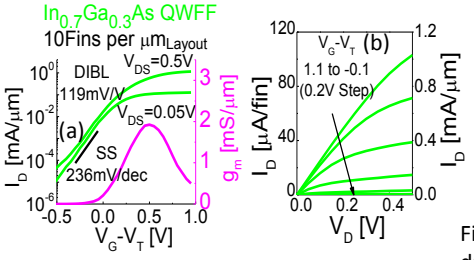


Fig 7: Experimental (a) I_DV_G and (b) I_DV_D of short channel $In_{0.7}Ga_{0.3}As$ QW FF with L_G=120nm and W_{FIN}=55nm. With layout density of 10 fins per µm layout width, 1.16mA/µm at V_G-V_T=1V, V_{DS}=0.5V. Peak g_m is 1.9mS/µm. I_{OFF} = 30 nA/µm. SS = 236 mV/dec. DIBL = 119 mV/V.

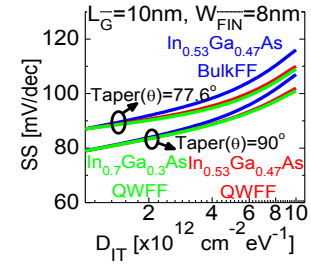


Fig 10: $In_{0.53}Ga_{0.47}As$ Bulk FF shows higher sensitivity to D_{IT} and fin profile compared to both QW FFs.