Microelectronics Reliability 54 (2014) 861–874

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory Invited Paper

Tunnel FET technology: A reliability perspective ☆

Suman Datta [a,*], Huichu Liu [a], Vijaykrishnan Narayanan [b]

[a] Electrical Engineering Department, The Pennslyvania State University, University Park, PA 16802, USA
[b] Computer Science Engineering Department, The Pennslyvania State University, University Park, PA 16802, USA

ARTICLE INFO

Article history:
Received 1 February 2014
Accepted 3 February 2014
Available online 4 March 2014

ABSTRACT

Tunneling-field-effect-transistor (TFET) has emerged as an alternative for conventional CMOS by enabling the supply voltage (V_{DD}) scaling in ultra-low power, energy efficient computing, due to its sub-60 mV/decade sub-threshold slope (SS). Given its unique device characteristics such as the asymmetrical source/drain design induced uni-directional conduction, enhanced on-state Miller capacitance effect and steep switching at low voltages, TFET based circuit design requires strong interactions between the device-level and the circuit-level to explore the performance benefits, with certain modifications of the conventional CMOS circuits to achieve the functionality and optimal energy efficiency. Because TFET operates at low supply voltage range ($V_{DD} < 0.5$ V) to outperform CMOS, reliability issues can have profound impact on the circuit design from the practical application perspective. In this review paper, we present recent development on Tunnel FET device design, and modeling technique for circuit implementation and performance benchmarking. We focus on the reliability issues such as soft-error, electrical noise and process variation, and their impact on TFET based circuit performance compared to sub-threshold CMOS. Analytical models of electrical noise and process variation are also discussed for circuit-level simulation.

1. Introduction

Continued transistor scaling and transistor density increasing have significantly increased the power density on chip. Supply voltage V_{DD} scaling leads to a quadratic reduction of the dynamic power consumption, which is highly desired for energy efficient computing in the power-constrained applications [1]. To achieve the same drive-strength (on-state current, I_{on}), the threshold voltage (V_{th}) has to be scaled proportionately while reducing the V_{DD} of a transistor, causing an exponential increase of the leakage current (I_{off}) and the static leakage power [2]. This exponential increase of I_{off} arises from the thermal limited 60 mV/decade sub-threshold slope (SS) in MOSFETs. The trade-off between the V_{th} reduction and low static leakage power slows the V_{DD} scaling, and thereby restrains the further power reduction for high-performance, low power digital applications.

By taking the advantage of the high energy filtering of the band-to-band tunneling (BTBT) mechanism, Tunneling Field Effect Transistor (TFET), as an alternative device architecture, has been proposed to further enable the V_{DD} scaling due to its sub-60 mV/decade steep switching at the room temperature [3]. Over the past decade, TFET has gathered tremendous interest, and various approaches have been explored to experimentally demonstrate high I_{on} and steep slope in TFETs. An SS of 30 mV/decade at 300 K has been achieved in both strained tri-gate nanowire Si n-type TFET [4], and vertical Si nanowire gate-all-around (GAA) p-type TFET [5]. Recent progress in the integration of vertical III–V nanowire-channels on Si led to a minimum subthreshold slope (SS) of 21 mV/decade with bias voltage V_{DS} of 0.1 V and 1 V [6]. Significant improvement of I_{on} (>100 μA/μm) at low V_{DD} (<0.5 V) was reported in III–V material based TFET [7–9]. Carbon nanotube (CNT) and Graphene nanoribbon (GNR) based TFETs were also investigated as alternative approaches ([10,11]). Recently, group IV materials ($Ge_{1-x}Sn_x$) have been explored as promising candidates to realize complementary TFETs with engineered direct band-gaps ([12,13]). Performance benchmarking for beyond-CMOS logic devices ([14]) shows that hetero-junction TFET (HTFET) can achieve optimal over 10^{15} Integer Ops/s/cm^2 at power consumption less than 1 W/cm^2, which is considered as the most promising energy efficient device compared to other electronic and spintronic devices. Given the practical limitations such as the asymmetrical device architecture induced uni-directional conduction, modifications of circuit designs (e.g. TFET SRAMs, pass-transistor logic) are required for TFET circuit implementation [15–17]. The increased device sensitivity to radiation, noise, process variation

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* Corresponding author.
E-mail addresses: sdatta@engr.psu.edu (S. Datta), hxl249@psu.edu (H. Liu), vijay@cse.psu.edu (V. Narayanan).

http://dx.doi.org/10.1016/j.microrel.2014.02.002
0026-2714/

at reduced V_{DD} pose further challenge on robust circuit operation using TFETs [18]. Thus, performance analysis taking into account of radiation induced soft-error, electrical noise and process variations, needs to be applied to evaluate TFET technology against low voltage CMOS.

In this review paper, we focus on the device design, characterization and performance benchmarking of III–V TFETs using the device-circuit co-design framework to analyze the soft-error performance, electrical noise profile and variation effects, providing more insights for energy efficient computing using TFET technology. This paper is divided into five sections. Section 2 describes the design approaches for III–V TFETs, performance benchmarking and simulation framework for TFET circuit implementation. In Section 3, we will discuss the radiation induced transient error generation in III–V TFET, and the circuit-level evaluation of the soft-error performance for low voltage applications. Section 4 presents the electrical noise characteristics of III–V TFET and analytical models for circuit implementation. The variation effects on III–V TFET compared to sub-threshold Si-FinFET are explored in Section 5 with performance fluctuation evaluation for low voltage SRAMs. Conclusions are provided in Section 6.

2. Interband Tunnel FET (TFET) technology for energy efficient computing

2.1. TFET design, fabrication and characterization

The current generation in MOSFETs is determined by the thermionic emission of high energy carriers, in which only carriers with energy exceeding the source-channel electrostatic potential barrier contribute to the on-state current. These high energy carriers follow the Fermi–Dirac distribution and hence have an energy slope of kT (where k is the Boltzman constant, T is the absolute temperature), causing a thermal limited sub-threshold slope of 60 mV/decade at the 300 K (room temperature). Unlike MOSFETs, TFETs are designed with asymmetrical source/drain doping (p-i-n) as reverse-biased gated p-i-n diodes (Fig. 1a). The current generation in TFETs is enabled by the band-to-band tunneling (BTBT) at the source-channel junction, in which the carriers at the high energy tail of the Fermi–Dirac distribution are filtered by a tunneling window [3]. Thus, a sub-60 mV/decade SS, in principle, can be achieved in TFET.

The key challenges in TFET design involve the high on-state current, which is limited by the tunneling probability, and the steep sub-threshold slope, which can be degraded by the thermal energy determined trap-assist-tunneling (TAT) [19]. Thus, the design of TFET involves: the choice of material systems for tunneling barrier reduction, good gate electrostatics for steep SS and I_{on}/I_{off} ratio, reducing the interface traps to suppress the TAT. Low band-gap (E_g) materials (e.g. germanium, III–Vs, etc.) offer both low effective mass (m^*) and freedom to achieve hetero- band-alignment to improve the tunneling probability (T_{WKB}) at low voltage. Tunnel junction with steep doping profile and low defects are also critical for TAT reduction and steep SS. Improved gate-control going from the planar device structure towards the gate-all-around nanowire structure can further improve the gate electrostatics with steep SS and high I_{on}. The quality of the gate-dielectrics is essentially important for the effective gate-control in transistor operation.

Based on the device design requirement, III–V semiconductors are attractive for TFET fabrication due to their direct band-gaps and wide range of compositionally tunable band-alignment [20,21,19]. Our previous work in [22,7] first demonstrated the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ HTFET with MOSFET-like on-current, by taking advantages of the effective tunneling barrier reduction at the source-channel junction without reducing the band-gap of the channel material, which led to a simultaneous enhancement of the I_{on} and I_{on}/I_{off} ratio (Fig. 1b and c). Tables 1 and 2 present the performance of the fabricated TFETs from selected literature data, showing the progress in TFET development toward ultra-thin body, gate-all-around, highly scaled EOT and broken-gap tunneling junction design with continuously improved I_{on} and steep slope for both n-type [20,23,24,7,25,8] and p-type TFETs [13,26–28,4]. The recent work in [4] demonstrated the first strained-Si nanowire complementary TFET inverter operating at $V_{DD} = 0.2$ V with the

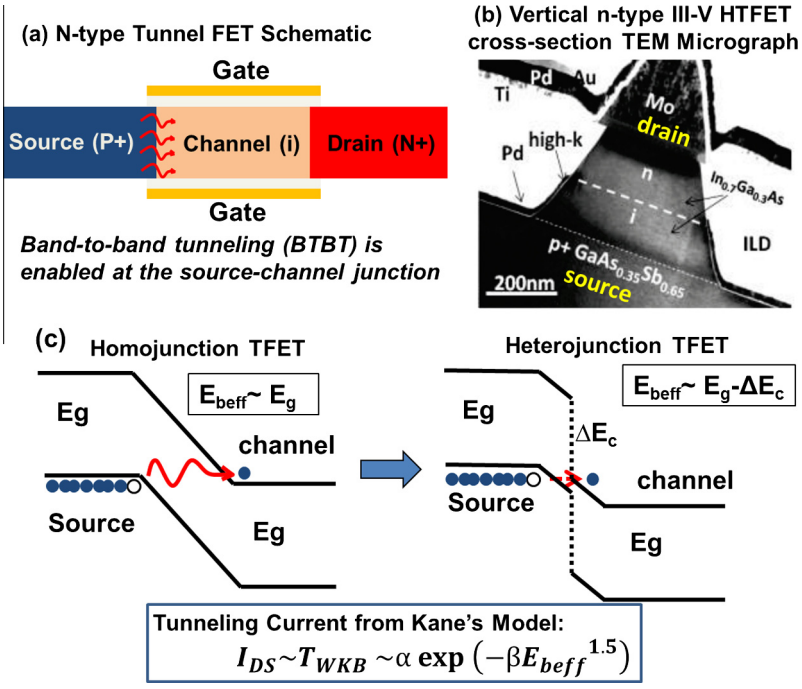


Fig. 1. (a) Double-gate Tunnel FET schematic. (b) Fabricated III–V HTFET Transmission electron microscopy (TEM) micrograph. (c) Tunneling barrier engineering from homojunciton TFET to heterojunction TFET for on-state current improvement by tunnel barrier E_{beff} reduction.

Table 1
Fabricated n-TFET device characteristics.

NTFET reference	Source-channel material	EOT (nm)	I_{ON} (μA/μm)	V_{DS} (V)	$V_{ON} - V_{OFF}$ (V)	I_{ON}/I_{OFF}	S_{MIN} (mV/dec)	S_{EFF} (mV/dec)
Zhou IEDM 2012	GaSb–InAs	1.3	180	0.5	1.5	6e3	200	400
Zhou EDL 2012	InP–InGaAs	1.3	20	0.5	1.75	4.5e5	93	310
Mohata VLSI 2012	GaAsSb–InGaAs	1.75	135	0.5	1.5	1.7e4	230	350
Zhao APL 2011	$In_{0.7}Ga_{0.3}As$	1.2	40	0.5	2	2e5	84	380
Li EDL 2012	AlGaSb–InAs	1.6	78	0.5	1.5	1.6e3	125	470
Dewey IEDM 2011	$In_{0.53}Ga_{0.47}As$	1.1	5	0.3	0.9	7e4	58	190

Table 2
Fabricated p-TFET device characteristics.

PTFET reference	Source-channel material	EOT (nm)	I_{ON} (μA/μm)	V_{DS} (V)	$V_{ON} - V_{OFF}$ (V)	I_{ON}/I_{OFF}	S_{MIN} (mV/dec)	S_{EFF} (mV/dec)
Jeon VLSI 2010	SOI	~0.9	1.2	−1	−1	7e7	32	47
Mayer IEDM 2008	GeOI	~2.2	3	−1	−1.5	1.4e2	130	200–300
Villalon VLSI 2012	Strained SiGe/SOI	1.25	112	−1	−1.5	3.1e6	33	133
Yang IEDM 2012	GeSn	–	4.3	−1	−1	1e2	–	~750
Knoll APL 2013	Strained Si nanowire	2.2	10	−0.5	−1.2	~1e7	90	~120

first time transient response characterization. Moreover, the high frequency switching of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken-gap HTFET was demonstrated in [9], showing intrinsic cut-off frequency (f_T) of 22 GHz and 39 GHz at a channel-length of 200 nm at 0.3 V and 0.5 V, respectively. Improved f_T at low DC power was projected with the channel-length scaling. Therefore, TFET technology exhibits great potential to overcome the energy efficiency challenge for ultra-low power digital and mixed-signal/analog applications.

2.2. Device-circuit co-design framework for TFET performance benchmarking

For circuit-level implementation and performance evaluation, it is of interest to develop compact analytic models for TFET for use in circuit simulator. Many works on TFET compact models and analytical expressions development have been reported focusing on specific aspects such as TFET designs, operation regions and performance projections, including the different gate configurations [29,30], output characteristics [31], and scaling impact [32]. To meet the circuit and system design purpose, simple, accurate and predictive SPICE models to describe the device operation of TFET are yet to be developed.

For III–V HTFET based circuit evaluation, we employed the look-up table based Verilog-A model incorporating with TCAD Sentaurus device simulation for TFET based circuit implementation [15,33]. The GaSb–InAs III–V HTFET device model was calibrated with full-band atomistic simulations in [15] with a dynamic non-local band to band tunneling model to account accurately for the inter-band tunneling transitions in III–V HTFET. A baseline Si-FinFET Verilog-A model was also generated using TCAD Sentaurus and calibrated against experiment data in [34]. At the gate-length of 20 nm, III–V HTFET exhibits 7 times I_{on} improvement at $V_{DD} = 0.3$ V with an average sub-threshold slope of 30 mV/decade, $I_{off} = 5$ nA/μm. Our results agree well with the atomistic NEGF simulation projection in [35].

The two-dimensional look-up tables in Verilog-A models include the transfer characteristics $I_{DS}(V_{GS}, V_{DS})$, the gate-source capacitance $C_{Gs}(V_{GS}, V_{DS})$ and the gate-drain capacitance $C_{GD}(V_{GS}, V_{DS})$ across a range of drain-source voltage bias V_{DS} and gate-source voltage bias V_{GS}, obtained from DC and small-signal simulation. Hence, the Verilog-A models can capture both DC and transient characteristics in the circuit-level analysis. Fig. 2 illustrates the Verilog-A model schematic of III–V HTFET, and the voltage transfer characteristics and the transient output characteristics of a HTFET based inverter for model validation.

Fig. 3 shows the performance benchmarking of the III–V HTFET based inverter with fanout = 1 (FO1 inverter) and 32-bit prefix-tree Hans-Carlson Adder compared to the Si-FinFET based circuits [33]. HTFET inverter outperforms Si-FinFET inverter below 0.5 V, with a favorable energy-delay trade-off, where Si-FinFET inverter is limited by the static leakage energy below 0.3 V at low activity (1%). Similarly, the 32-bit Adder evaluation reveals the energy consumption minima at 0.3 V for Si-FinFET 32-bit Adder, while III–V HTFET 32-bit Adder shows continued energy reduction with V_{DD} scaling. The improved energy-delay performance of III–V HTFET arises from the steep slope induced high I_{on} and high I_{on}/I_{off} ratio at reduced V_{DD}.

2.3. TFET based Static Random Access Memory (SRAM) design

The Verilog-A model based device-circuit co-design framework has been widely applied in TFET based circuit implementation, to explore the potential energy efficiency benefits for low-power digital and analog/RF applications [33,15,16,36,37,17]. Here we present III–V HTFET based Static Random Access Memory (SRAM) design as in [15] to showcase the design aspects for TFET based circuits. Different SRAM topologies were studied as candidates for III–V HTFETs, taking into account of the advantages from improved drive current at low V_{DD} as well as the shortcomings from the unidirectional conduction due the asymmetrical source/drain design (p-i-n structure).

Due to the unidirectional conduction, modification of the traditional 6-transistor (6T) based CMOS SRAM cell with higher transistor number is required for read/write operation. Fig. 4 illustrates the SRAM cell schematics of 8T TFET Transmission-Gate (TG) SRAM, 8T/10T dual-port (DP) SRAM, TFET Schmitt-Trigger (ST) SRAM. The benchmarking of these TFET based SRAM designs are shown in Fig. 5, including read-noise-margin (RNM), write-noise-margin (WNM) and energy-delay performance with supply voltage scaling. We observe that the utility of the Schmitt-Feedback [38] can provide significant noise-margin improvement for HTFET SRAM cell design. HTFET based SRAM designs present significant delay reduction below 0.4 V, and dynamic energy reduction below 0.3 V, due to the drive-current enhancement at low voltage compared to sub-threshold Si-FinFET SRAM designs.

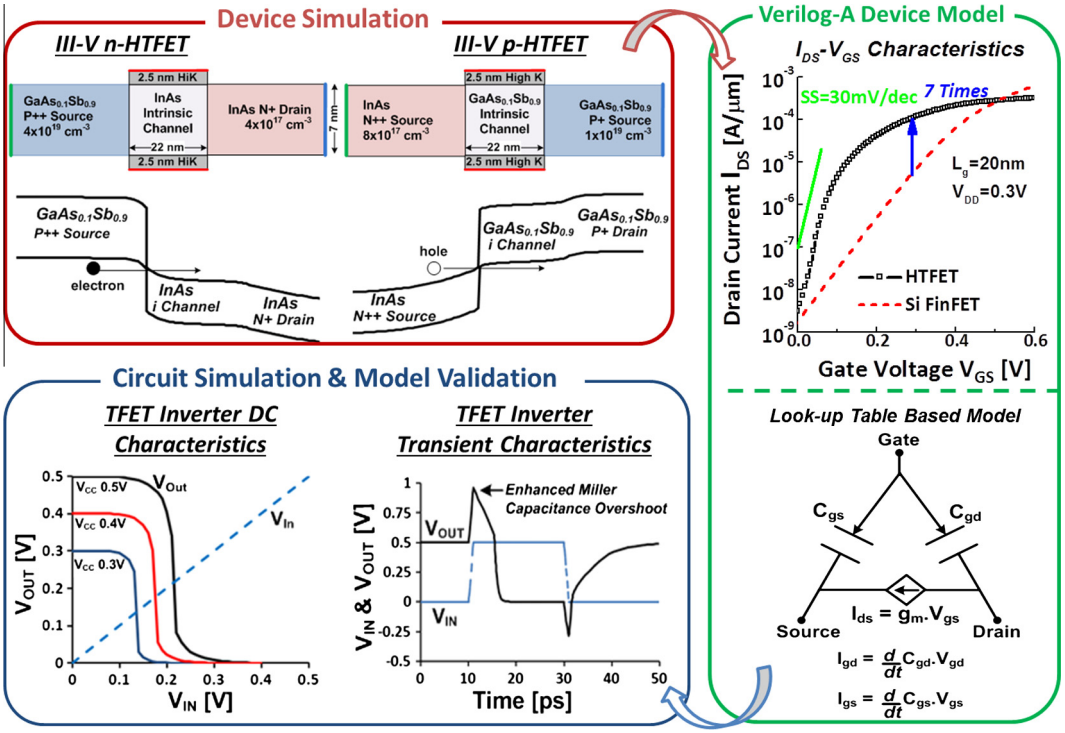


Fig. 2. Look-up table based verilog-A model generated from Sentaurus TCAD device simulation to perform TFET circuit analysis. DC and transient characteristics can be successfully captured.

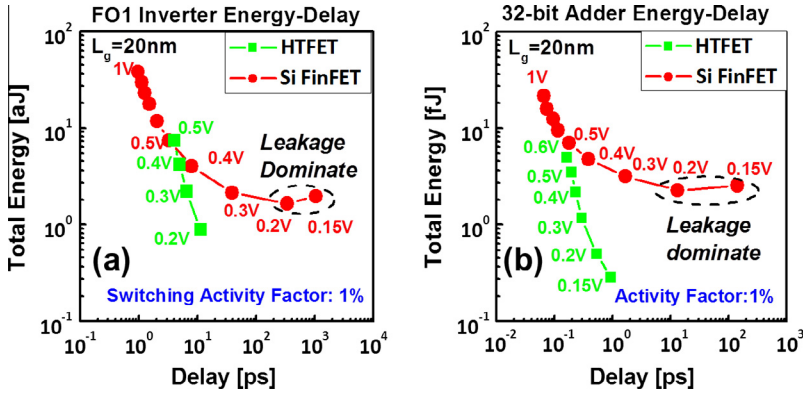


Fig. 3. (a) Fanout = 1 (FO1) inverter energy delay comparison for 20 nm Si FinFET and HTFET. HTFET shows improved energy efficiency for below 0.5 V operation, while Si FinFET reaches the leakage bound at $V_{cc} = 0.15$ V. (b) 32-bit Hans-Carlson Adder energy-delay evaluation for 20 nm HTFET and Si FiFET at activity factor of 1%.

3. TFET soft-error performance

3.1. Radiation reliability challenge for low power devices

Radiation induced single-event upset (SEU), also known as soft-error, has become the key challenge for data center applications with growing number of computation nodes [39]. The projected 100 times increase of the soft-error rate (SER) per chip from 180 nm to 16 nm technology node can cause a significant degradation of system reliability, considering the 8% increase of the SER per logic state bit for each technology generation [39]. V_{DD} scaling imposes further challenges to sustain a low SER due to the circuit node charge reduction [40,41]. As discussed in Section 2, narrow band-gap materials are attractive for channel replacement due to the mobility enhancement for low power devices, and also known as good candidates to realize TFETs for tunneling barrier reduction. However, these narrow band-gap materials generally have low ionization energies, and hence are more sensitive to radiation compared to silicon [42]. In [43], we investigate the radiation induced soft-error generation and propagation in III–V GaSb–InAs HTFET based circuits compared to Si-FinFET and III–V FinFET (InAs as channel material, same as III–V HTFET).

3.2. Transient current generation and bipolar gain effect reduction in Tunnel FET

We adopt the TCAD Sentaurus heavy ion model [44] to simulate the generated electron/hole (e/h) pairs along the ion track, and analyze the radiation induced transient current generation in III–V HTFET. The linear energy transfer (LET) describes the generated charge per length along the ion track. The generated charge results in transient current at the device off-state where $V_{GS} = 0$ V, $V_{DS} = V_{DD}$.

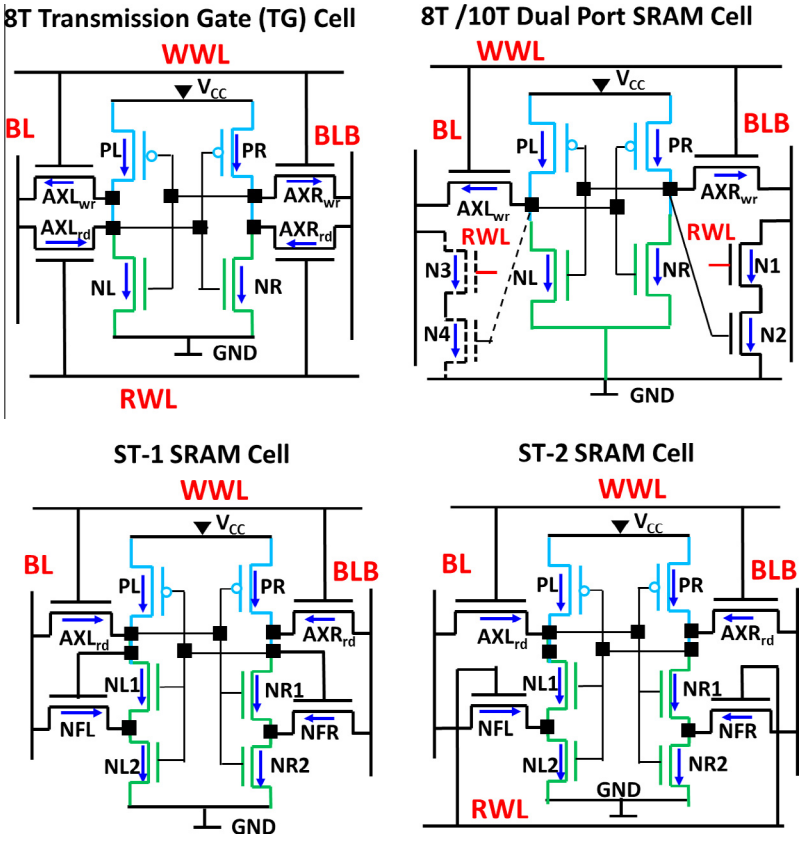


Fig. 4. SRAM design examples using HTFETs: 8T Transmission Gate (TG) cell, 8T (10T) dual port (DP) cell, ST-1 and ST-2 with Schmitt-feedback. TFET orientation is illustrated in each design.

The transient current generation in fully-depleted-channel devices can be enhanced by the bipolar gain effect [45]. In n-type Si-FinFET, the radiation induced electrons in the channel are collected at the drain due to the source-drain bias, while the generated holes are stored in the body due to the source-channel barrier (Fig. 6). This hole storage increases the channel potential and reduces the source barrier, causing additional electrons flowing into the channel and increasing the transient current (Fig. 7), which is known as bipolar gain effect.

Due to the built-in p-i-n structure and the presence of the tunneling barrier at the source-channel junction, the source barrier lowering effect in TFET is eliminated. Both electrons and holes are collected through the ambipolar transport (Fig. 7), which reduces the bipolar gain effect. As a result, III–V HTFET exhibits approximately 80% reduction in transient duration and 90% reduction in collected charge over Si-FinFET at $LET = 100\ \mathrm{fC}/\mu m$, $V_{DD} = 0.5$ V, while III–V FinFET shows higher transient current magnitude and charge collection than Si-FinFET due to its reduced source-channel barrier.

3.3. Simulation methodology for soft-error rate evaluation

Due to the practical limitation of the radiation measurements for the emerging logic devices and circuits, we develop the SER evaluation methodology involving the charge deposition, transient current generation and critical LET extraction from material and device-level to circuit-level as shown in Fig. 8. GENAT4 [46] Monte Carlo simulation is used for the neutron radiation induced charge deposition using the measured neutron spectrum [47]. 2.06 times enhancement of charge deposition over Si is observed for InAs by integrating the sea-level neutron energy range from 10 MeV to 1000 MeV (soft-error sensitive) [48]. The deposited charge, described as LET, is applied to the TCAD device models to generate the transient current profile library, and then used as transient input at the victim nodes for time-domain circuit simulation using Spectre [49]. SER calculation is carried out by using the technology adaptable empirical model [50].

3.4. Soft-error performance of TFET SRAMs and TFET combinational logic

For SRAM SER analysis, the neutron strike is induced at the n-type transistor (as victim device) connected to the bit-node, which initially stores 1. The bit-node recovers for low LET due to the cross-coupling feedback loop, but eventually flips as LET increases. 6T Si and III–V FinFET SRAM cell (except HTFET) and iso-area 10T ST2 SRAM cell for Si and III–V FinFET and III–V HTFET are evaluated with V_{DD} scaling (Fig. 9), considering the required noise-margin for TFET SRAM design as discussed in Section 2.3. A cross-over of the extracted critical LET comparing Si-FinFET cell to III–V FinFET cell is observed at $V_{DD} = 0.5$ V, indicating the improved drive current of III–V FinFET compensates the enhanced charge deposition. For 10T TFET SRAM cell, 4.5 times and 7 times improvement of the critical LET are achieved at 0.5 V and 0.3 V respectively, contributed from both the reduced charge collection as described in Section 3.3, and the enhanced on-state Miller capacitance effect [51] as radiation-hardening coupling-capacitance [52] to assist the node recovery.

In combinational logic circuits, error propagation and error rate are strongly impacted by the electrical and latching window masking effects. Fig. 10 illustrates the electrical masking in FO1 inverter chain and latching window masking in NAND based D Flip Flop

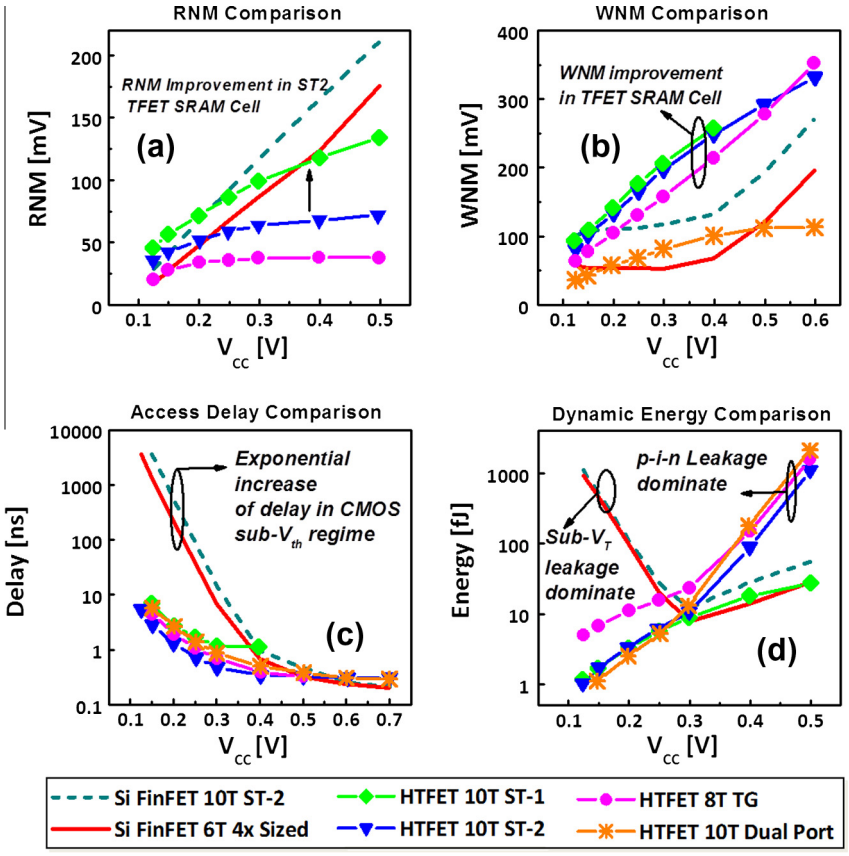


Fig. 5. (a) Read-Static Noise Margin (RNM) and (b) Write-Static Noise Margin (WNM) evaluation for different TFET SRAM cell designs as compared to 4 × sized Si FinFET 6T baseline design (as an iso-area comparison) and 10T ST2 cell design. HTFET 10T ST2 design shows desired noise margin for low V_{CC} operation. Performance benchmarking of (c) access delay and (d) energy consumption with supply voltage scaling for different TFET SRAM cell designs comparing with Si FinFET SRAM cell designs. HTFET SRAM cells exhibit reduced delay and improved energy efficiency for low V_{CC} operation.

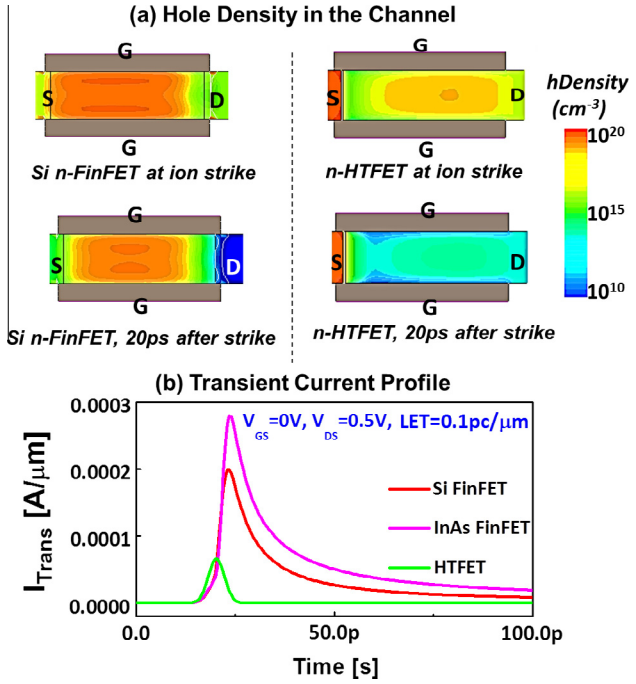


Fig. 6. (a) Ion strike induced electron/hole pair generation in n-type HTFET and Si FinFET schematics. (b) Band diagrams for Si n-FinFET and nHTFET before/after ion strike. Hole storage induces barrier lowering and additional charge collection (bipolar gain) in Si n-FinFET. For nHTFET, holes can be collected at source, which reduces the bipolar gain effect.

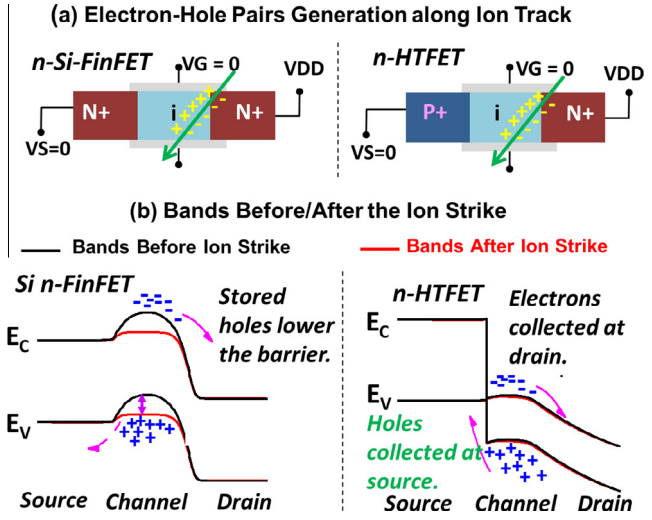


Fig. 7. (a) Time evolution of hole density in n-type device channel region. Hole density decreases fast in nHTFET due to the ambipolar transport by the reversed biased p-i-n structure. (b) Radiation induced transient current profile for n-type Si FinFET, III–V (InAs) FinFET and III–V HTFET.

(DFF). The victim node is assumed at the input of the first-stage inverter, causing a transient voltage pulse propagating along the inverter chain. When the propagated voltage reaches the DFF during the latching window and its pulse width (d) exceeds the latch window (w), an error is latched by the DFF. We extract the LET causing

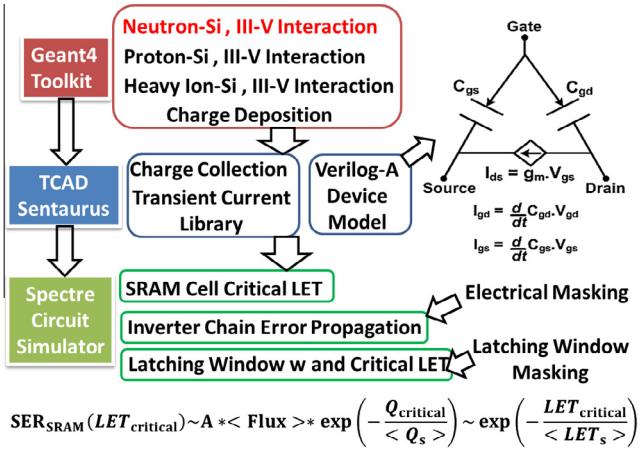


Fig. 8. Soft-error-rate (SER) evaluation methodology.

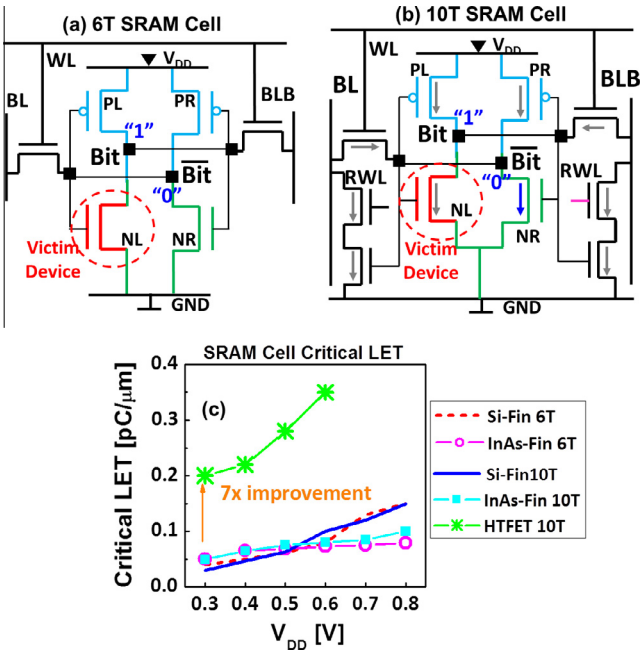


Fig. 9. (a) 6T and (b) 10T SRAM cell schematics. Strike on storage node induced charge exceeding node charge can cause an error. HTFET (unidirectional) current flow direction is illustrated for 10T cell. (c) Extracted critical LET for 6T and 10T iso-area SRAM for Si FinFET, III–V FinFET and 10T HTFET with voltage scaling. HTFET shows 7 times improvement compared to Si FinFET at 0.3 V for 10T case.

the voltage pulse latched as the latching window critical LET. The probability of an error in combinational logic is determined by the ratio (w/c) of the latch window (w) to the clock cycle (c) and the critical LET. A higher drive current can reduce the latching window w of DFF and hence reduce w/c, but also reduces critical LET. Fig. 11 shows the extracted latching window w and latching window critical LET comparing Si, III–V FinFETs and III–V HTFETs with V_{DD} scaling. TFET DFF outperforms Si and III–V FinFET DFF below 0.6 V and 0.4 V, resulting in a reduced latching window. 8 times improvement of the latching window critical LET is observed for III–V TFET circuits at 0.3 V compared to Si-FinFET circuits due to

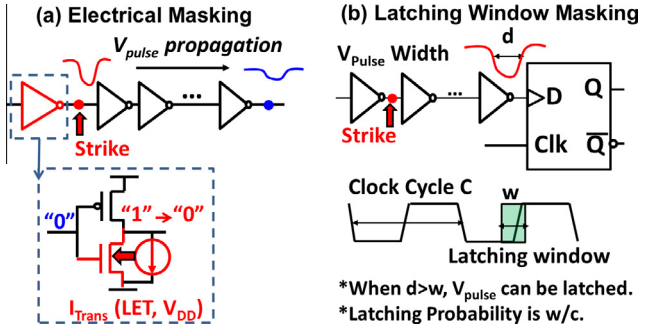


Fig. 10. (a) Electrical masking effect illustration using FO1 inverter chain. The strike is induced at the 1st stage nFET, where the transient current causing a voltage pulse. (b) DFF latch window masking schematic. Propagated transient voltage pulse width d exceeding the latch window w can be latched with the probability of w/c.

the reduced transient current magnitude and duration as described in Section 3.2.

3.5. SER evaluation with voltage scaling

Given the charge deposition analysis and critical LET extraction, the SRAM cell SER and logic SER are calculated based on the methodology described in Section 3.2. Fig. 12a and b shows the relative SRAM SER and logic SER for Si-FinFET, III–V FinFET and III–V HTFET with V_{DD} scaling, respectively. III–V FinFET shows increased charge deposition due to low ionization energy, which increases the SER for SRAM cell for all V_{DD} compared to Si-FinFET. For combinational logic, III–V FinFET shows reduced SER compared to Si-FinFET below 0.5 V due to improved latching window masking. With the same channel material as III–V FinFET, III–V HTFET, however, shows superior soft error resilience for voltage range from 0.3 V to 0.6 V for both SRAM and logic. III–V HTFET shows superior radiation resilience compared to both Si and III–V FinFET over the voltage range from 0.3 V to 0.6 V for both SRAM and combinational logic. This fundamental advantage stems from the bipolar gain reduction, the on-state enhanced Miller capacitance effect and the improved latching window masking with on-current improvement at low V_{DD}, making III–V HTFET a promising candidate for radiation resilient ultra-low power applications.

4. TFET noise performance

Electrical noise poses a growing reliability concern for optimal system design at scaled technology nodes [53,54]. Due to the increased sensitivity of circuit performance and reduced signal range at low V_{DD}, the noise figure is one of the key design factors in both analog/mixed-signal and RF circuits as well as semiconductor memories [55,56]. Thus, it is of great importance to evaluate the electrical noise characteristics for TFET as pursuing the power reduction.

4.1. TFET flicker noise characterization and analytical modeling

The flicker noise is the dominant low frequency noise arising from trapping/de-trapping of carriers in multiple trap states in the gate oxide [54]. Due to the BTBT determined current transfer characteristics, the source-channel tunneling barrier (E_{beff}) design strongly affects the flicker noise characteristics in III–V TFETs. In [57], we characterize the flicker noise performance of $In_{0.7}Ga_{0.3}As$ homojuntion with $E_{beff} = 0.58$ eV (Homoj-TFET) and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterojunction TFETs (Heteroj-TFET) with $E_{beff} = 0.25$ eV to analyze the impact of hetero-interface on flicker noise. Flicker noise measurements were performed at 77 K and 300 K with a constant V_{DS} of 500 mV (Fig. 13). At 300 K,

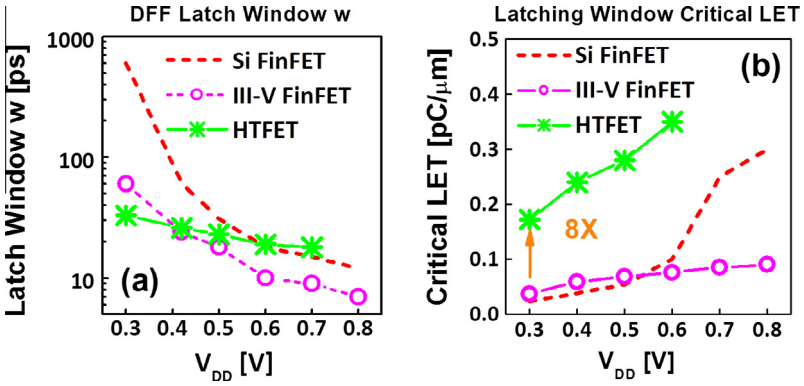


Fig. 11. (a) Latch window w comparison with V_{DD} scaling. HTFET D Flip Flop (DFF) outperforms Si FinFET and III–V FinFET based DFFs at 0.4 and 0.6 V. (b) Latching window critical LET. HTFET shows 8 × critical LET improvement compared to Si FinFET at 0.3 V. III–V FinFET shows a cross-over at 0.5 V due to reduced latching window to clock cycle ratio, w/c.

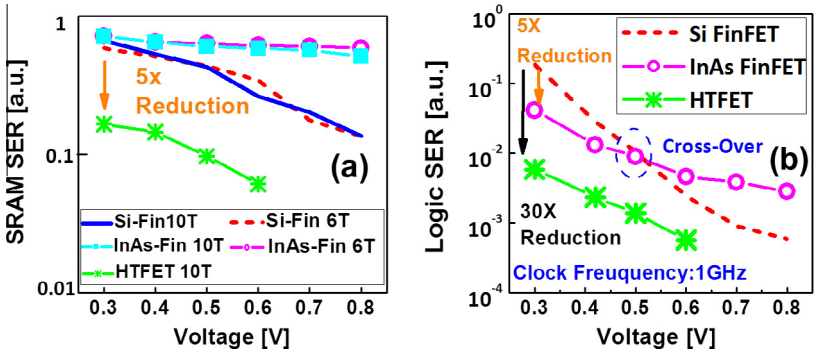


Fig. 12. (a) SRAM SER and (b) logic SER comparison with voltage scaling for Si, III–V FinFET and HTFET. HTFET shows superior soft error resilience for both SRAM and logic. III–V FinFET logic shows lower SER below 0.5 V over Si FinFET logic.

Homoj- and Heteroj- TFETs exhibit comparable normalized drain current noise levels, where both BTBT and trap assisted tunneling (TAT) affect the transfer characteristics. At 77 K, where only BTBT dominates, Heteroj-TFET shows much lower flicker noise than Homoj-TFET at a given drain current.

Based on the experiment results, an analytical model using the carrier number fluctuation theory is proposed (Fig. 14) [57]. In TFET, the spread of the BTBT generated carriers in the channel is much smaller than the channel length, which is defined as the effective channel length L'. Thus, the electron within L' gets trapped/de-trapped to the oxide traps when its energy is around the quasi-fermi level of the channel electrons. As a result, the fluctuation in the trapped charge lead to fluctuation in the junction electric field and hence the band-to-band generation rate. Due to the lower electric field arising from the smaller E_{beff} at a given drain current, Homoj-TFET has a smaller L' than Heteroj- TFET. For Heteroj- TFET at a given drain current, smaller E_{beff} and larger L' results in lower flicker noise level. As shown in Fig. 13, assuming $N_t = 1 \times 10^{13}$ cm^{-2}, the proposed analytical model shows excellent agreement with the measured noise spectrum.

4.2. TFET random telegraph noise (RTN) simulation

The source of RTN in both TFET and Si-FinFET is attributed to capture and emission of channel carriers by the individual interface traps [58,59] as observed in highly scaled technology node [60]. RTN characteristic and its impact on device design and circuit performance have been investigated in [61,62] for Si TFET technology. In [63], we evaluate the RTN characteristic of III–V HTFET using TCAD simulation, to investigate the drain current fluctuation (RTN amplitude) induced by a trapping of an electron charge in an acceptor-type interface-state at the gate oxide-channel interface. Because a trapped charge near the source can alter the junction electric field and hence affect the BTBT rate, the RTN of TFET can be more profound when the trap is located near the source-end of the channel. This is different from Si-FinFET, where the maximum RTN amplitude occurs near the mid-channel region due to the screening of the high concentration of electrons in the channel and the presence of the drain field [64]. Fig. 15a reveals that the maximum RTN amplitude with gate length L_g scaling comparing III–V HTFET and Si-FinFET at $V_{GS} = 0$ V and 0.3 V. At $V_{GS} < 0.3$ V, the RTN amplitude of III–V HTFET is reduced compared to Si-FinFET and decreases rapidly as V_{GS} approaching 0 V. Compared to Si-FinFET, the lower RTN amplitude of the III–V HTFET is due to the higher carrier concentration in the channel at low V_{GS} arising from the steep switching, which screens the charge trap and hence reduces the RTN amplitude. Also, while Si-FinFET exhibits increased RTN with physical L_g scaling, the RTN amplitude of III–V HTFET does not scale inversely with L_g due to the effective channel length L' determined drain current as discussed in Section 4.1. Fig. 15b shows the proposed analytical model for III–V HTFET based on the carrier number fluctuation theory, which agrees well with the numerical simulation over a V_{DD} range of 0.1 V to 0.5 V. In summary, the increased screening of the charge trap from higher channel carrier concentration in HTFET, accompanied by the weak dependence of RTN on the physical gate length scaling, enables 40% reduction of relative RTN amplitude in HTFET as compared to Si-FinFET at $V_{DD} = 0.3$ V, $L_g = 20$ nm.

4.3. TFET RTN effect on low voltage SRAM design

At sub-20 nm technology nodes, SRAM is known as the most vulnerable digital component to RTN due to the usage of the minimum sized transistor [56,60]. In [65], we implemented the RTN

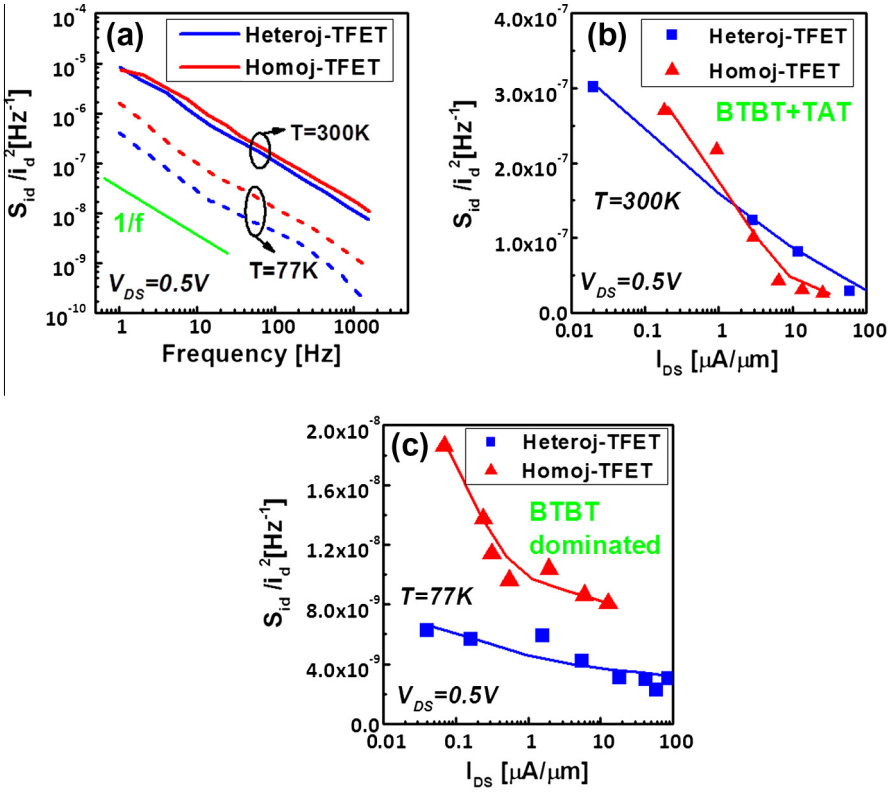


Fig. 13. (a) Flicker noise power measurements comparing Homoj-TFET and Heteroj-TFET *vs.* frequency for $T = 300$ K and 77 K, where Heteroj-TFET shows lower noise power at 77 K. (b) Flicker noise analysis at 300 K, both BTBT and TAT determine the noise power. (c) Flicker noise analysis at 77 K showing BTBT dominated noise power.

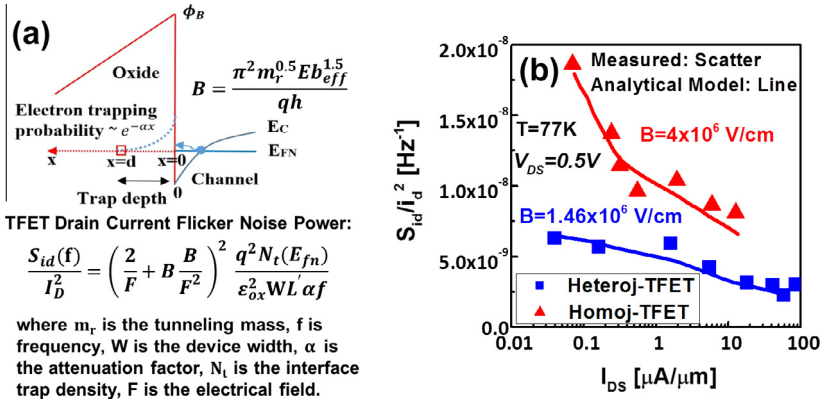


Fig. 14. (a) TFET Flicker noise analytical model based on the pure BTBT assumption. Trapping/detrapping of electrons around E_{fn} into the trap states in the oxide results in flicker noise. (b) Proposed analytical model is in excellent agreement with the experimental data.

analytical model in circuit simulation to evaluate TFET based SRAM designs from the RTN immunity perspective. As discussed in Section 2.3, III–V HTFET based 10T Schmitt-Trigger SRAM (ST2 SRAM topology) shows improved read/write noise margins as compared to Si-FinFET 10T ST2 SRAM and iso-area 6T SRAM, which is used in our study. Given the effect of RTN on each transistor exhibits as a threshold voltage shift ΔV_{th}, 1024 combinations in a 10T ST2 SRAM cell are evaluated to identify the impact on SRAM read/write noise margins. Fig. 16 shows the RNM and WNM distribution at $V_{cc} = 0.25$ V comparing III–V HTFET and Si-FinFET ST2 SRAM cell, where the worst case degradations of RNM and WNM are still comparable. RNM/WNM of ST2 SRAM for the worst case RTN with V_{cc} scaling are shown in Fig. 17 comparing HTFET and Si-FinFET ST2 SRAM, where Si-FinFET SRAM shows significant RNM/WNM degradation (>30%) at sub-0.2 V due to extremely low I_{on} compared to III–V HTFET. At ultra-low V_{cc}, higher I_{on} and higher I_{on}/I_{off} ratio of HTFET lead to the improved screening effect of the traps and thereby reduce the RTN caused noise margin degradation.

To compare the RTN performance of an iso-area 6T Si-FinFET SRAM, we use 4 × sized transistors for the 6T Si-FinFET SRAM to evaluate the noise margin of the worst case RTN as compared to 10T ST2 Si-FinFET and HTFET SRAM. We also evaluate the power-delay metric of the 256 × 256 SRAM array at an activity factor of 5% (Fig. 18). At $V_{cc} = 0.175$ V HTFET ST2 SRAM shows 43.24% and 11.1% improvement of worst case RNM over 4 × sized 6T Si-FinFET SRAM and 10T ST2 Si-FinFET SRAM, respectively, and 75 times and 21 times faster read-access time as compared to FinFET ST2 SRAM and FinFET 6T-4 × sized SRAM respectively. Our analysis showcases

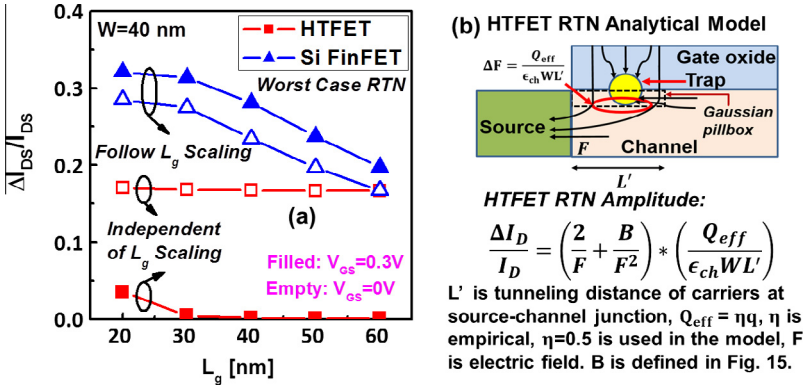


Fig. 15. (a) Gate length dependence of relative RTN amplitude. HTFET RTN does not increase inversely with L_g scaling as tunneling distance of carriers shows weak dependence onL_g. Off-state at $V_{gs} = 0$ V RTN is also shown for reference. (b) RTN analytical modeling. Single charge trap reduces electric field near source-channel junction. The reduction in electric field is approximated assuming an effective charge Q_{eff} in channel and applying Gauss Law.

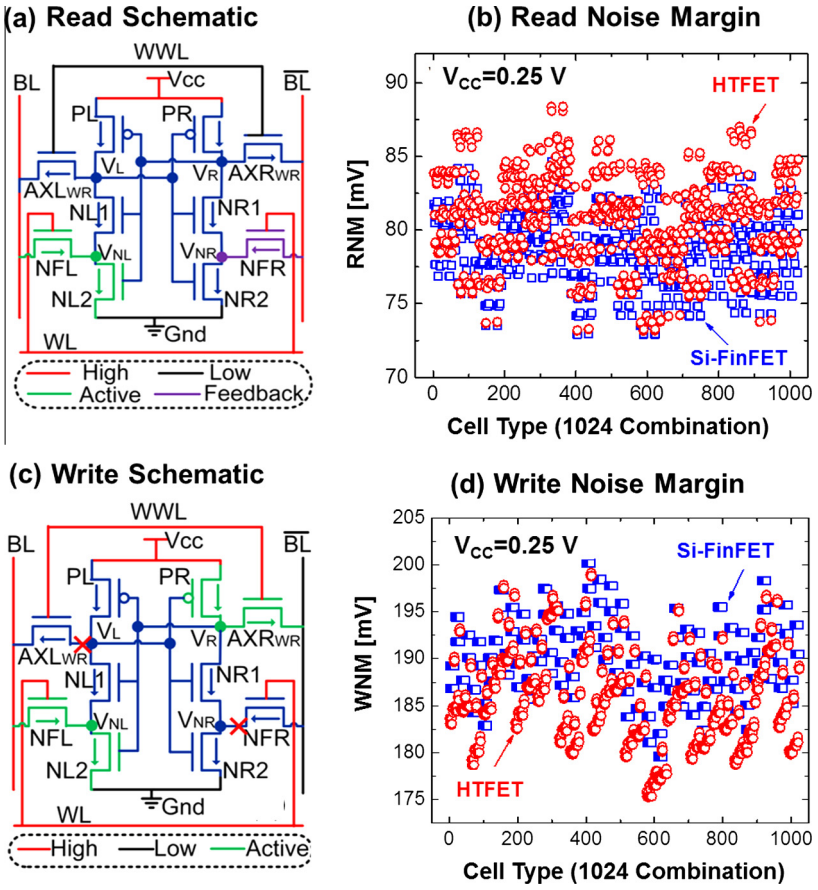


Fig. 16. 10T ST2 SRAM (a) read schematic (b) RNM in presence of RTN in 1024 possible cell types (c) write schematic (d) WNM in presence in 1024 possible cell types at 0.25 V comparing Si FinFET and TFET based design.

that HTFET ST2 SRAM is a potential candidate to meet performance and power requirements at ultra-low V_{cc} SRAM applications.

4.4. TFET electrical noise modeling for circuit implementation

The high frequency white noise sources, such as the channel thermal noise and the shot noise, are detrimental to analog/RF applications. In [63], we developed transistor level Verilog-A based electrical noise models including flicker, shot and thermal noise for HTFET as compared to Si-FinFET for circuit-level analysis. Because the forward and reverse components of tunneling current across the tunnel junction, tunnel devices, in general, exhibit enhanced shot noise than MOSFETs, which is modeled by a Fano Factor $F = 2$ here for III–V HTFET [66,67]. Comparable thermal noise model can be assumed for HTFET and Si-FinFET, which is proportional to the channel conductance at zero V_{DS} [58,68]. The flicker noise for Si-FinFET is modeled as in [58], while III–V HTFET's flicker noise model is as discussed in Section 4.1. The overall input referred noise power (S_{VG}) is presented in Fig. 19 comparing HTFET and Si-FinFET. At low frequency $f = 100$ kHz, where the flicker noise dominates, 1.5 times reduction of the input referred noise is observed in HTFET over Si-FinFET due to the improved intrinsic gain

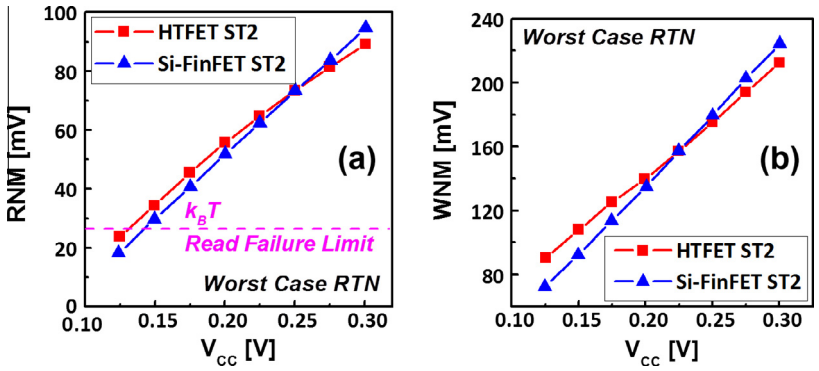


Fig. 17. (a) RNM and percentage of RNM variation (b) WNM and percentage of WNM variation with V_{cc} scaling. HTFET 10T ST2 SRAM shows less variation with V_{cc} scaling in the presence of RTN.

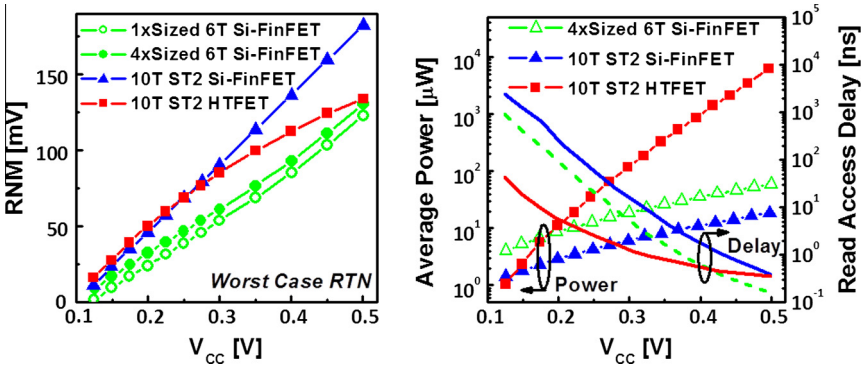


Fig. 18. (a) RNM of 10T ST2 SRAM compared against 6T SRAM (b) Average power consumption of 256 × 256 SRAM array with 5% activity factor. Read-access delay is also shown.

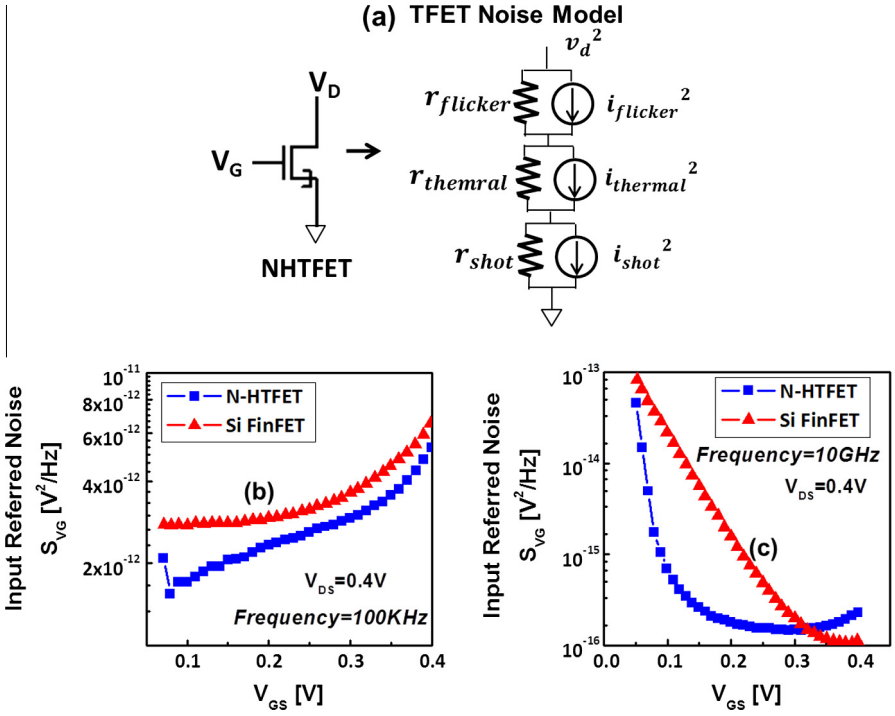
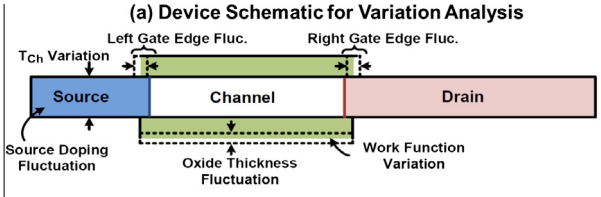


Fig. 19. (a) Representation of flicker, shot and thermal electrical noise models (noise current sources) implemented at transistor level. Input referred noise power comparison for HTFET and Si-FinFET (b) 100 kHz, (c) 10 GHz at $L_g = 20$ nm.



(b) Sources of Variations for TCAD Simulation

Variation N(μ,σ)	μ	3σ
Channel Thickness, t_{ch} [nm]	5	0.5
Oxide Thickness, t_{ox} [nm]	2.5	0.3
HTFET Source Doping cm^{-3}	$4.5x10^{19}$	$5x10^{18}$
HTFET Gate Workfunction, WF [eV]	4.85	0.005
Si FinFET Gate Workfunciton, WF [eV]	4.48	0.005
Left Gate Edge to Channel Center [nm]	-20	2
Right Gate Edge to Channel Center [nm]	+20	2

Fig. 20. (a) Illustration of III–V HTFET variation model (b) sources of variations for III–V TCAD Simulation.

from the steep switching. At high frequency $f = 10$ GHz, shot noise increases for TFET, causing the input referred noise of TFET to exceed the sub-threshold Si-FinFET.

Our evaluation on flicker, shot and thermal noise of HTFET reveals that at a nominal operation voltage of 0.3 V, HTFET exhibits competitive input referred noise as compared to Si-FinFET in kHz and MHz frequency range, which meets the bandwidth requirement of ultra-low voltage sensor application. At operating voltage exceeding 0.3 V with frequency range of 10 GHz and higher (RF domain), however, the HTFET input referred noise increases moderately due to the presence of shot noise. The transistor-level Verilog-A model can be further implemented to the circuit-level noise simulation.

5. Variation impact on TFET performance

The impact of process variation on transistor performance is increasingly important for both high performance computing using highly scaled transistors [69], and energy efficient applications using near-/sub-threshold CMOS [70]. Due to the exponential dependence of the I_{on} on the tunneling-barrier width, variation sources that can alter the tunneling-barrier width can cause a significant I_{on} fluctuation in TFET ([15,18]). In this section, we focus on the device-level variation modeling for TFET and its impact on TFET SRAM noise margin for low voltage application.

5.1. TFET Variation modeling

We studied the variation sources using a L_g of 40 nm, double-gate ultra-thin-body (UTB) HTFET ([15]) including fluctuations in source doping, oxide thickness (T_{ox}), gate-contact work function (WF), left/right gate edge overlap, body thickness (T_b) (Fig. 20). In this model, we assume (1) only small fluctuation occurs, and (2) each source is independent, where the correlations between the sources are omitted. The analytical expression of on-current variance σI_{on}^2 is as:

$$\sigma I_{on}^2 = \left(\frac{\delta I_{on}}{\delta T_b}\right)^2 + \left(\frac{\delta I_{on}}{\delta T_{ox}}\right)^2 + \left(\frac{\delta I_{on}}{\delta WF}\right)^2 + \cdots$$

To validate the analytical model, we simulated 2000 samples of Si-FinFET and HTFET devices using Monte Carlo simulation in TCAD Sentaurus, assuming independent Gaussian distributions for each source of variation. The results show good agreement with the analytical model. Fig. 21a and b shows a break-down of the contribution of various sources of variations to the total variance comparing HTFET and Si-FinFET. The contribution from gate-source overlap fluctuation is dominated for $V_{DD} > 0.5$ V, due to the depletion induced tunnel-barrier width change. For

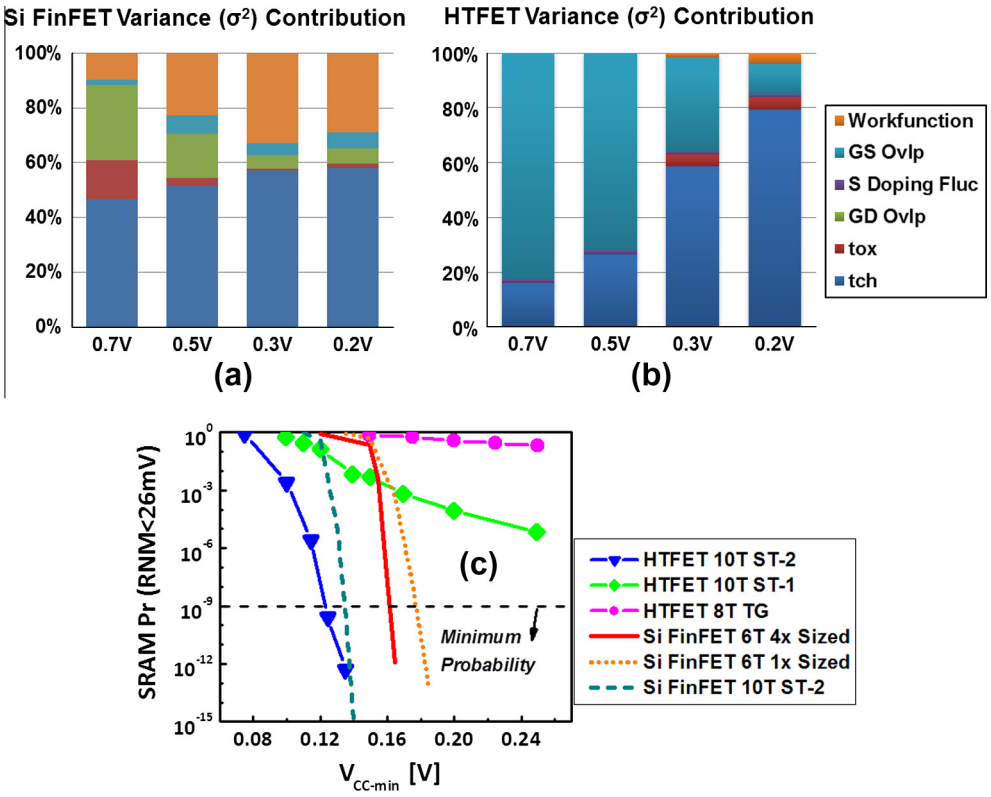


Fig. 21. Contribution of variance components in (a) Si FinFET and (b) HTFET due to various sources of variation at different V_{CC}. (c) Probability of read-upset for various Si FinFET and HTFET SRAM configuration.

$V_{DD} < 0.3$ V, T_b variation begins to dominate for both HTFET and Si-FinFET, due to the quantum confinement effect induced effective band-gap variation and causing tunneling barrier width fluctuation in HTFET. Recent work in [18] shows workfunction fluctuation dominates the performance variation of III–V nanowire HTFET at $L_g = 13$ nm, due to the increased workfunction variation (±83 mV) in highly scaled technology node.

5.2. Variation impact on low voltage TFET SRAM design

Given the variation coefficients obtained from the validated analytical model, we extend the look-up table based Verilog-A model to perform the circuit-level Monte-Carlo simulation for SRAM including all possible sources of variation. 1000 Monte-Carlo samples are generated for various CMOS and TFET SRAM designs to estimate the mean and sigma of the noise margins at different V_{DD}. Fig. 21c plots the read-upset probability as a function of V_{DD} for different configurations of SRAM cells. CMOS ST2 SRAM and HTFET ST2 SRAM exhibit comparable best read V_{cc-min} of 134 mV and 124 mV, respectively, due to the improved variation tolerance from the feedback. At its V_{cc-min}, the HTFET ST2 SRAM provides more energy efficiency benefit with 1.2 times lower dynamic energy, and 13 times lower leakage power consumption compared to the CMOS ST2 SRAM.

6. Conclusions

In this review paper, we have explored the TFET device design, application space, and the impact of the reliability issues on TFET device and circuit performance for energy efficient computing. In order to bridge the emerging device design and the circuit implementation, a device-circuit co-design framework by employing the look-up table-based Verilog-A model has been developed for TFET performance benchmarking, circuit implementation and reliability analysis. Compared to Si-FinFET technology, HTFET based logic circuits exhibit improved energy efficiency for below 0.5 V operation due to the steep slope at low V_{DD}. Desired read/write noise margin and improved energy efficiency can be achieved in higher transistor-count TFET SRAMs (e.g. ST2 topology), compared to the sub-threshold Si-FinFET designs. III–V HTFET based RF rectifier also shows improved sensitivity and desired power conversion efficiency at low RF input power for energy scavenging applications. Despite of the low voltage operation, III–V HTFET exhibits superior radiation resilience and favorable performance compared to Si-FinFET technology, with the presence of electrical noise and process variation. Soft-error analysis shows significant improved radiation resilience of III–V TFET based circuits compared to both Si and III–V FinFET based circuits over the voltage range from 0.3 V to 0.6 V, which comes from the bipolar gain reduction, the on-state enhanced Miller capacitance effect and the improved latching window masking with on-current improvement at low V_{DD}. Analytical models of electrical noise and process variation have been developed for III–V HTFET, which further enables the circuit-level evaluation of the noise and variation induced performance degradation for both digital and analog/mix-signal applications.

Acknowledgement

The authors would like to thank Bijesh Rajamohanan, Rahul Pandey, Matthew Cotter, Vinay Saripalli, Dheeraj Mohata for their contributions to this work. This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of the six SRC STARnet Centers, sponsored by MARCO and DARPA, and was also supported in part by the National Science Foundation (NSF) ASSIST ERC 1160483, Intel ARO and DTRA.

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