Layout-Dependent Strain Optimization for p-Channel Trigate Transistors

Salil Mujumdar, Kingsuk Maitra, and Suman Datta, *Senior Member, IEEE*

***Abstract*—In this paper, we investigate the optimization of device layout and embedded source/drain (eS/D) shape profile for strain engineered 22-nm node Si and SiGe p-channel trigate field-effect transistors by finite-element method simulations. A nested trigate layout with dummy gates is found to retain the maximum channel stress for all three conduction planes. The tradeoff between achievable mobility enhancement and active device density for the nested trigate layout is also investigated in this paper. Next, the impact of the eS/D shape on the channel stress for all three conduction planes is studied, and the rounded eS/D shape is found to be the optimal shape contrary to the planar case with sigma-shaped eS/D. Finally, strained SiGe channel trigate transistors are investigated as a potential candidate for future technology nodes. The evolution of formation and relaxation of the average strain of the compressively strained SiGe channel is systematically studied as a function of fin formation, embedded S/D formation, and layout configuration.**

***Index Terms*—Embedded source/drain (S/D), fin nesting, gate nesting, p-channel, Si, SiGe, trigate, uniaxial strain.**

I. Introduction

STRAIN has been a key technique responsible for planar CMOS performance enhancement for over a decade [1]. The focus has shifted from biaxial to uniaxial strain over the years given the greater advantages of uniaxial strain, particularly for enhancement of hole transport [1]. Uniaxial strain along the $\langle 110 \rangle$ direction provides a much larger mobility enhancement $(\Delta\mu/\mu\%)$ and a smaller V_t shift compared with biaxial strain [1], which is critical for further scaling of the MOS technology. p-channel MOS (pMOS) shows a greater enhancement factor than nMOS with strain [2], thus translating to a more balanced performance suitable for complementary technology. The channel orientations of interest for strained pMOSFETs are: 1) the (100)/$\langle 110 \rangle$ channel due to its high mobility enhancement factor; and 2) the (110)/$\langle 110 \rangle$ channel due to its inherently higher hole mobility than the (100)/$\langle 110 \rangle$ channel [2], [3]. Embedded SiGe source–drain and compressive contact etch stop layers (cCESLs) [4], [5] are the dominant techniques for inducing strain in strain engineered pMOSFETs.

Manuscript received July 22, 2011; revised September 6, 2011; accepted October 4, 2011. Date of publication November 2, 2011; date of current version December 23, 2011. The review of this paper was arranged by Editor D. Esseni.

S. Mujumdar and S. Datta are with the Department of Electrical Engineering, The Pennsylvania State University, University Park, PA 16802 USA (e-mail: sum231@psu.edu; sdatta@engr.psu.edu).

K. Maitra is with GLOBALFOUNDRIES, Albany, NY 12084 USA (e-mail: kingsuk.maitra@globalfoundries.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2171968

Trigate transistors are considered to be the lead contenders for replacing planar CMOS for future technology nodes [6]–[8]. In addition, recently, high-Ge-content SiGe and pure Ge channels have been recognized as attractive alternatives to Si for future high-performance pMOS devices due to higher unstrained hole mobility values and enhancement factors [2], [9]. Strain engineered Si/SiGe/Ge p-channel trigate FET is thus a topic of significant interest. Uniaxial strain in p-channel trigate FETs is achieved either by embedding larger lattice constant materials (e.g., Si_xGe_{1-x}) as source/drain (S/D) stressor regions [10] or by patterning biaxially strained epitaxial layers or by cCESL [11], [12]. In the former case, there is always a possibility of strain relaxation of the embedded (eS/D) regions through their free surfaces due to the absence of shallow trench isolation (STI). In the latter case, ion-implantation-induced S/D amorphization can relax the channel strain almost completely for extremely scaled gate lengths [13]. A nested device layout, which is a common strategy in the physical design of circuits [14], has to be adopted to minimize S/D relaxation associated with free surfaces of the eS/D regions and thus maximize the channel strain. Thus, the average uniaxial strain retention for top plane and sidewall in p-channel trigate FETs will depend on the following factors: 1) the average distance between the source and the drain $L_{S/D}$; 2) the eS/D Ge content; 3) the number of nested gates; 4) the number of nested fins; 5) the shape of the eS/D regions; 6) the eS/D etch depth; 7) the channel Ge content; 8) the residual strain due to patterning biaxial strained epitaxial layers retained and after S/D recess etch; and 9) the gate pitch. In this paper, we systematically study the contribution of all the above factors to the average channel stress except the effect of gate pitch, which is kept constant for all cases. Average stress values and mobility enhancements for (100) and (110) planes are separately calculated keeping in mind the anisotropic behavior of these quantities, thus giving a more realistic estimate of achievable enhancement.

II. Simulation Methodology

Finite-element method (FEM) simulations are performed using COMSOL Multiphysics [15]. For benchmarking the FEM simulations, device structures with dimensions, substrate/channel, and eS/D compositions identical to those in [16] were simulated and the extracted stress S_{XX} values along the channel length (transport direction) were compared with the corresponding experimental values. A linear elastic model with orthotropic channel behavior was implemented in order to realistically estimate achievable levels of channel stress. The elastic moduli, shear moduli, and Poisson's ratios of Si

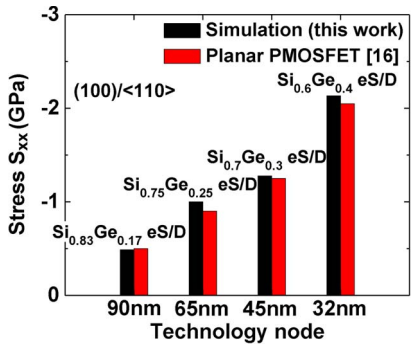

Fig. 1. FEM simulations benchmarked for compressively strained planar pMOSFETs. The simulated device dimensions are identical to those in [16] for which the corresponding channel measurements are taken. The simulations are done assuming only the eS/D regions as the stressor sources.

and germanium for (100)/⟨110⟩ and (110)/⟨110⟩ were obtained from [17], and the elastic moduli, shear moduli, and Poisson's ratios for $Si_{1-x}Ge_x$ alloys were obtained by a linear interpolation between those for Si and germanium. The lattice constant for $Si_{1-x}Ge_x$ was calculated from Vegard's law. The thermal expansion coefficient of the eS/D regions was modified to incorporate the eS/D to channel lattice mismatch that is responsible for introducing uniaxial compressive strain in the channel. No other stressor sources, except the eS/D regions, were assumed in this paper. The channel stress values extracted from the simulations show good agreement between the simulated and experimental values, as shown in Fig. 1, thus validating the choice of the elastic model and values of elastic moduli/Poisson's ratios used, as well as the assumption of the eS/D regions being the dominant stressor sources in experimentally reported values.

Figs. 2 and 3 show the trigate structures simulated for evaluating the contribution of various factors to the channel stress of p-channel trigate FETs. A relaxed Si substrate is assumed for p-channel Si trigate FETs, whereas a relaxed $Si_{0.4}Ge_{0.6}$ virtual substrate is assumed for the $Si_{0.4}Ge_{0.6}$ channels. The top surface is the (100) plane with the sidewall being the (110) plane for all the device structures investigated. The channel direction is ⟨110⟩ for all cases. Average stress and corresponding mobility enhancements for top surface (100) and sidewalls (110) are extracted only for the central channel (red). An inversion layer thickness $t_{\rm inv}$ of 2 nm for both (100) and (110) planes is assumed for the calculation of average surface channel stress for all the structures simulated. The surfaces are assumed to be traction free for all cases. A nonuniform mesh with fine meshing, particularly near heterointerfaces such as eS/D and channel interface regions and relatively coarser meshing farther away from heterointerfaces, ensuring that further mesh refinement does not alter the simulated stress levels, is chosen to accurately estimate strain levels in regions with rapidly changing strain levels and to reduce the overall mesh points to reduce the computation time. For evaluating the contribution of 2) S/D Ge content, 3) number of gates, and 4) number of fins to the average channel stress, the trigate structures in Fig. 2 are also simulated with three different eS/D Ge contents (i.e., 25%, 30%, and 40%).

It is evident that the current transport in trigate FETs is increasingly dominated by the sidewalls as we reduce the fin width. Engineering the sidewall surface channel stress and hole mobility is thus of prime importance for future technology nodes and would need careful consideration of the eS/D shape profiles. The trigate structures in Fig. 3 ($Si/Si_{0.4}Ge_{0.6}$ channels with $Si_{0.6}Ge_{0.4}/Ge$ eS/D regions, respectively) are studied to evaluate the effect of 5) S/D shape and 6) channel Ge content on the average channel stress and corresponding mobility enhancement. The contribution of etch depth is studied for the sidewalls of the nested gate (four dummy gates) structure due to the sidewall-dominated transport in trigate FETs as aforementioned. The eS/D etch depth was reduced by 10 nm with the other dimensions, as well as the channel and eS/D compositions remaining the same.

Further improvement in the channel stress achieved through a combination of global + eS/D techniques is of prime interest. The evolution of the channel stress, similar to the approach in [18], following fin patterning, S/D recess etch, and eS/D regrowth for uniaxially strained $Si_{1-x}Ge_x$ epilayers is investigated with three different channel Ge contents for the structure in Fig. 2(d). The substrate is assumed to be a Si substrate with isotropic behavior.

The mobility enhancement of strained Si channels over unstrained Si channels is obtained from the hole mobility versus channel stress plot for Si given in [2]. The mobility enhancements for strained $Si_{1-x}Ge_x$ (110)/⟨110⟩ channels over unstrained $Si_{1-x}Ge_x$ (110)/⟨110⟩ channels are obtained by a linear interpolation between the enhancements for Si (110)/⟨110⟩ channels [2] and Ge (110)/⟨110⟩ channels [19], whereas the mobility enhancement for SiGe (100)/⟨110⟩ channels is taken from the SiGe (100)/⟨110⟩ channel hole mobility versus channel stress plot given in [2]. In addition, as the mobility versus channel stress plots in [2] and [19] have been obtained using band structure calculations instead of relying on piezoresistive coefficients, they predict a realistic estimate of the achievable mobility enhancements.

III. Results and Discussion

The stress-inducing mechanism of the eS/D, the shape of the eS/D regions, and the presence of free surfaces result in a varying stress profile along the channel length, as shown in Fig. 4. Hence, an average stress needs to be extracted for both the (100)/⟨110⟩ and the (110)/⟨110⟩ channels to estimate the achievable mobility enhancement. The average stress is taken as the average value of the stress profiles for the respective conduction planes, where the stress profiles are obtained for a channel depth of 2 nm into the fin. Fig. 5(a) shows the average stress values for the (100)/⟨110⟩ channel of the trigate structures in Fig. 2 for three different Ge contents in the eS/D regions. The channel stress for the planar pMOSFET case with the corresponding eS/D Ge contents [16] is also shown for comparison. The percentage reduction in the average channel stress compared to the planar case is shown in the inset in Fig. 5(a). The stress degradation for the 40% eS/D Ge content is of interest due to the significantly higher channel stress levels for both the planar and nonplanar cases, as shown in

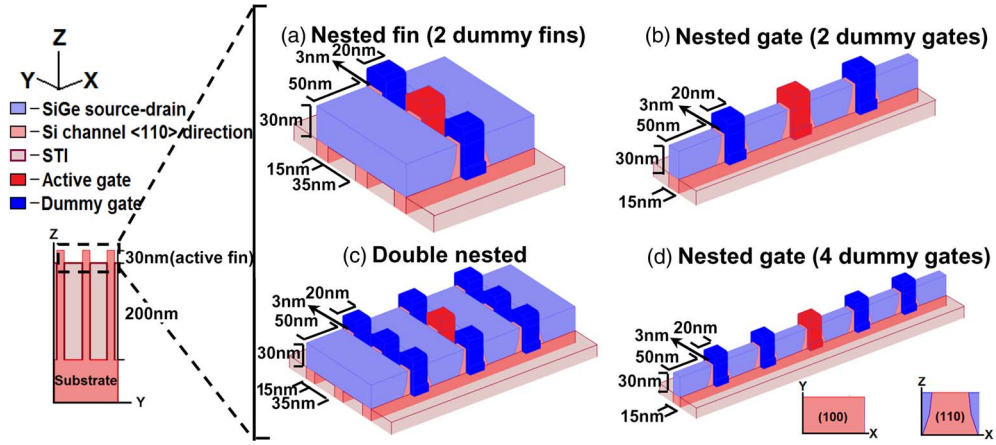

Fig. 2. Schematics of the simulation structures for evaluating the contribution of $L_{S/D}$, eS/D Ge content, number of nested gates, number of nested fins, and eS/D etch depth to the average channel stress. The average channel stress is calculated only for (red) the active gate.

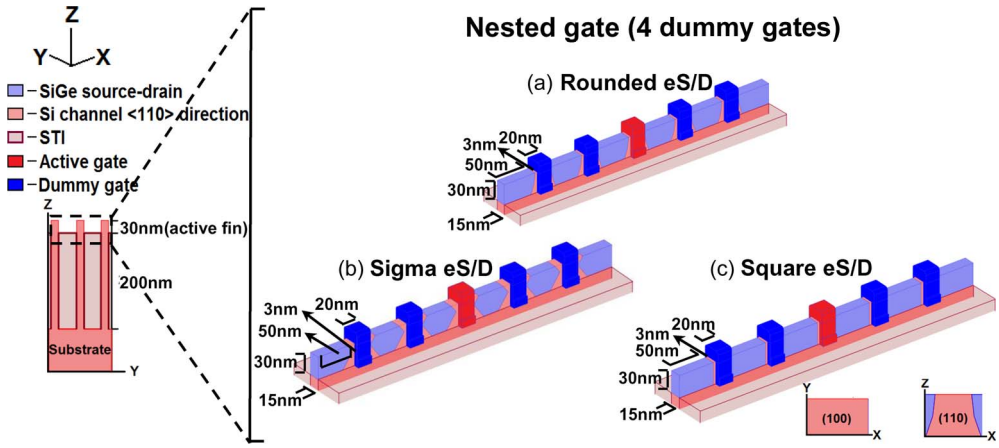

Fig. 3. Schematics of the simulation structures for evaluating the contribution of eS/D shape and channel Ge content to the average channel stress keeping the same lattice mismatch between the channel and eS/D regions. The average channel stress is calculated only for (red) the active gate.

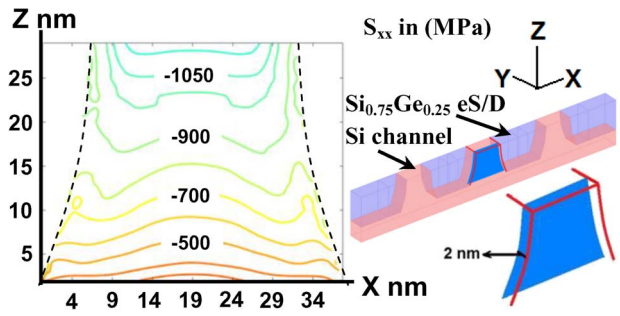

Fig. 4. Sidewall [(110)/⟨110⟩] stress profiles [S_{XX} (stress along channel length) in megapascals] for the nested gate (two dummy gates) structure (Si channel + $Si_{0.75}Ge_{0.25}$ eS/D.

Fig. 5(a). Therefore, the discussion henceforth will focus on the stress degradation for the trigate structures in Fig. 2 with 40% eS/D Ge content compared to the planar case (40% eS/D Ge content). The absence of STI causes significant reduction in the channel stress of the trigate structures compared to the planar case. The nested fin (two dummy fins) structure shows the highest average (100)/⟨110⟩ channel stress reduction indicating significant relaxation of the S/D regions through their free surfaces. The nested gate (two dummy gates) structure shows an ∼23% reduction in the average channel stress for the (100)/⟨110⟩ channel orientation, stressing the importance of gate nesting in improving the channel stress. The double-nested structure displays an even higher average (100)/⟨110⟩ channel stress. The free eS/D sidewalls (parallel to the channel length) of the nested gate (two dummy gates) are eliminated in the double-nested structure after merging the eS/D regions, resulting in increased average (100)/⟨110⟩ channel stress for the double-nested structure.

The nested gate (four dummy gates) structure shows least degradation in the (100)/⟨110⟩ channel stress compared to the planar case among all four trigate structures. The nested gate (four dummy gates) structure also features a smaller number of dummy gates compared with the double-nested structure, as shown in Fig. 2, implying that gate nesting is the optimal strategy for maximizing the average (100)/⟨110⟩ channel stress.

Fig. 5(a) also shows the improvement in the average channel stress with increasing eS/D Ge content. The average stress for the (100)/⟨110⟩ channel shows a significant enhancement of ∼1.6× on increasing the S/D Ge content from 25% to 40% for all the structures. It can be concluded that elimination of the free sidewalls (normal to the channel length) of the eS/D regions, achieved by nesting dummy gates, is crucial to obtain acceptable levels of stress for the (100)/⟨110⟩ channel.

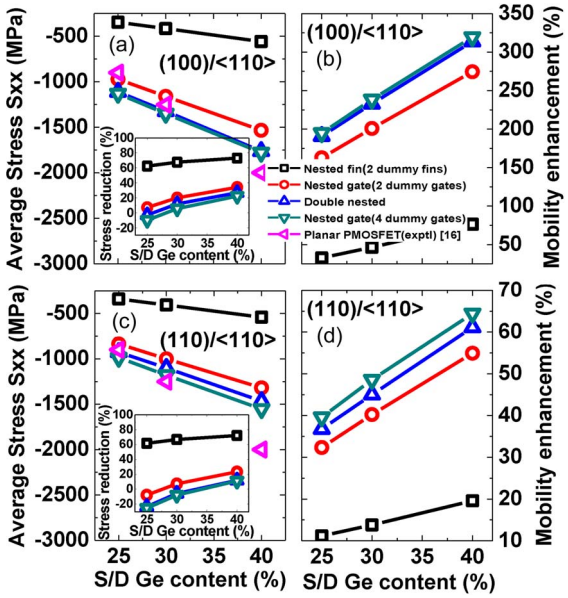

Fig. 5. Average channel stress and corresponding mobility enhancement plots for the (100)/⟨110⟩ and (110)/⟨110⟩ channels of the structures in Fig. 2(a)–(d). Mobility enhancements are obtained from the hole mobility versus stress plots in [2]. The solid lines are drawn to serve as a guide.

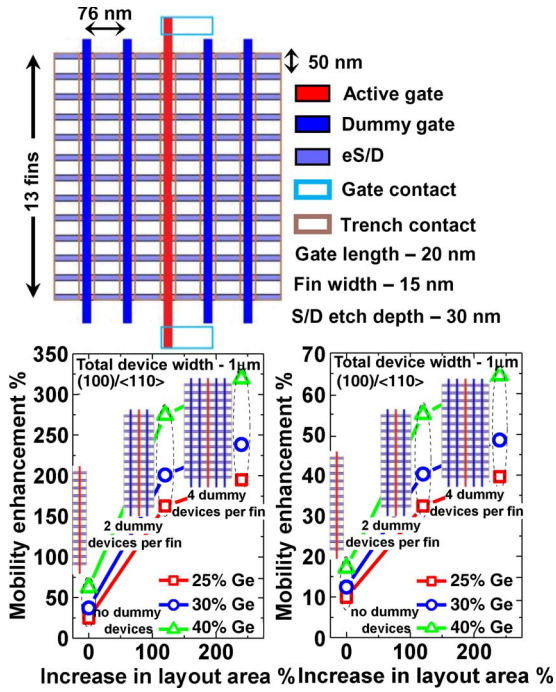

Fig. 6. Top surface and sidewall channel mobility enhancements versus increase in the layout area for a total active device width of 1 μm for Si with different eS/D germanium contents.

Fig. 5(b) plots the (100)/⟨110⟩ channel mobility enhancement for the corresponding average stress values in Fig. 5(a). The nested gate (four dummy gates) shows the highest mobility enhancement corresponding to the highest channel stress among all the trigate structures considered.

Fig. 5(c) plots the average (110)/⟨110⟩ channel stress values for the trigate structures in Fig. 2 with three different eS/D Ge contents. The extracted average channel stress values are again compared to the planar case [16], and the percentage reduction in the average channel stress is plotted in the inset in Fig. 5(c). The average (110)/⟨110⟩ channel stress values display a similar trend to the (100)/⟨110⟩ channel stress levels shown in Fig. 5(a). The nested gate (four dummy gates) shows least reduction in the average channel stress compared to the planar case [16], which again shows that the nested gate (four dummy gates) is the best structure. The (110)/⟨110⟩ channel, similar to the (100)/⟨110⟩ channel, shows a $\sim$1.6$\times$ enhancement in the average channel stress when the eS/D Ge content is increased from 25% to 40% for all the trigate structures.

It is evident that the average (110)/⟨110⟩ channel stress is smaller than the average (100)/⟨110⟩ channel stress for all the trigate structures due to increased $L_{S/D}$ for the sidewalls as opposed to the top surface.

Fig. 5(d) gives the (110)/⟨110⟩ channel mobility enhancement for the corresponding average stress values in Fig. 5(c). Although the mobility enhancement for the (110)/⟨110⟩ channel is smaller than that for the (100)/⟨110⟩ channel, the (110)/⟨110⟩ sidewall channel, due to its higher unstrained mobility, offers an advantage over the (100)/⟨110⟩ top surface channel [2] ensuring the viability of implementing the (110)/⟨110⟩ orientation for sidewall channels.

The average (110)/⟨110⟩ channel stress for the 20-nm eS/D etch depth nested gate (four dummy gates) structure is $\sim$ 0.97$\times$ of the (110)/⟨110⟩ channel stress for the 30-nm S/D etch depth nested gate (four dummy gates) structure, confirming the role of increased etch depth in improving the channel stress. The improvement in the channel stress due to increase in the eS/D etch depth serves as an important addition to the increase in the current of the unstrained device due to increased effective width.

It is clear from the above discussion that the nested gate layout is the optimal layout strategy for achieving maximum surface channel stress for both the top surface and sidewall planes.

Although gate nesting offers significant improvement in the channel stress for both the top surface and sidewall conduction planes, the reduction in the active device density with increasing number of dummy gates poses a critical problem of reduced functionality per unit chip area. An optimum tradeoff in the achievable mobility enhancement with an acceptable reduction in the active device density needs to be devised for successfully implementing the nested gate layout strategy. Fig. 6 plots the achievable mobility enhancement versus the increase in the layout area considering an effective active device width of 1 μm for the single-gate finger, three-gate finger, and five-gate finger trigate structures. It is evident that the tradeoff between the active chip area and the mobility enhancement will depend on the active device density constraint. For a relatively relaxed active device density constraint, the nested gate (two dummy gates) layout is optimal, featuring a significant mobility enhancement for the (100)/⟨110⟩ and (110)/⟨110⟩ channels. Although the five-gate finger layout features an unacceptable reduction in the active device density, the two devices in the immediate left and right of the central trigate FET can be activated, thus alleviating the problem of reduced active device density. The activated devices, however, will not display the same mobility

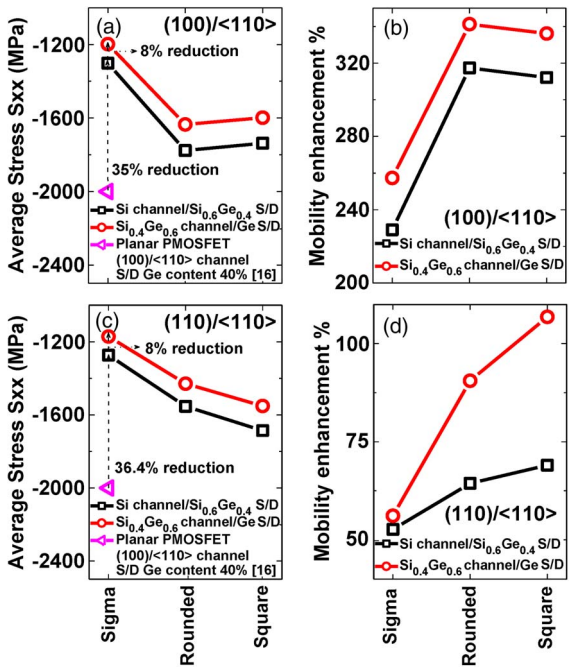

Fig. 7. Average sidewall (100)/⟨110⟩ and (110)/⟨110⟩ channel stress and corresponding mobility enhancement plots for the structures in Fig. 3(a)–(c). Mobility enhancement for the (100)/⟨110⟩ channel is obtained from the mobility versus stress plots in [2], whereas the mobility enhancement for the (110)/⟨110⟩ channel is calculated by a linear interpolation between those for Si [2] and for Ge [19]. The solid lines are drawn to serve as a guide.

enhancement as the central trigate due to degraded channel stress levels for all three conduction planes. Hence, careful device design has to be done in order to overcome the problems posed by dissimilar performance levels of active devices in the nested gate layout. A similar argument can be made for the seven-gate finger layout and so on.

Engineering the eS/D shape profile for maximizing the sidewall channel stress is critically important as aforementioned. Fig. 7(a) plots the average (100)/⟨110⟩ channel stress values for the nested gate (four dummy gates) structure with different eS/D profiles, as shown in Fig. 3. The average (100)/⟨110⟩ channel stress for the $Si/Si_{0.4}Ge_{0.6}$ channel with $Si_{0.6}Ge_{0.4}$/Ge sigma eS/D shows significant reduction compared to the planar case [16]. The (100)/⟨110⟩ Si channel with the rounded and square $Si_{0.6}Ge_{0.4}$ eS/D displays a stress reduction of ∼11.1% from the planar case, whereas the $Si_{0.4}Ge_{0.6}$ channel with the rounded and square Ge eS/D shape profiles shows further stress reduction of ∼8% from the strained Si (100)/⟨110⟩ channel. $L_{S/D}$, being the same for the (100)/⟨110⟩ channel for both rounded and square eS/D cases, the (100)/⟨110⟩ channel shows similar channel stress degradation compared to the planar case [16].

Hence, the rounded/square eS/D shape profiles featuring smaller $L_{S/D}$ are optimal for the introduction of maximum stress for the (100)/⟨110⟩ channel for both the Si and SiGe channels. The stress levels for the $Si_{0.4}Ge_{0.6}$ channel are ∼0.92× of the values for the corresponding Si channel in Fig. 3(a)–(c) for the same lattice mismatch between the channel and S/D regions due to the smaller elastic moduli and Poisson's ratios of $Si_{0.4}Ge_{0.6}$ compared to Si [17].

Fig. 7(b) plots the mobility enhancement for the strained (100)/⟨110⟩ Si and $Si_{0.4}Ge_{0.6}$ channels. It is evident that the $Si_{0.4}Ge_{0.6}$ channel outperforms the Si channel in spite of its smaller average (100)/⟨110⟩ channel stress due to the higher mobility enhancement factor featured by the $Si_{0.4}Ge_{0.6}$ channel [2]. The $Si_{0.4}Ge_{0.6}$ channel also features a higher unstrained (100)/⟨110⟩ hole mobility value than Si [2], thus providing a significant advantage over the strained Si channel.

Fig. 7(c) plots the average channel stress for the (110)/⟨110⟩ sidewall. The average (110)/⟨110⟩ channel stress for $Si/Si_{0.4}Ge_{0.6}$ with $Si_{0.6}Ge_{0.4}$/Ge sigma eS/D again shows significant reduction compared to the planar case [16]. The (110)/⟨110⟩ Si channel with the rounded and square $Si_{0.6}Ge_{0.4}$ eS/D cases shows a 22.4% and 15.7% reduction, respectively, in the average stress compared to the planar case [16], whereas the $Si_{0.4}Ge_{0.6}$ channel stress shows further reduction of ∼8% from the Si channel for the rounded and square Ge eS/D cases. The square S/D nested gate (four dummy gates) structure has the least $L_{S/D}$ for the (110)/⟨110⟩ sidewall compared to the other two eS/D profiles resulting in maximum (110)/⟨110⟩ channel stress among all three structures.

The corresponding mobility enhancement for the (110)/⟨110⟩ sidewall for both Si and $Si_{0.4}Ge_{0.6}$ channels is plotted in Fig. 7(d). The $Si_{0.4}Ge_{0.6}$ channel offers a higher mobility enhancement than Si for the (110)/⟨110⟩ channel also in spite of its lower average stress levels. Along with the higher mobility enhancement factor, the SiGe channels also possess an inherently higher unstrained hole mobility value compared to Si for the (110)/⟨110⟩ channel [2], thus clearly demonstrating the advantage of implementing strained SiGe/Ge channels for future technology nodes.

Thus, the sigma-shaped eS/D shows significant degradation in the average (100)/⟨110⟩ and (110)/⟨110⟩ channel stress resulting in degraded mobility enhancements due to a larger $L_{S/D}$ compared to the rounded and square eS/D structures, and hence, it is not a viable option for trigate FETs as opposed for strained planar pMOSFETs [20]. Although, from the above discussion, the square-shaped eS/D is seen to be the best option for achieving maximum channel stress for all three conduction planes, the rounded eS/D has to be adopted due to the square-shaped eS/D being impractical to implement.

Fig. 8(a)–(d) plots the stress profile evolution following biaxially strained $Si_{0.75}Ge_{0.25}$ epitaxial growth on Si, fin patterning, S/D recess etch, and eS/D (1.7% mismatch) regrowth, respectively. The biaxially strained epilayer features minimum stress relaxation/stress profile variation due to the absence of traction free surfaces, as shown in Fig. 8(a). Fin patterning, however, results in stress reduction and a larger stress profile variation compared to the biaxially strained layer, as is evident in Fig. 8(b), due to the creation of free surfaces. Variation in the stress profile will depend on the dimensions and, particularly, the length of the fin. The smaller the length, the greater the variation in the stress profile. The S/D recess etch further relaxes the residual stress of the fin in Fig. 8(b) almost completely due to the creation of free surfaces next to the channel, as shown in Fig. 8(c). The residual stress profile in Fig. 8(c) shows maximum compressive stress at the bottom of the sidewall and least compressive stress at the topmost part of the sidewall, i.e.,

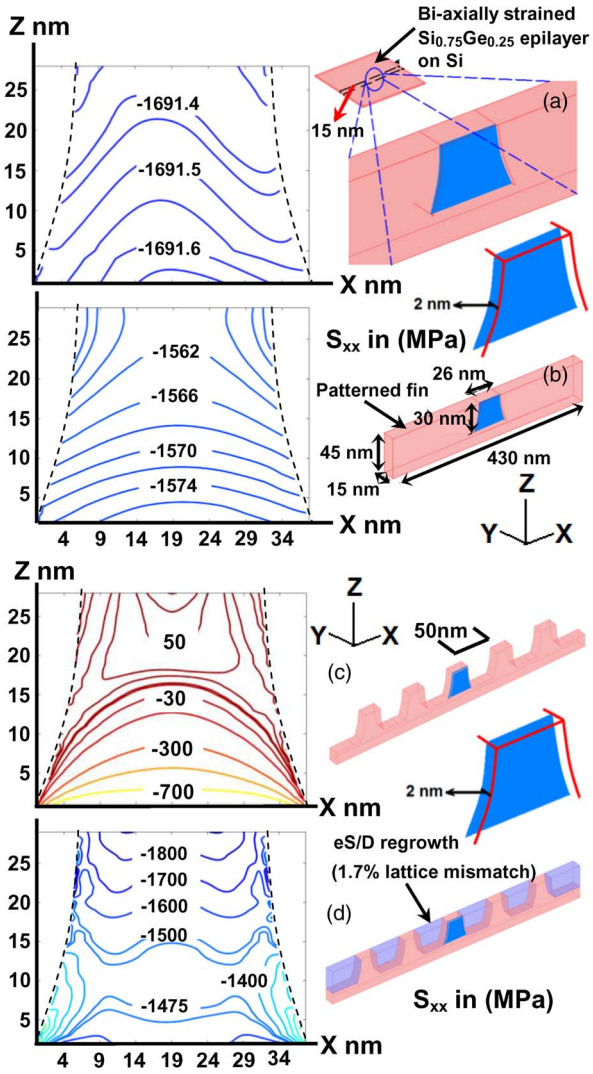

Fig. 8. (a) and (b) Stress evolution following biaxially strained $Si_{0.75}Ge_{0.25}$ epitaxial layer growth and fin patterning. (c) and (d) Stress relaxation after S/D recess etch and stress recovery after eS/D regrowth.

a trend reverse to that for the eS/D case, as shown in Fig. 4. The global + eS/D combination hence displays a more uniform sidewall channel stress profile, as shown in Fig. 8(d), translating to minimal V_t variation along the sidewall, thus offering an advantage over the eS/D technique.

Fig. 9(a) plots the average stress for a combination of the residual stress and the 1.7% lattice mismatched eS/D induced stress for the $Si_{1-x}Ge_x$ channels with three different channel Ge contents. As aforementioned, the Young's modulus of the SiGe channel decreases with increasing Ge content. This results in a decrease in the average channel stress for the same eS/D to channel lattice mismatch, as can be seen from the trend for the eS/D case (relaxed channel in the absence of eS/D). The (100)/⟨110⟩ channel stress for the global + eS/D combination is smaller than that for the eS/D case and shows a trend similar to the eS/D stressor case due to the residual stress becoming increasingly tensile for the (100)/⟨110⟩ channel with increasing Ge content. The (110)/⟨110⟩ channel stress for the global + eS/D combination, however, is higher than that for the

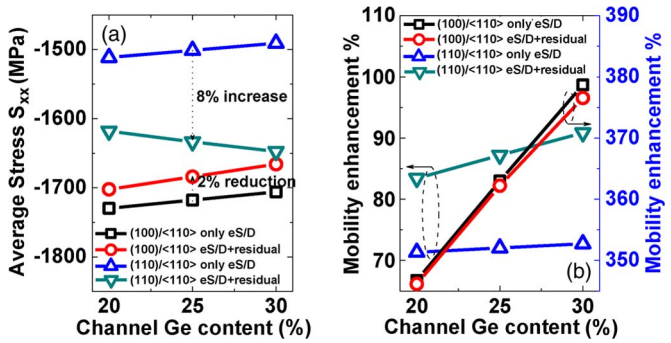

Fig. 9. (a) Average (100)/⟨110⟩ and (110)/⟨110⟩ channel stress with residual stress and eS/D stressors. (b) Mobility enhancements for the (100)/⟨110⟩ and (110)/⟨110⟩ channels with only eS/D stressors and a combination of eS/D induced and residual stress. The solid lines are drawn to serve as a guide.

eS/D case due to increasing compressive residual stress with increasing channel Ge content.

Fig. 9(b) plots the corresponding mobility enhancement for the (100)/⟨110⟩ and (110)/⟨110⟩ channels for the global + eS/D and the eS/D cases. The higher (110)/⟨110⟩ hole mobility enhancement for the global + eS/D combination ensures its viability in future technology nodes.

IV. Conclusion

We have thoroughly investigated and optimized the device layout and eS/D shape profiles of strain engineered p-channel trigate FETs. Nested gate layout is the optimal layout strategy displaying greater channel stress than the nested fin (two dummy fins) and double-nested structures. Increasing eS/D Ge content offers significant improvement in the channel stress. The rounded eS/D structure, due to its smaller $L_{S/D}$, displays significantly higher stress levels compared with the sigma eS/D structure for all conduction planes converse to the planar case. The eS/D technique, when combined with the nested gate layout strategy and the global stressor technique, demonstrates significant channel stress retention and a greater uniformity in the channel stress even for extremely scaled p-channel trigate FETs. The eS/D technique can be thus expected to continue to serve as an important addition to the conventional stressors for future p-channel trigate FETs.

References

[1] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 221–224.

[2] M. Chu, Y. Sun, U. Aghoram, and S. E. Thompson, "Strain: A solution for higher carrier mobility in nanoscale MOSFETs," *Annu. Rev. Mater. Res.*, vol. 39, pp. 203–229, 2009.

[3] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in n- and p-MOS inversion layers on (100), (110), and (111) Si," in *IEDM Tech. Dig.*, 2004, pp. 225–228.

[4] S. Ito, H. Namba, K. Yamaguchi, T. Hirata, and K. Ando, "Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design," in *IEDM Tech. Dig.*, 2000, pp. 247–250.

[5] S. Gannavaram, N. Pesovic, and M. C. Ozturk, "Low temperature (800 °C) recessed junction selective Si–germanium source/drain technology for sub-70 nm CMOS," in *IEDM Tech. Dig.*, 2000, pp. 437–440.

[6] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted Tri-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.

[7] N. Serra, F. Conzatti, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, S. Thomas, T. E. Whall, E. H. C. Parker, D. R. Leadley, L. Witters, A. Hikavyy, M. J. Hytch, F. Houdellier, E. Snoeck, T. J. Wang, W. C. Lee, G. Vellianitis, M. J. H. van Dal, B. Duriez, G. Doornbos, and R. J. P. Lander, "Experimental and physics-based modeling assessment of strain induced mobility enhancement in FinFETs," in *IEDM Tech. Dig.*, 2009, pp. 1–4.

[8] F. Conzatti, N. Serra, D. Esseni, M. D. Michielis, A. Paussa, P. Palestri, L. Selmi, S. M. Thomas, T. E. Whall, D. Leadley, E. H. C. Parker, L. Witters, M. J. Hytch, E. Snoeck, T. J. Wang, W. C. Lee, G. Doornbos, G. Vellianitis, M. J. H. van Dal, and R. J. P. Lander, "Investigation of strain engineering in FinFETs comprising experimental analysis and numerical simulations," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1583–1593, Jun. 2011.

[9] F. Conzatti, P. Toniutti, D. Esseni, P. Palestri, and L. Selmi, "Simulation study of the on-current improvements in Ge and sGe versus Si and sSi nano-MOSFETs," in *IEDM Tech. Dig.*, 2010, pp. 15.2.1–15.2.4.

[10] J. Kavalieros, B. S. Doyle, S. Datta, G. Dewey, and R. Chau, "Tri-gate transistor architecture with high-κ gate dielectrics, metal gates and strain engineering," in *VLSI Symp. Tech. Dig.*, Jun. 2006, pp. 62–63.

[11] T. Irisawa, T. Numata, T. Tezuka, K. Usuda, S. Nakaharai, N. Hirashata, N. Sugiyama, E. Toyoda, and S. Takagi, "High performance multi-gate pMOSFET using uniaxially-strained SGOI channels," in *IEDM Tech. Dig.*, 2005, pp. 709–712.

[12] K. Shin, C. O. Chui, and T. J. King, "Dual stress capping layer enhancement study for hybrid orientation FinFET CMOS technology," in *IEDM Tech. Dig.*, 2005, pp. 988–991.

[13] Z. Ren, K. L. Saenger, H. J. Hovel, J. P. De Souza, J. A. Ott, R. Zhang, S. W. Bedell, G. Pfeiffer, R. Bendernagel, V. Chan, D. K. Sadana, C. Y. Sung, M. Khare, M. Ieong, G. Shahidi, and H. Yin, "Uniaxial strain relaxation on ultra-thin strained-Si directly on insulator (SSDOI) substrates," in *Proc. 8th ICSICT*, pp. 136–138.

[14] M. Alioto, "Analysis and evolution of layout density of FinFET logic gates," in *Proc. ICM*, 2009, pp. 106–109.

[15] [Online]. Available: http://www.comsol.com/products/structural-mechanics/

[16] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S.-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, and S. Natarajan, "High performance 32nm logic technology featuring 2nd generation high-κ + metal gate transistors," in *IEDM Tech. Dig.*, 2009, pp. 1–4.

[17] J. J. Wortman and R. A. Evans, "Young's modulus, shear modulus, and Poisson's ratio in Si and Germanium," *J. Appl. Phys.*, vol. 36, no. 1, pp. 153–156, Jan. 1965.

[18] G. Eneman, G. Hellings, J. Mitard, L. Witters, S. Yamanguchi, M. Garcia Bardon, P. Christie, C. Ortolland, A. Hikavyy, P. Favia, M. Bargallo Gonzalez, E. Simoen, F. Crupi, M. Kobayashi, J. Franco, S. Takeoka, R. Krom, H. Bender, R. Loo, C. Claeys, K. De Meyer, and T. Hoffmann, " $Si_{1-x}Ge_x$-Channel PFETs: Scalability, layout considerations and compatibility with other stress techniques," *ECS Trans.*, vol. 35, no. 3, pp. 493–503, 2011.

[19] T. Krishnamohan, D. Kim, T. V. Dinh, A.-T. Pham, B. Meinerzhagen, C. Jungemann, and K. Saraswat, "Comparison of (001), (110) and (111) uniaxial- and biaxial- strained-Ge and strained-Si PMOS DGFETs for all channel orientations: Mobility enhancement, drive current, delay and off-state leakage," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[20] N. Tamura, Y. Shimamune, and H. Maekawa, "Embedded Si germanium (eSiGe) technologies for 45 nm nodes and beyond," in *Proc. IJWT*, 2008, pp. 73–77.

Salil Mujumdar received the M.S. degree in electronic science from the University of Pune, Pune, India, in 2008 and the M.S. degree in electrical engineering from The Pennsylvania State University, University Park, in 2011.

He is currently a Device Engineer with Intermolecular Inc., San Jose, CA. His research interests include strain engineering in trigate FETs, oxide/III–V interface characterization and modeling, and characterization and modeling of contacts to III–V quantum-well FETs.

Kingsuk Maitra received the M.S. degree in theoretical physics from the University of Kalyani, Kalyani, India, in 2000, the M.S. degree in microelectronics from the Indian Institute of Science, Bangalore, India, in 2002, the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 2005, and the M.B.A. in entrepreneurship and product design from Rensselaer Polytechnic Institute, Troy, NY, in 2011.

He is a member of the Technical Staff with GLOBALFOUNDRIES (formerly AMD) research team, Albany, NY, working on exploratory devices for advanced CMOS nodes (14 nm and beyond). He also spent a year at Intel development and three summers (2003–2005) at the IBM T.J. Watson Research Center, working on high-κ/metal gate stacks for advanced CMOS nodes. He is the author or coauthor of about 25 journal and conference articles, named as an inventor on 10 patents, and given multiple invited talks and tutorials. His research interests include transport phenomena in semiconductors, device/circuit cooptimization, and advanced process integration.

Dr. Maitra serves in the Technical Program Committees of multiple international conferences such as DRC, ISQED, and CICC.

Suman Datta (SM'06) received the Bachelor's degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1995 and the Ph.D. degree in electrical and computer engineering from the University of Cincinnati, Cincinnati, OH, in 1999.

Currently, he is a Professor of electrical engineering with The Pennsylvania State University, University Park. From 1999 to 2007, as a member of the Logic Technology Development Group, Intel Corporation, he was instrumental in the demonstration of indium–antimonide-based quantum-well transistors operating at room temperature with a record energy-delay product, the first experimental demonstration of metal gate plasmon screening and channel strain engineering in high-κ/metal gate CMOS transistors, and the investigation of the transport properties in nonplanar "trigate transistors. In 2007, he joined The Pennsylvania State University as the Joseph Monkowski Associate Professor of Electrical Engineering. His group is exploring new materials and novel device architecture for CMOS "enhancement" and "replacement" for future energy-efficient computing applications. He is the holder of more than 130 U.S. patents.

Dr. Datta is a Distinguished Lecturer of the IEEE Electron Devices Society.