Electrical Noise in Heterojunction Interband Tunnel FETs

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***Abstract*— We present an analysis of electrical noise in III–V heterojunction TFET (HTFET). Using numerical simulations, random telegraph noise (RTN) amplitude induced by a single charge trap is investigated with regard to trap location, electron band-to-band-generation rate, bias, and transistor size. It is found that HTFET RTN amplitude does not scale inversely with gate length and is governed by tunneling distance of carriers at source-channel junction. HTFET exhibits 40% less relative RTN amplitude at 0.3 V at gate lengths around 20 nm, over subthreshold Si-FinFET. RTN of HTFET at $V_{GS} = 0$ V is higher for a trap location at source-channel tunnel junction. To analyze flicker, shot, and thermal noise, we created transistor level Verilog-A-based electrical noise models. The results indicate HTFETs competitive noise performance in megahertz frequency range, over Si-FinFET. In the range 10 GHz or more with operating voltages exceeding 0.3 V, HTFET input noise is worse due to the dominance of shot noise. A differential amplifier with active load is used to examine the electrical noise performance at circuit level. We emphasize that high intrinsic gain, drive current, and output resistance of HTFET can be used to achieve superior mixed signal performance metrics in HTFET design over Si-FinFET design, at an improved electrical noise performance.**

***Index Terms*— Electrical noise, flicker, heterojunction TFET (HTFET), random telegraph noise (RTN), shot, Technology Computer Aided Design (TCAD) simulation, thermal, trap, Verilog-A-based model.**

I. Introduction

TUNNEL FET has emerged as a strong alternative to conventional MOSFET for low-voltage and low-power applications. III–V heterojunction TFET (HTFET) with MOSFET like ON-current and sub-60-mV/decade subthreshold slope has been demonstrated in [1] and [2]. Ensuring optimum design performance at low operating voltages and at scaled technology nodes is a great challenge, where electrical noise poses a serious reliability concern [3], [4]. The low frequency noise sources, such as the random telegraph noise (RTN) and flicker noise, scale reciprocally with design footprint, which degrades the performance of both analog, mixed-mode circuits [5] as well as semiconductor memories [6], [7]. The threshold voltage (V_{th}) fluctuation from RTN is shown to exceed 3σ V_{th} variation due to random dopant fluctuation at sub-22-nm nodes [8] as the dominant source of variation in subthreshold MOSFET [9]. Furthermore, the high frequency white noise sources, such as the channel thermal noise and the shot noise are detrimental to analog/RF applications [10]. Hence, a detailed analysis of electrical noise in HTFETs, starting from device level and extending to circuit level evaluation is the goal of this paper.

Our analysis focuses on sub-0.5 V operation regime, which is suitable for low power electronic applications. The Si-FinFET used in our simulations has V_{th} of 0.4 V, hence we will draw comparisons based on near-threshold or subthreshold Si-FinFET design versus HTFET design at a nominal operating voltage of 0.3 V. We specifically focus on III–V HTFET instead of Si-TFET, as Si-TFET suffers from low ON-current [11] and is more vulnerable to RTN as compared with Si-FinFET [12]. We start by investigating a relative RTN amplitude in HTFET in Section II. The aggregate effect of low frequency flicker noise and high frequency shot and thermal noise is examined in Section III. Finally, the electrical noise performance of HTFET versus Si-FinFET-based analog circuit design has been analyzed in Section IV.

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II. Random Telegraph Noise

A. Background and Simulation Setup

The source of RTN in both HTFET and Si-FinFET is attributed to capture and emission of channel carriers by the interface traps [13]. However, as it has been reported for Si-TFETs [14], the HTFET RTN can be more pronounced when the trap is located near the source end of the channel. This is because a trapped charge near the source end can alter the junction electric field and affect the interband tunneling rate. Our goal is to explore the effect of drain current fluctuations (RTN amplitudes) induced by a trapping of an electron charge in an acceptor–type interface state at the gate oxide–channel interface. The RTN analysis for both HTFET and subthreshold Si-FinFET has been presented in a comparative fashion to bring out the key differences.

The simulation setup consists of a 2-D double-gate structure (extended in 3-D, in device simulation) with a nominal gate length of 20 nm and width 40 nm, for both n-type HTFET and n-type Si-FinFET, as shown in Fig. 1(a). The gate oxide has equivalent oxide thickness (EOT) of 0.7 nm. The n-HTFET has GaSb source doped 10^{19} cm^{-3} p-type, intrinsic InAs channel and InAs drain doped 10^{17} cm^{-3} n-type.

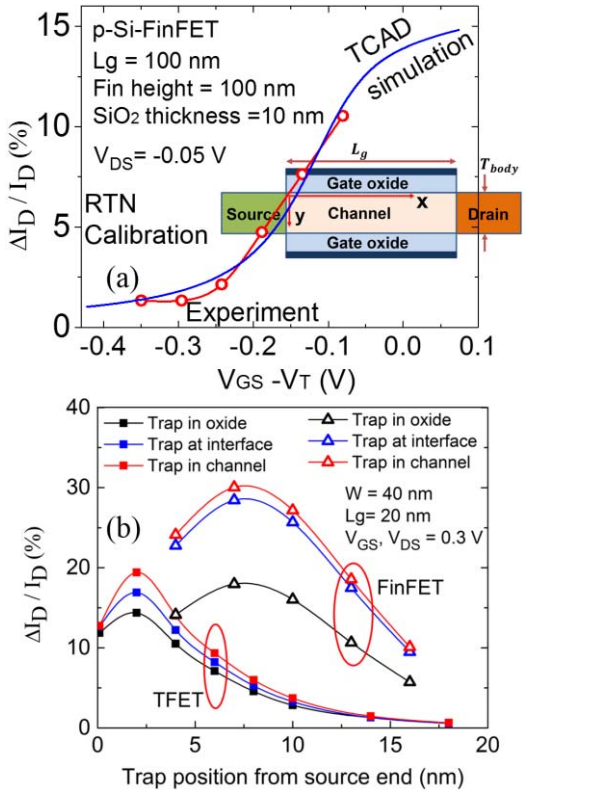

Fig. 1. (a) Calibration of TCAD RTN amplitudes against experimental results reported for p-Si-FinFET [17]. Inset: the Double-gate (DG) simulation structure. (b) Relative RTN amplitude dependence on trap depth and location along channel for TFET and FinFET (n-type).

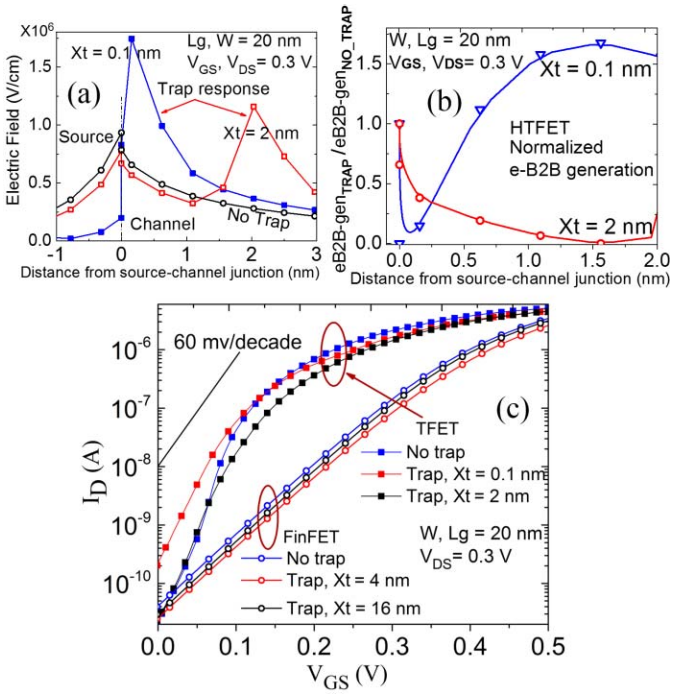

Fig. 2. (a) HTFET electric field profile near source-channel tunnel junction. Profile with trap causes a local reduction in field toward source and a local enhancement toward drain. (b) Electron band-to-band generation rate at tunnel junction, for two trap locations, Xt = 0.1 and 2 nm, normalized against no-trap case. Trap at Xt = 2 nm causes net higher degradation in generation rate. (c) Effect of trap on I_D–V_{GS} characteristics of HTFET and Si-FinFET.

The n-Si-FinFET has source/drain doped 10^{20} cm^{-3} n-type and a 10^{16} cm^{-3} doped p-type channel. The body thickness T_{body} (fin width) of Si-FinFET is 12 nm while HTFET uses a scaled body thickness of 7 nm corresponding to 20-nm channel length [13]. We used Sentaurus TCAD simulator for device simulations [15]. Sentaurus TCAD simulates the structure extending in the third dimension with device width specified by user. TCAD device characteristics of Si-FinFET are calibrated against experimentally demonstrated Si-FinFET device whereas the characteristics of HTFET are calibrated against full-band atomistic simulations, details of which are presented in [16]. A dynamic nonlocal band-to-band tunneling model [15] is used to account accurately for the interband tunneling transitions in HTFET. The tunneling path is determined dynamically based on the energy band profile of the source-channel tunnel junction and generation rate is obtained through nonlocal path integration [15].

B. RTN Simulation Methodology and Calibration

RTN due to a single charge trap is modeled by confining the charge trap to a single node (with predefined coordinates) of mesh, which is suitably refined to limit the speed degradation, while maintaining computational accuracy. A mesh spacing of 2 Å was used around the oxide–channel interface to capture field perturbation due to interface charge trap. The trap concentration is computed automatically by Sentaurus TCAD simulator such that a filled trap always corresponds to one electronic charge [15]. The trapping of electron in the interface trap causes a degradation ΔI_D in the nominal drain current magnitude I_D. This is expressed in terms of normalized RTN amplitude, $\Delta I_D/I_D$. The calibration of normalized RTN amplitudes from TCAD simulations against experimental RTN data for p-Si-FinFETs [17] is shown in Fig. 1(a). An excellent match is achieved assuming midchannel trap location.

C. RTN Dependence on Trap Location

We first analyze the relative RTN amplitude dependence on trap location: 1) in the channel, from the source toward the drain and 2) on varying trap depth: trap in oxide, trap at oxide–channel interface, and trap inside channel. The trap depth inside channel and inside oxide has been limited to 3–4 Å from the oxide–channel interface. As observed from Fig. 1(b), relative RTN amplitude is maximum when the trap is located inside channel followed by trap at the interface and it is minimum when the trap is inside gate oxide. Since we consider the channel to be defect free, our (worst case) analysis is based on the trap located at the oxide–channel interface, which produces the highest RTN. We also identify that, for HTFET, the RTN amplitude is highest for a trap near source end (distance from source-channel junction, Xt = 2 nm), but not for trap almost exactly at source-channel metallurgical junction (Xt = 0.1)nm. However, for Si-FinFET, the worst case RTN is produced for a trap near the source side of midchannel region. An explanation of the observed trends is presented below.

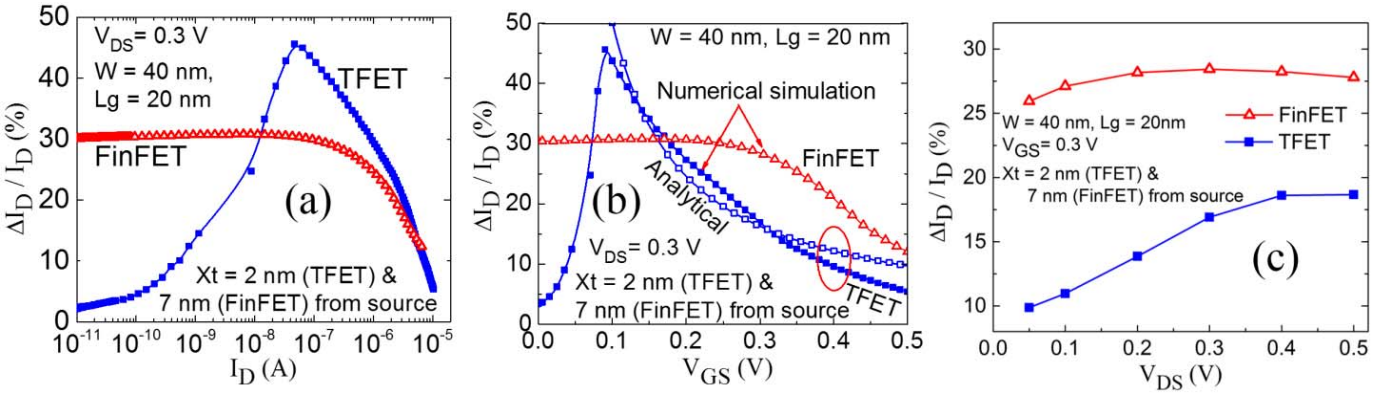

Fig. 3. Relative RTN amplitude dependence. (a) Drain current. (b) Gate voltage. (c) Drain voltage. For $V_{GS} > 0.2$ V, HTFET exhibits lower relative RTN over Si-FinFET. Analytical model (Section II-G) shows good agreement with the TCAD numerical simulations for V_{GS} in range 0.1–0.4 V.

A single charge trap in HTFET positioned at the oxide–channel interface causes a local reduction in the electric field in the channel region on the source side of the trap location. On the other hand, the field enhances in the channel region toward the drain side of the trap location. This behavior is shown in Fig. 2(a), as the trap acts as a natural sink for electric field lines, which are directed toward the source tunnel junction from the channel region. The electron band-to-band (e-B2B) generation rate at distance 1–2 nm away from the source-channel junction is highest and is crucial in deciding tunneling current. The reduction in the electric field on the source side of the trap location decreases the e-B2B generation rate at the source-channel heterojunction, consequently reducing the tunneling current. The local enhancement in electric field toward the drain side of the trap position produces a minor increase in the e-B2B generation rate (and consequently in the tunnel current). We apply this understanding to separately analyze two different trap locations at distance Xt = 0.1 and 2 nm from the source-channel junction. As observed from Fig. 2(a), the trap at location Xt = 0.1 nm shows a peak electric field very close to junction, which contributes both in locally decreasing the e-B2B generation rate at the junction and increasing it just 4–5 Å distance away from it. However, for the trap at Xt = 2 nm, the electric field stays low for a considerably larger distance near the junction as compared with the trap at Xt = 0.1 nm, and hence it produces a net major drop in e-B2B generation rate in 1–2-nm distance of the source-channel junction, as shown in Fig. 2(b). Thus, the trap at location Xt = 2 nm in effect produces a greater reduction in the tunneling current magnitude, and a relatively higher RTN amplitude.

As the trap location in HTFET is moved away from the source, the relative RTN amplitude decreases. This is because the drain current is primarily decided by the tunneling at heterojunction. Moreover, the traps on the drain side of the channel are screened by the higher electron density. Hence, the highest RTN amplitude occurs near the source side of the channel (however, not exactly at tunnel junction, as explained before) due to the modulation of the source-channel junction electric field.

In the case of Si-FinFET, an electron trap near source end is screened due to the high electron concentration in the channel [18], whereas a trap located near the drain end produces a small RTN amplitude due to the presence of the drain field [19]. The maximum RTN amplitude occurs on the source-side of the midchannel region, which corresponds to Xt = 7 nm in our simulations. For further analysis, we will assume trap locations that result in the worst case RTN in HTFET (Xt = 2 nm) and in Si-FinFET (Xt = 7 nm) unless the trap position is stated explicitly.

D. Effect of Trap on Off-State Current Characteristics

Fig. 2(c) shows the I_D–V_{GS} characteristics of both HTFET and Si-FinFET with trap location as a parameter. The off-state current increases with the presence of trap in HTFET, whereas in Si-FinFET, in contrast, the off-state current reduces marginally. This is because in HTFET at small gate biases, the local enhancement in the electric field and hence in the off-state e-B2B generation rate at the source-channel heterojunction is highly pronounced for the trap at Xt = 0.1 nm where the peak electric field occurs within a nanometer of the junction. This cause the off-state current to increase by approximately seven times from the no-trap value, along with degrading the switching slope. Traps farther away from the tunneling junction produce negligible rise in the off-state current. The minor decrease in the off-state current in Si-FinFET is due to the increased potential barrier from the trap, which impedes the thermionic electron injection from the source region.

E. RTN Dependence on Gate and Drain Bias

Relative RTN amplitudes as a function of drain current produced at constant drain bias are shown in Fig. 3(a). For a given on-state drain current, the RTN amplitude observed in HTFET is higher as compared with Si-FinFET. However, the magnitude of gate bias required to obtain the same drain current in HTFET is much less as compared with Si-FinFET. Hence, as shown in Fig. 3(b), for $V_{GS} > 0.2$ V, the relative RTN amplitudes are 10%–40% less (depending upon gate voltage) in HTFET over Si-FinFET. The reduction in HTFET RTN is due to higher carrier concentration in the channel region as compared with Si-FinFET (as HTFET exhibits early turn-on), which screens the charge trap more effectively.

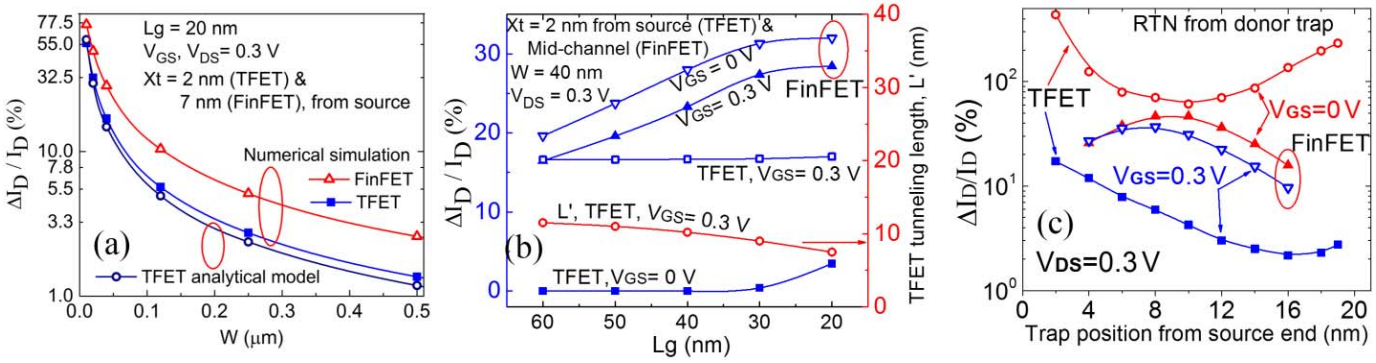

Fig. 4. Relative RTN amplitudes. (a) Transistor width dependence. Analytical model (Section II-G) agrees well with numerical simulation. (b) Gate length dependence. HTFET RTN does not increase inversely with Lg scaling as tunneling distance of carriers shows weak dependence on Lg. Off-state RTN is also shown for reference. (c) Response of donor–type interface trap.

With increase in the gate bias, the carrier concentration in channel region Increases, which increases the screening of charge trap and hence reduces the RTN amplitudes. Moreover, as V_{GS} approaches 0 V, HTFET relative RTN amplitudes reduce rapidly compared with Si-FinFET. This is because $\Delta I_D/I_D$ follows similar trend as g_m/I_D [12], and for HTFET g_m/I_D shows a drop as V_{GS} approaches 0 V (Fig. 8). The dependence of relative RTN amplitude as a function of drain bias V_{DS} is shown in Fig. 3(c). The increase in V_{DS} reduces the carrier concentration near the trap location and hence increases the RTN amplitude. The RTN amplitude saturates following I_D saturation. For Si-FinFET, a small drop in the RTN amplitude at $V_{DS} = 0.5$ V is observed as the minimum electron concentration point in the channel crosses the trap location (near midchannel). However, this effect is not visible in HTFET as the trap causing maximum RTN is located near the source-channel tunnel junction.

F. RTN Dependence on Transistor Size

The relative RTN amplitude induced by the charge trap becomes more pronounced as transistor width is reduced because the trap is less screened in reduced dimensions. This is reflected in the rapid reduction in e-B2B generation rate at the tunneling junction with width reduction, in HTFET. A similar trend is observed in the case of Si-FinFET, as shown in Fig. 4(a). The inverse proportionality relation between the relative RTN amplitudes and transistor width is consistent with the carrier number fluctuation theory [13]. The simulation results of Si-FinFET are also consistent with [18] for the subthreshold MOSFET. The relative RTN amplitude as high as 78% is possible at transistor widths of around 10 nm in Si-FinFET and 56% in HTFET under similar bias conditions.

The dependence of the relative RTN amplitude on gate length Lg is shown in Fig. 4(b). For Si-FinFET, the RTN amplitude increases with Lg scaling consistent with [13]. The departure from the conventional $1/Lg$ scaling trend predicted by carrier number fluctuation theory, in Si-FinFET at sub-30-nm gate length can be explained by assuming a small exclusion region of zero conductivity around the trap, as described elsewhere [18]. However, in the case of HTFET, the RTN amplitude remains almost constant with physical gate length scaling. This is expected in HTFET, where the drain current is controlled by the tunneling distance of carriers at the source-channel junction [20] and aligns with the findings for Si-TFET [12]. The weak dependence of the RTN amplitude on Lg in HTFET is shown in Fig. 4(b). This translates into approximately 40% reduced percent fluctuations in the drain current in HTFET over Si-FinFET, at gate lengths of around 20 nm at 0.3 V, which is an important reliability measure for RTN [19].

We have focused our investigation to acceptor-traps, as the analyzed devices are n-channel FETs where the drain current is primarily affected by electron trapping in acceptor–type interface states. For reference, relative RTN amplitude from a donor–type interface trap (positive charged when empty) is shown in Fig. 4(c). HTFET show significant improvement in donor trap RTN response over Si-TFET reported in [12] due to their higher channel carrier density. Off-state relative RTN amplitudes for HTFET are degraded over Si-FinFET due to change in tunnel barrier caused by the positive charge trap, similar to Si-TFET [12]. On-state donor trap response is still superior in HTFET as the interface trap is more screened due to increased channel carrier density in HTFET as compared with Si-FinFET.

G. HTFET Relative RTN Amplitudes Analytical Model

To model the relative RTN amplitude in HTFET analytically, we assume a uniform effective electric field F at the tunneling junction and use the Kane and Keldysh relation for e-B2B generation rate, R [15]

$$I_D \propto R = AF^2 e^{-B/F} \tag{1}$$

where

$$A = \frac{\pi m_r^{0.5} q^2}{9h^2 E b_{\text{eff}}^{0.5}} \quad B = \frac{\pi^2 m_r^{0.5} E b_{\text{eff}}^{1.5}}{qh}. \tag{2}$$

Eb_{eff} and m_r denote the effective tunneling barrier and tunneling mass, respectively [15]. Equation (1) can be used to express relative RTN amplitude as

$$\frac{\Delta I_D}{I_D} = \left(\frac{2}{F} + \frac{B}{F^2}\right) \Delta F \tag{3}$$

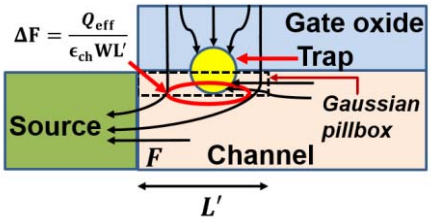

Fig. 5. Single charge trap reduces electric field near source-channel junction. The reduction in electric field is approximated assuming an effective charge Q_{eff} in channel and applying Gauss Law.

where we approximate the change in channel electric field near tunnel junction ΔF due to the trapped charge from Gauss Law, as shown in Fig. 5

$$\Delta F = \frac{Q_{\text{eff}}}{\varepsilon_{\text{ch}} W L'}. \tag{4}$$

L' denotes the tunneling distance of carriers at the source-channel heterojunction [20], ε_{ch} is the electrical permittivity of channel region, and Q_{eff} is the effective charge in channel, which causes reduction in the source-channel junction field, and can be approximated as $Q_{\text{eff}} = \eta q$, where $\eta < 1$, q is electronic charge. In our simulations with worst case RTN, $\eta = 0.5$ provided good fit with numerical simulations. Equations (3) and (4) yield the final form for the relative RTN amplitude as

$$\frac{\Delta I_D}{I_D} = \left(\frac{2}{F} + \frac{B}{F^2}\right) \frac{\eta q}{\varepsilon_{\text{ch}} W L'}. \tag{5}$$

The results from the analytical model agree well with numerical simulations, as shown in Figs. 3(b) and 4(a). To integrate HTFET RTN in circuit simulation, the mean capture and emission times of RTN can be modeled by Shockley–Reed-Hall statistics and the trap capture cross sections can be used from experimentally reported data [21]. Equation (5) can then be used to model RTN amplitudes using an approach similar to that suggested for MOSFETs [22].

III. Flicker, Shot, and Thermal Noise

A. HTFET and Si-FinFET Electrical Noise Device Models

We now focus on characterizing flicker, shot, and thermal noise performance of HTFET versus Si-FinFET. Flicker noise is the dominant noise at low frequencies, which arises from trapping/detrapping of carriers in trap states in the gate oxide around quasi-Fermi level, as shown in Fig. 6(a). The flicker noise model for HTFET used in our simulations is carrier number fluctuation-based [20]

$$\frac{S_{\text{id}}(f)}{I_D^2} = \left(\frac{2}{F} + \frac{B}{F^2}\right)^2 \frac{q^2 N_t(E_{\text{fn}})}{\varepsilon_{\text{ox}}^2 W L' \alpha f} \tag{6}$$

where $S_{\text{id}}(f)$ is the drain current noise power, α is the attenuation factor of carriers in gate oxide, N_t is the interface trap density, while F, B, and L' are all as defined previously.

The flicker noise of Si-FinFET in subthreshold regime, from correlated fluctuations in both channel carriers and mobility, can be approximated by the following [5]:

$$\frac{S_{\text{id}}(f)}{I_D^2} = \frac{AkT}{WL\alpha f N^{*2}} \tag{7}$$

where $S_{id}(f)$ and α are as defined in (6). Parameter A is approximated as effective oxide trap density and N^* is a function of gate capacitance as defined in [5].

The subthreshold thermal noise model [5] is used for Si-FinFET. For HTFET, we use the thermal noise model of on-state MOSFET, which is proportional to the channel conductance at zero drain-source bias [23]. However, the dominant form of white noise in HTFET is shot noise, which is modeled similar to that of case of tunnel diodes [24]

$$i_{\text{shot}}^2 = 2q I_D \Gamma \tag{8}$$

where Γ is the Fano factor, which models the deviation of shot noise magnitude from the nominal Poissonian value of $2qI_D$. Unlike MOSFET, TFETs show higher shot noise. This is typical for tunnel devices where the forward and reverse components of tunneling current across the tunnel junction [I_{CV} and I_{VC}, as shown in Fig. 6(b)] can enhance shot noise due to their individual contributions [24], [25]. The value of Fano factor depends on applied biases and has been reported separately for different material systems [26], [27]. For GaAs/AlAs heterosystem resonant tunnel diodes, a maximum Fano factor of 1.7 was reported [26] whereas Fano factor values as high as 10 were observed in tunnel devices elsewhere [27]. However, due to lack of any experimental data reported for shot noise Fano factor in GaSb/InAs heterojunction, we choose $\Gamma = 2$ in our simulation. This is a good choice for the worst case shot noise analysis, being the maximum reported value of Fano factor for 0.1–0.5 V range of operation [27], which is relevant for low power analog circuit applications. Since no frequency dependence of fano factor is reported in the experimental data for shot noise in heterojunction tunnel diode systems [26], we assume that Γ is frequency independent.

The device level HTFET and Si-FinFET electrical noise models were implemented as flicker and white noise sources in Verilog-A-based code [28] for circuit level simulation in the Cadence Spectre circuit simulator [29] [Fig. 6(c)]. The corner frequency distinguishing flicker noise dominant noise spectrum against white noise (shot and thermal noise) for HTFET is typically ~1 GHz. The simulations were conducted for both n/p channel HTFET and Si-FinFET at two different frequencies: 1 MHz and 10 GHz, which were chosen to bring out the difference in noise performance of FETs due to low frequency flicker noise and high frequency white noise. We assume an interface trap density of 5×10^{11} cm^{-2} and 10^{12} cm^{-2} for Si-FinFET and HTFET, respectively. Both HTFET and Si-FinFET have width of 1-μm, gate length of 20 nm, and EOT of 0.7 nm. A tunneling length $L' = 6$ nm was used for HTFET extracted from TCAD numerical simulations.

B. Noise Simulation Results

The results of transistor level noise simulations are presented for HTFET and Si-FinFET in the form of normalized drain current noise power at output (S_{id}/I_D^2) versus drain

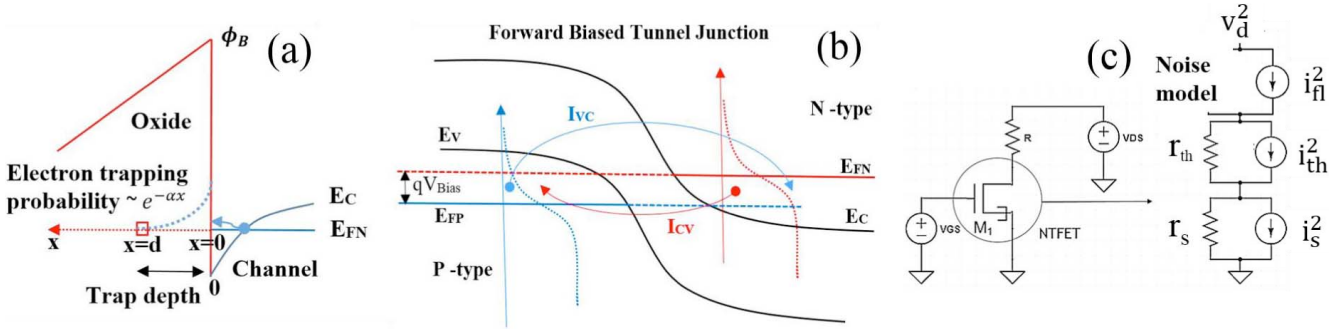

Fig. 6. (a) Flicker noise is caused by trapping/emission of carriers by trap states in oxide. (b) Shot noise across tunnel junction can enhance due to individual contributions from forward and reverse tunnel currents. (c) Representation of flicker, shot, and thermal electrical noise models (noise current sources) implemented at transistor level.

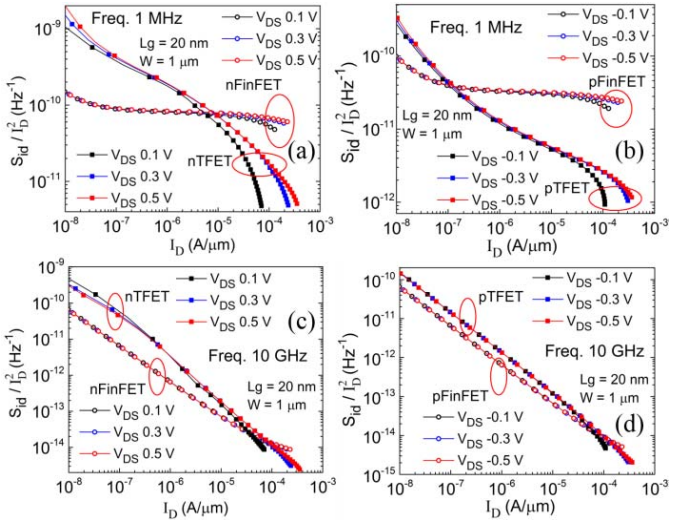

Fig. 7. Normalized drain current noise power: HTFET versus Si-FinFET. (a) n-FET, 1 MHz. (b) p-FET, 1 MHz. (c) n-FET, 10 GHz. (d) p-FET, 10 GHz.

current I_D, and gate referred noise power at input ($S_{\rm VG}$) versus gate voltage ($V_{\rm GS}$). Fig. 7 shows $S_{\rm id}/I_D^2$ versus I_D for both n/p-HTFET and Si-FinFET at frequencies of 1 MHz and 10 GHz. At 1 MHz, the flicker noise is dominant and due to smaller tunneling length of carriers in HTFET, a larger drain current noise is observed for both n/p-HTFET at low I_D. However, as the carrier density in HTFET increases progressively with gate bias at a much faster rate as compared with Si-FinFET (due to sub-kT/q switching slope in HTFET), the $S_{\rm id}/I_D^2$ of HTFET decays more rapidly. HTFETs exhibit 10 times reduced (normalized) drain current noise for I_D exceeding 0.1 mA/μm, as compared with Si-FinFET at 1 MHz. On the other hand, the high frequency noise response of both n/p-HTFET, measured at 10 GHz, is dominated by the shot noise. The cross-over between the noise characteristics of HTFET and Si-FinFET occurs at a much higher drain current value as compared with the low frequency characteristics. However, at 10 GHz, HTFET still demonstrate an overall reduction of around two times in normalized drain current noise over Si-FinFET for I_D exceeding 0.1 mA/μm.

To understand the variation of input referred noise power ($S_{\rm VG}$) versus gate voltage ($V_{\rm GS}$) for n/p-HTFET along with

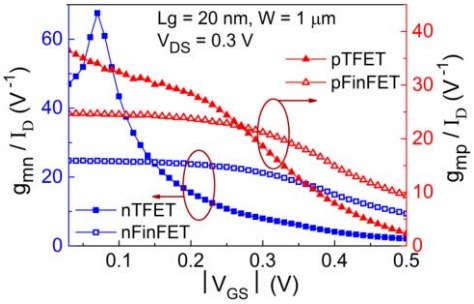

Fig. 8. g_m/I_D characteristics: HTFET versus Si-FinFET (gmn and gmp correspond to n- and p-FET, respectively).

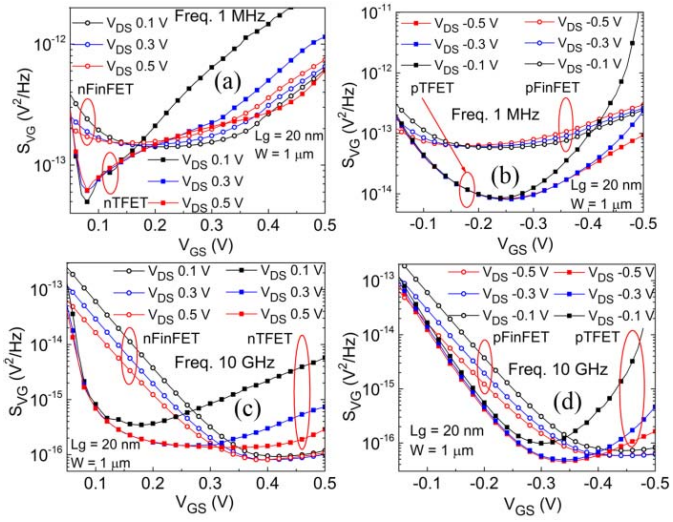

Fig. 9. Input referred noise power: HTFET versus Si-FinFET. (a) n-FET, 1 MHz. (b) p-FET, 1 MHz. (c) n-FET, 10 GHz. (d) p-FET, 10 GHz.

Si-FinFET, it is helpful to analyze the corresponding g_m/I_D characteristics, shown in Fig. 8. As observed, g_m/I_D peaks at low $V_{\rm GS}$ and decreases progressively as $V_{\rm GS}$ is increased. The input referred noise $S_{\rm VG}$ shows inverse square dependence on gate transconductance g_m, which is manifested from the dependence of $S_{\rm VG}$ on $V_{\rm GS}$ shown in Fig. 9. At 1 MHz, following the trend of g_m/I_D, n-HTFET shows approximately 1.2 times increased $S_{\rm VG}$ over n-Si-FinFET whereas p-HTFET shows 7.2 times reduced $S_{\rm VG}$ over p-Si-FinFET, at a gate and

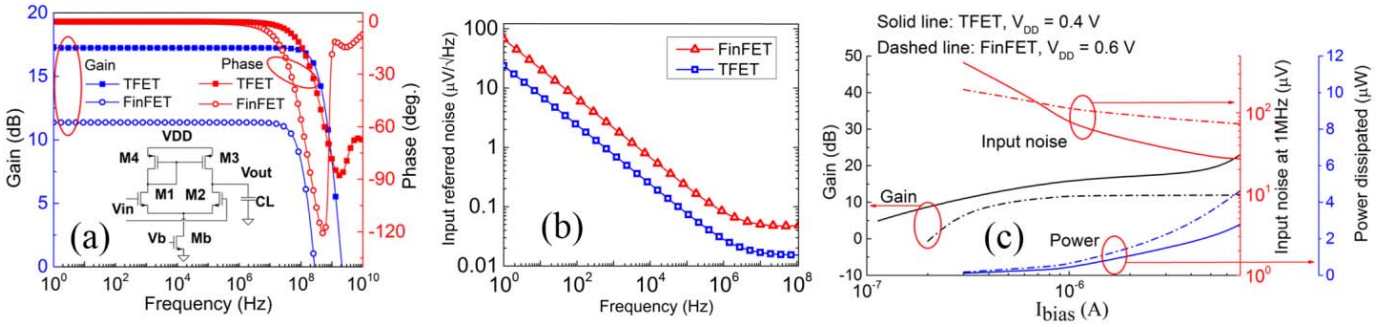

Fig. 10. Differential amplifier with active load: HTFET versus Si-FinFET. (a) Schematic and ac response. (b) Input referred noise dependence on frequency. (c) Gain, input noise, and power dissipation of the design at different bias currents.

drain bias of 0.3 V (in magnitude). The reduction of S_{VG} achieved in p-channel devices is due to the g_m/I_D advantage for p-HTFET being present for a larger range of gate bias as compared with n-HTFET. On the other hand, at 10 GHz, although the shot noise dominates HTFET drain current noise spectrum still HTFET input referred noise becomes very comparable with that of Si-FinFET due to higher intrinsic gain of HTFET. Hence, at frequency of 10 GHz and a gate and drain bias of 0.3 V, n/p-HTFET exhibit 1.3 and 3.3 times less S_{VG}, respectively, as compared with n/p-Si-FinFET. Note that HTFET S_{VG} increases rapidly as the gate voltage is increased beyond 0.3 V, as the g_m/I_D advantage of HTFET is lost at higher V_{GS}.

HTFET thus shows an overall improved electrical noise performance as compared with Si-FinFET for frequencies in the megahertz range. At high frequencies in the range 10 GHz, the shot noise dominates HTFET noise spectrum and can degrade mixed signal circuit performance. However, as HTFET-based designs offer a higher gain and larger bandwidth at same operation voltage as compared with the subthreshold CMOS design, analog circuit designers can exploit this to their advantage as described through a circuit example in the following section.

IV. Circuit Implementation of Noise Models

The electrical noise models for flicker, shot, and thermal noise were implemented in a differential amplifier with active load (a single stage op-amp.) to analyze the noise performance of HTFET versus subthreshold Si-FinFET-based circuit design. The circuit [schematic shown in Fig. 10(a)] was optimized separately for subthreshold Si-FinFET and HTFET designs with load capacitance $C_L = 0.1$ fF (comparable with gate capacitance) to achieve a similar range of gain with certain design restrictions such as, minimum gain of 10 dB, maximum power dissipation of 5 μW, and input referred noise in the range $\mu V/\sqrt{Hz}$.

The ac response of both HTFET design and Si-FinFET design is shown in Fig. 10(a). Table I lists the specifications and performance metrics of the circuit for both HTFET and Si-FinFET design. Note that the HTFET design has same transistor sizing (iso-area design) as Si-FinFET for fair electrical noise comparison. The HTFET design offers two times higher gain at 17.4% less power as compared with the subthreshold Si-FinFET. The 3-dB cutoff frequency is 4.6 times higher

TABLE I
Metrics for Diff-Amp Design

Specification	HTFET	Si-FinFET
V_{DD}	0.4 V	0.6 V
Power	1.9 μW	2.3μW
Gain	17.3 dB	11.3 dB
3dB freq.(fc)	457 MHz	100 MHz
Input noise (at 1MHz)	28 μV	81 μV
Phase Margin	92°	79.6°
CMRR	21.0 dB	25.8 dB
PSRR	28.5 dB	13.3 dB
W/L (same for both designs): M1-M2, M3-M4, Mb (μm/μm)	77.5/0.02, 55/0.02, 2.5/0.02	

in HTFET design with respect to Si-FinFET design. A high differential gain in HTFET design improves the power supply noise rejection capability by approximately six times over Si-FinFET while CMRR is moderately less (21.0 versus 25.8 dB) due to slight increase in common mode gain caused by high g_m of transistors M1 and M2 in HTFET design.

Fig. 10(b) compares the input referred noise of HTFET design and Si-FinFET-based diff-amp design. A higher gain of HTFET design reduces its input referred noise by approximately three times as compared with Si-FinFET. For a given bandwidth, e.g., 1 MHz, the input referred noise voltage for HTFET and Si-FinFET (which defines the minimum limit on input signal distinguishable from device noise) is 28 and 81 μV, respectively. Thus, HTFET design can detect smaller signal amplitudes without corruption from electrical noise.

Fig. 10(c) compares the performance of HTFET and Si-FinFET design at different bias currents, with regard to gain, input referred noise (at 1-MHz bandwidth) and power dissipation metrics. At low bias currents, the intrinsic gain g_m of the transistors is small, which results in an overall small gain of the design. HTFET design still shows improved gain due to higher g_m of HTFET as compared with Si-FinFET. At higher bias current, the gain of Si-FinFET design saturates at around 11 dB, as the output resistance of Si-FinFET degrades with increase in bias current, making the overall gain almost constant. Whereas in HTFET, the improvement in g_m at higher drive current surpasses the degradation in output resistance, resulting in a net increased gain. The input referred noise characteristics in Fig. 10(c) indicate HTFET design shows reduced input referred noise as compared with Si-FinFET,

for bias currents of 0.7 μA and higher, which is attributed to improved gain of HTFET at increased bias current. Finally, Fig. 10(c) also shows that the HTFET design can be biased at higher ON-current to take advantage of high gain and reduced input referred noise features, while still maintaining a low power operation due to its reduced supply voltage as compared with Si-FinFET design. Additionally, given the exponential dependence of drain current on threshold voltage coupled with low ON-currents in the subthreshold regime, it is more difficult to realize stable biasing schemes and maintain circuit performance in subthreshold CMOS design in the presence of variation induced degradation [9], [30]. On the other hand, HTFET-based circuit design are more robust as they exhibit an early turn-on voltage, higher drive currents, and output resistance as compared with subthreshold CMOS design [2], [31]. The effect of temperature change on HTFET ON-current is negligible, which is another desirable feature for reliable biasing circuits [32]. Hence, the overall design specifications make HTFET-based analog mixed signal circuit design more suitable for low-voltage/low-power applications.

V. Conclusion

In this paper, we have performed an analysis of electrical noise in III–V HTFET compared against subthreshold Si-FinFET. HTFET exhibits superior electrical noise performance when contrasted with subthreshold Si-FinFET at 0.3 V. Increased screening of the charge trap from higher channel carrier concentration in HTFET, accompanied by the weak dependence of RTN on the physical gate length scaling enables 40% reduction of relative RTN amplitude in HTFET as compared with Si-FinFET, at 0.3 V for gate length of 20 nm. On the other hand, at $V_{GS} = 0$ V and for trap located at source-channel tunnel junction, RTN increases in the case of HTFET. Our evaluation on flicker, shot, and thermal noise performance of HTFET reveals that at a nominal operation voltage of 0.3 V, HTFET exhibits competitive input referred noise as compared with Si-FinFET in megahertz frequency range, which meets the bandwidth requirement of ultralow voltage sensor applications [33]. However, at operating voltage exceeding 0.3 V with frequency range 10 GHz and higher (RF domain), the HTFET input referred noise increases moderately due to the presence of shot noise. Through a circuit level implementation of noise models in HTFET versus subthreshold Si-FinFET design, we have shown that improved performance metrics can be achieved in HTFET design at a reduced input referred noise, by taking advantage of high intrinsic gain and drive current of HTFET, besides benefitting from its low-voltage/low-power operation.

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