Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability

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***Abstract*— We investigate the effect of a single charge trap random telegraph noise (RTN)-induced degradation in III–V heterojunction tunnel FET (HTFET)-based SRAM. Our analysis focuses on Schmitt trigger (ST) mechanism-based variation tolerant ten-transistor SRAM. We compare iso-area SRAM cell configurations in Si-FinFET and HTFET. Our results show that HTFET ST SRAMs provide significant energy/performance enhancements even in the presence of RTN. For sub-0.2 V operation (Vcc), HTFET ST SRAM offers 15% improvement in read-write noise margins along with better variation immunity from RTN over Si-FinFET ST SRAM. A comparison with iso-area 6T Si-FinFET SRAM with wider size transistors shows 43% improved read noise margin in 10T HTFET ST SRAM at Vcc = 0.175 V. In addition, HTFET ST SRAM exhibits 48X lower read access delay and 1.5X reduced power consumption over Si-FinFET ST SRAM operating at their respective Vcc-min.**

***Index Terms*— Heterojunction TFET, random telegraph noise (RTN), trap, electrical noise, TCAD simulation, SRAM.**

I. Introduction

RANDOM Telegraph Noise (RTN) is a prominent source of threshold voltage fluctuation ΔV_{Th} in MOSFETs [1]. For sub-14 nm technology nodes, ΔV_{Th} from RTN is expected to exceed that from random dopant fluctuation [2], which has been so far the dominant source of variation for sub-threshold MOSFETs. Since the RTN scales inversely with the device footprint, it makes SRAM design most vulnerable to RTN due to minimum-sized transistors used in the cell. Hence, it is of great significance to explore RTN immunity of SRAM designs using CMOS and post CMOS device technologies.

RTN in SOI based Tunnel FET has been studied through simulations in [3] and experimentally in [4]. At very low supply voltage, Vcc, compound semiconductor (III-V) based Heterojunction Tunnel FET (HTFET) has emerged as an alternative for conventional subthreshold MOSFET due to its high on-current and sub-60 mV/decade subthreshold slope [5], [6]. HTFET based Schmitt-Trigger SRAM (ST2 SRAM topology [7]) is shown to offer improved read/write noise margins, with sufficient variation tolerance as compared to Si-FinFET ST2 SRAM [8]. Here we specifically focus on analyzing RTN tolerance of both 6-Transistor (6T) SRAM and 10T ST2 SRAM, for both Si-FinFET and HTFET.

II. Simulation Methodology

Each transistor exhibits a variation of threshold voltage, ΔV_{Th}, caused by trapping and de-trapping of the charge carriers at the interface trap site. Hence, the RTN in each transistor of an "n-T" SRAM cell produces 2^n unique RTN cell-variants [9]. We analyze all 2^n combinations to identify the impact on SRAM read/write noise margins, to examine the RTN induced variation immunity of the SRAM cell. A limitation of this approach [9] is it does not capture the time evolution of RTN. However, since we are quantifying the worst case RTN induced degradation across two different technologies, the current approach still serves as a useful indicator.

The device parameters and the calibration methodology for both Si-FinFET and HTFET, used in SRAM simulations, are provided in [10]. The drain current fluctuation, $\Delta I_{\rm D}$, from RTN is transformed into ΔV_{Th} through the transconductance, $\rm g_m$ at each bias point [11]. For Si-FinFET, $\Delta I_{\rm D}$ was modeled from [12]. For HTFET we use following analytical expression calibrated against TCAD simulations over a Vcc range of 0.1V to 0.5V [10]:

$$\frac{\Delta I_{\rm D}}{\rm I_D} = \left(\frac{2}{\rm F} + \frac{\rm B}{\rm F^2}\right) \frac{\eta q}{\varepsilon_{\rm ch} \rm WL''} \qquad (1)$$

where F is electric field at the source-channel tunneling junction, L″ the tunneling distance of carriers and constant B are as defined in [10], $\varepsilon_{\rm ch}$ is the channel electrical permittivity, and $\eta = 0.5$ is an empirical parameter. In transistor level RTN models we have assumed trap locations giving rise to worst case RTN at device level in operation range of 0.1 V–0.5 V [10]. For HTFET, the trap is located at 2 nm from tunnel junction, whereas for Si-FinFET it is positioned at near mid-channel region. Additionally, in case of HTFET, the impact of a trap located at tunnel junction on SRAM performance has been discussed at end of Section III. RTN from this trap location does not produce worst case noise margins for practical range of Vcc for SRAM operation (for this trap location, $\Delta I_{\rm D}/\rm I_D$ extracted from TCAD simulation is directly used into Verilog-A lookup table based transistor model). Details regarding circuit simulation methodology is presented in [8]. The fluctuation in V_{Th} due to RTN is integrated into the SRAM design for circuit level simulation in the Cadence Spectre circuit simulator [13].

III. Results

Due to the uni-directional conduction in HTFET resulting from its asymmetric source-drain architecture, 6T

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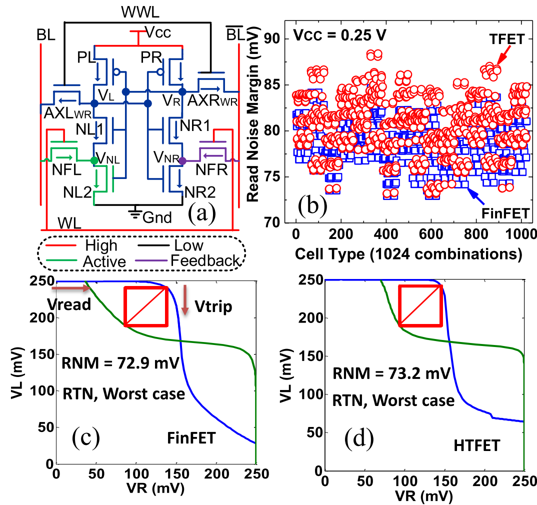

Fig. 1. 10T ST2 SRAM (a) read schematic (b) RNM in presence of RTN in 1024 possible cell types (c) (d) Worst case RTN RNM, FinFET and HTFET.

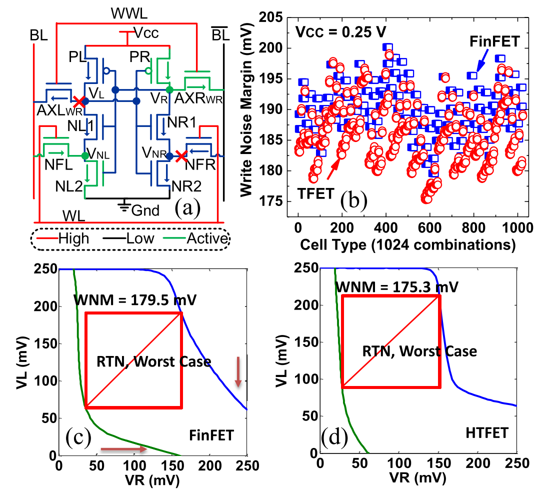

Fig. 2. 10T ST2 SRAM (a) write schematic (b) WNM in presence of RTN in 1024 possible cell types (c) (d) Worst case RTN WNM, FinFET and HTFET.

HTFET SRAM cannot perform simultaneous read and write operation [8]. 6T SRAM shows significant degradation in Read Noise Margin (RNM) due to RTN as shown later [Fig. 4(a)]. Hence, we explore the RTN tolerance of Schmitt Trigger (ST) mechanism based ST2 SRAM topology which has been shown to exhibit variation immunity and to be suitable for ultra-low Vcc operation [7]. We will use the same transistor sizing scheme as used in [8] in order to draw comparison between the RTN performance of HTFET and Si-FinFET based ST2 SRAM.

A 10T ST2 SRAM cell in read mode is shown in Fig. 1(a). Due to RTN in each transistor, a total of 1024 cell combinations are possible. The RNM distribution is depicted in Fig. 2(b) at Vcc = 0.25V. The intrinsic RTN-free RNM for HTFET and FinFET ST2 SRAM is 83.9 mV and 81.7 mV, respectively. Higher Ion and Ion/Ioff ratio of HTFET improves the intrinsic RNM of HTFET ST2 SRAM over Si-FinFET. However, the worst case degradation in RNM (due to RTN) is still comparable: 12.7 % in HTFET and 11 % for Si-FinFET. The percentage RNM degradation is very sensitive to Vcc as we discuss later. Worst case RNM [Fig. 1(c) and (d)] results from RTN in pull-up transistor PL, and in pass gate transistor NFL, along with RTN in pull-down transistor NR2.

Fig. 2 depicts Write Noise Margin (WNM) of ST2 SRAM cell at Vcc = 0.25V. Note that intrinsic no-RTN WNM of HTFET is 183.6 mV which is less compared to 189.2 mV of Si-FinFET, still the % worst case degradation in WNM due to RTN in Si-FinFET is higher: 5.11% against 4.57% of HTFET. Worst case WNM is caused by RTN in pull-up transistor PL and in pass gate transistor NFL, along with RTN in pull-down transistor NR2 and in pass gate transistor AXRWR.

The effect of Vcc scaling on the RTN impact on RNM/WNM is depicted in Fig. 3(a) and (b). Both worst case and best case changes in the SRAM noise margin due to RTN are shown in Fig. 3, which is essential to capture RTN tolerance of SRAM cell. Intrinsic read/write noise margins of ST2 SRAM improve in HTFET design for sub-0.225 V, over subthreshold Si-FinFET. This is a direct consequence of higher Ion/Ioff ratio coupled with increased on-current in HTFET at ultra-low Vcc, which both reduces the influence of trap on channel carriers by screening, as well as improves the

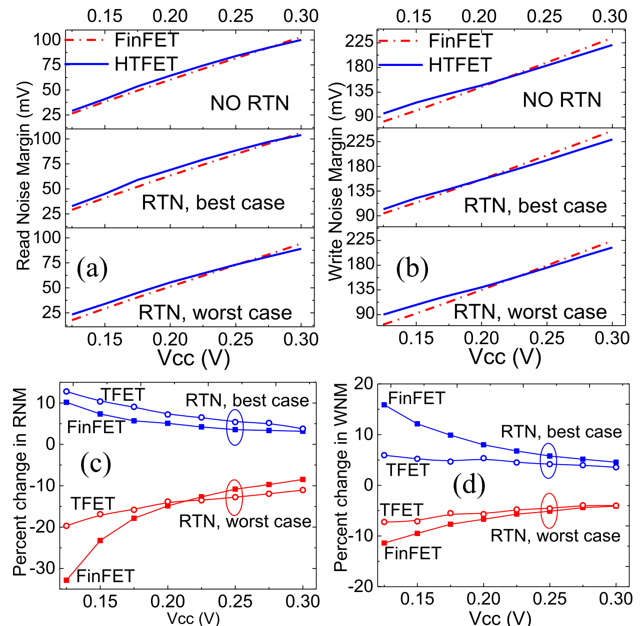

Fig. 3. 10T ST2 SRAM (a) RNM, and (b) WNM trend with Vcc scaling in presence of RTN. Percent change in RNM (c) and WNM (d) indicates HTFET ST2 SRAM is more immune to RTN induced variation.

efficiency of Schmitt feedback action [8] (thereby benefitting the noise margin). Fig. 3(c) and (d) display the percentage variation in RNM/WNM of ST2 SRAM with Vcc scaling. HTFET ST2 SRAM displays a symmetric change in noise margin (best case /worst case RTN) for both read and write operation whereas Si-FinFET SRAM shows significant RNM degradation (>30%) sub-0.2V due to extremely low on-currents in RTN affected subthreshold devices (which also deteriorates Schmitt feedback mechanism and hence the noise margins). Hence, HTFET ST2 SRAM exhibits overall better immunity against RTN induced variation in noise margin in contrast to subthreshold Si-FinFET ST2 SRAM, at ultra-low Vcc. At Vcc = 0.15 V, with worst RTN, HTFET ST2 SRAM offers 15.8% and 17.2% improvement in RNM and WNM over Si-FinFET.

It is important to compare the RTN performance of iso-area 6T Si-FinFET SRAM against 10T ST2 HTEFT SRAM

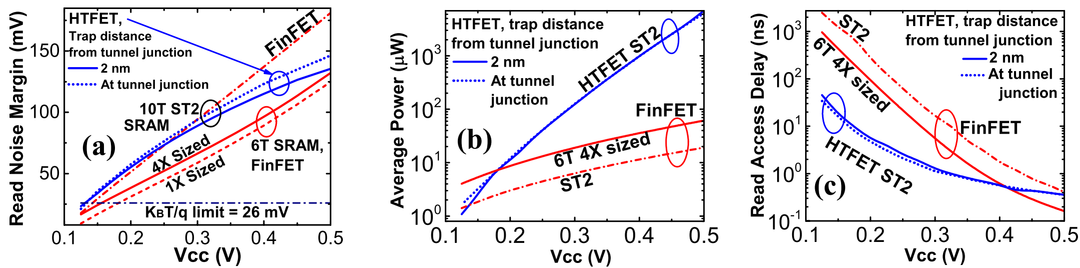

Fig. 4. (a) RNM of 10T ST2 SRAM compared against 6T SRAM (b) Average power consumption of 256×256 SRAM array with 5% activity factor (c) Read-access delay. For HTFET SRAM, plots for 2 different trap locations: trap at tunnel junction and at 2 nm away from tunnel junction are also shown.

TABLE I
NORMALIZED PERFORMANCE METRICS WITH RTN, AT VCCMIN

	HTFET 10T ST2	Si-FinFET 10T ST2	Si-FinFET 6T 4X sized
Vcc-min (mV)	132	145	158
Power dissipation	1X	1.5X	5X
Read-access delay	1X	48X	12X

as the influence of RTN diminishes in upsized transistors. In order to meet the iso-area condition, the 6T Si-FinFET SRAM uses 4X sized transistors [8] which results in improved RNM over 1X sized 6T SRAM, as depicted in Fig. 4(a). Still the RNM of 4X sized 6T Si-FinFET SRAM is 43% less that of 10T ST2 HTEFT SRAM (with trap distance, Xt = 2 nm from tunnel junction) at Vcc = 0.175V, and, hence, the performance of ST SRAM design remains superior due to Schmitt feedback action. RNM of 10T ST2 Si-FinFET SRAM improves at higher Vcc as Si-FinFET gains in on-current as it transitions out of subthreshold operation regime (V_{Th} ~0.4 V). The average power consumed by 256 × 256 SRAM array with an activity factor of 5%, using an approach similar to [8], is shown in Fig. 4(b) along with read access delay in Fig. 4(c). At Vcc = 0.175 V, HTFET ST2 SRAM (Xt = 2 nm) exhibits 75X and 21X faster read-access times as compared to FinFET ST2 SRAM and FinFET 6T-4X sized SRAM respectively.

In HTFET, RTN from the trap at tunnel junction is prominent only for VGS <0.1 V [10]. Hence, as Vcc scales down to 0.13 V and below [Fig. 4(a)], RTN from trap at tunnel junction produces worse SRAM RNM than RTN from the trap at Xt = 2 nm. However, lower limit on Vcc (Vcc-min) is set by a minimum RNM requirement of 26 mV ($k_B T/q$, T = 300K). This Vcc-min exceeds 0.13 V for all SRAM designs discussed in this work (refer Table I). Hence the effect of trap at the tunnel junction is not pronounced for practical SRAM Vcc range and consequently, the trap at Xt = 2 nm gives rise to worst case RTN. The trap at tunnel junction although turns the devices more leaky (higher average power than Xt = 2 nm trap, Fig. 4(b), still comparable to Si-FinFET ST2 SRAM at its Vcc-min) along with marginally fast read-access [Fig. 4(c)] enabled by higher drain current. The average power consumption and read-access delay of Si-FinFET ST2 and 6T-4X sized SRAM, normalized against HTFET ST2 SRAM, at their respective Vcc-min for worst case RTN, is shown in Table I, indicating power savings in HTFET design at ultra-low Vcc.

IV. CONCLUSION

RTN in HTFET based SRAM is analyzed for the first time. 6T HTFET SRAM shows significant degradation of RNM as compared to Si-FinFET 6T SRAM due to delayed saturation in HTFET output characteristics. 10T ST2 SRAM using Schmitt Trigger feedback mechanism to suppress variation is examined to explore its RTN immunity. For sub-0.225 V operation, HTFET ST2 SRAM supersedes Si-FinFET ST2 SRAM in performance due to high Ion and Ion/Ioff ratio of HTFET (which improves effectiveness of Schmitt feedback [8]). At 0.15V, HTFET ST2 SRAM offers 15.8% and 17.2% improvement in RNM and WNM respectively over Si-FinFET ST2 SRAM, besides exhibiting better tolerance against RTN induced variation and faster operation with competitive power dissipation. Thus HTFET ST2 SRAM meets performance and power requirements at ultra-low Vcc SRAM applications.

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