Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III–V Semiconductor) on Variation for Logic and SRAM Applications

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***Abstract*— The need to enhance transistor performance below 22-nm node has brought in a change in transistor architecture from planar bulk to either ultrathin-body SOI (UTB SOI) or 3-D trigate transistors. Further improvement in transistor performance at sub-7-nm node is likely to require replacement of silicon channel with high-mobility compound semiconductor (III–V) materials. This paper presents a numerical 3-D simulation study of process variation and sidewall roughness/surface roughness effects on 3-D trigate (tapered and rectangular cross sections) on bulk and UTB SOI devices. We also investigate the effects of variation on future III–V trigate transistors using the same 3-D TCAD scheme. The results show that the threshold voltage variation value, ΔV_T, in rectangular Si trigate and UTB SOI due to all the variation sources are 13.1 and 24.6 mV, respectively. Moreover, between Si and III–V compound semiconductors, the $In_{0.53}Ga_{0.47}As$ trigate shows 1.5 times lower total ΔV_T value making it a promising candidate for Si replacement. A Monte Carlo study of 6T SRAM cell with fin width or body thickness variation show that the 3σ value of read static noise margin [3σ(RSNM)] is least in SRAMs with rectangular Si trigate. This paper also shows that a 6T SRAM cell at different V_{CC} shows that a Si trigate has V_{CCmin} below 0.4 V.**

***Index Terms*— III–V compound semiconductor, FinFET, line edge roughness (LER), sidewall roughness (SWR), SRAM, surface roughness (SR), trigate, UTB SOI.**

I. Introduction

THE technology node of 22 nm has witnessed the evolution of the traditional planar bulk silicon transistor architecture to trigate on bulk Si [1] as well as the ultrathin-body planar SOI (UTB SOI) substrates [2]. With scaling, source and drain come closer to each other and the control of gate electrode on the channel weakens causing more short-channel effects (SCEs) in a planar transistor. In trigate transistors, however, the gate control on the channel increases threefold. Increase in the gate control and reduction in the SCEs are the main motivation behind the switch to trigate on bulk and UTB SOI devices [3], [4]. The improved electrostatics, lower drain to source leakage and near ideal subthreshold characteristics suppress the V_T variation in these devices enabling the possibility of aggressive V_{CC} scaling suitable for low-power mobile system-on-chip applications. Along with trigate architecture, replacing silicon with high-mobility compound (III–V) semiconductor is another big step toward enhancing transistor performance [5], [6]. It is crucial to study the variation effects on such promising future candidates of semiconductor industry.

At the sub-22-nm technology node, due to the small feature sizes these transistors will be highly sensitive to the process variations. In addition to gate length, L_G, oxide thickness, T_{ox}, and random-dopant fluctuation (RDF) parameters, trigate deals with fin width, W_{FIN}, fin height, H_{FIN}, and fin tapering angle, θ variation parameters unlike planar devices. The fin lithography and etching steps of trigate results in sidewall roughness (SWR) of the fin. Moreover, in UTB SOI there is surface roughness (SR) in the silicon body. Due to scaling, the critical dimensions of the transistor like the fin width or body thickness, W_{FIN}, are now becoming comparable with the parameters of SWR/SR viz. root-mean-square (rms) amplitude (Δ) and correlation length (Λ) [7], [8], [9]. Also, due to the lower effective mass of electron in compound (III–V) semiconductors than Si, the SWR/SR variation effect due to quantum confinement in the fin will be more in the former. With increased sources of variation and higher impact of SWR/SR, it is essential to do a comparative variation study on these devices.

In this paper, we present 3-D numerical simulation results to study the effect of process variations on transistor architecture and material. The circuit level impact of variations is illustrated using the 6T SRAM cell. The simulation setup for silicon trigate (with rectangular and tapered profiles) on bulk, UTB SOI and $In_{0.53}Ga_{0.47}As$ trigate along with the calibration results are discussed in Section II of this paper. Two different architectures namely trigate and UTB SOI are studied in

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Section III. The material comparison between silicon and $In_{0.53}Ga_{0.47}As$ trigate is carried out in Section IV of this paper. To see the impact of variation on circuits, we studied 6T SRAM cells with fin width variation as presented in Section V.

II. Simulation Methodology

Fig. 1 shows the 3-D simulation structures of (a) planar bulk Si nMOS, (b) Si trigate on bulk (rectangular and tapered profiles), (c) Si UTB SOI, and (d) $In_{0.53}Ga_{0.47}As$ trigate devices. Using Sentaurus 3-D TCAD simulator we first calibrate the Si trigate [1], Si UTB SOI [2], and $In_{0.53}Ga_{0.47}As$ trigate [5] devices.

The calibrated Si trigate transistor has a gate length, L_G of 26 nm, effective oxide thickness, EOT of 0.9 nm with 0.5 nm of SiO_2 sandwiched between HfO_2 and the fin, channel doping, N_{ch} of 1e16 cm^{-3}, and S/D doping, N_{sd} of 1e20 cm^{-3} operating at 0.8 V V_{CC}. The width at the middle part of the tapered trigate is 8 nm with tapering angle of 84°. The calibrated UTB SOI has L_G of 22 nm, EOT of 0.85 nm, N_{ch} of 1e16 cm^{-3}, N_{sd} of 2e20 cm^{-3}, and W_{FIN} of 5 nm operating at 1 V V_{CC}. The calibrated $In_{0.53}Ga_{0.47}As$ trigate has L_G of 60 nm, EOT of 1.2 nm, N_{ch} of 1e14 cm^{-3}, N_{sd} of 4e19 cm^{-3}, and WFIN of 40 nm operating at 0.5 V V_{CC}. 3-D drift diffusion simulations are carried out using the field-dependent mobility model (Caughey-Thomas) for transport and density gradient model to capture quantization effect. To calibrate these devices the mobility model is modified based on its doping dependence, high field saturation effects and normal field dependence. The normal field model takes into account the carrier scattering due to surface roughness at the semiconductor/insulator interface, particularly at high gate bias regime. Fig. 2 shows the calibrated $I_D V_G$ plots for all the three devices. Simulation results show excellent agreement with the experiment. The inset in Fig. 2(a) tabulates the calibrated parameter values. It can be seen in Fig. 2(b) that the simulated $In_{0.53}Ga_{0.47}As$ trigate shows better SCEs than the experimental. This is because we have assumed an ideal gate to $In_{0.53}Ga_{0.47}As$ fin interface with no interface state density (D_{it}) in the simulation.

In this paper, we have compared the variation effects in all these devices at 22-nm technology node with L_G of 26 nm and EOT 0.9 nm using the calibrated models of Si trigate, UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate. An equivalent planar Si nMOS device [Fig. 1(a)] is simulated for comparison purposes. Also, an equivalent Si trigate of rectangular cross-sectional profile with W_{FIN} of 8 nm is simulated.

Table I summarizes the electrical parameters of planar Si, Si trigate (rectangular and tapered profiles), UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate at fixed I_{OFF} of 100 nA/μm and V_{CC} of 0.8 and 0.5 V. Because of weaker gate control on the channel, planar Si transistors exhibit lower performance and higher SCEs than the trigate or UTB SOI devices. Si trigate with rectangular cross section performs better than tapered cross-sectional trigate. Moreover, at 0.5 V V_{CC}, $In_{0.53}Ga_{0.47}As$ trigate shows higher ON current than Si owing to the higher effective velocity, v_{Eff} of electrons in the former [inset of Fig. 2(b)]. Also, the better electrostatics in $In_{0.53}Ga_{0.47}As$ trigate is because of the higher effective channel length, L_{Eff}, than Si trigate [10]. L_{Eff} can be defined as the length over which the gate modulates the channel electron density. Plotting the electron density along the channel length in Fig. 3 at increasing gate biases for Si and $In_{0.53}Ga_{0.47}As$ trigates shows that the L_{Eff} is higher in the latter leading to better SCEs. This increase in L_{Eff} is because of the process limitation of lower source/drain (S/D) doping in $In_{0.53}Ga_{0.47}As$ trigates.

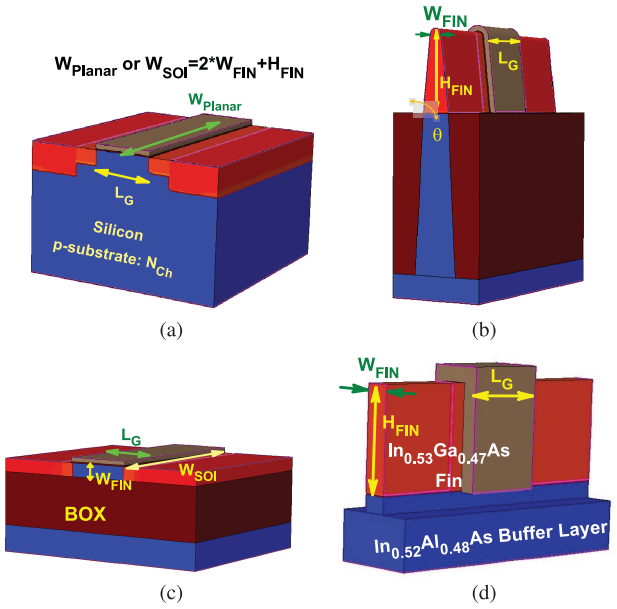

Fig. 1. 3-D TCAD models of (a) planar silicon, (b) bulk silicon trigate, (c) silicon UTB SOI, and (d) $In_{0.53}Ga_{0.47}As$ trigate.

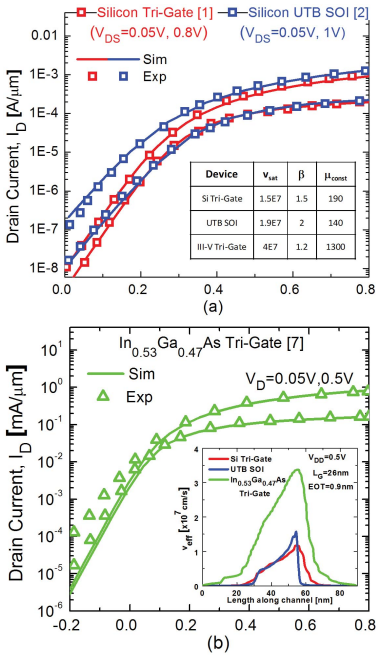

Fig. 2. $I_D V_G$ of calibrated 3-D models of Si trigate, UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate [1], [2], [5]. Inset in (a) tabulates the calibrated parameter values for all the devices. Inset in (b) compares the effective electron velocity, v_{eff}, along the channel region for all three devices.

TABLE I

COMPARISON OF THE ELECTRICAL PARAMETERS AT FIXED I_{OFF} OF 100 nA/μm OF PLANAR Si, BULK Si TRIGATE (TAPERED AND RECTANGULAR PROFILES), UTB SOI, AND $In_{0.53}Ga_{0.47}As$ TRIGATE AT 0.8 V V_{CC} AND 0.5 V V_{CC} WITH $L_G = 26$ nm

nMOS	V_TSat (mV)	I_{DSat} (mA/μm)	I_{DLin} (mA/μm)	SS (mV/dec)	DIBL (mV/V)
		V_{CC}=0.8V			
Planar Si	185	0.678	0.104	105	128
Tapered Si Tri-Gate	165	1.068	0.198	75	52
Rectangular Si Tri-Gate	151	1.155	0.222	70	43
UTB SOI	186	1.196	0.202	97	89
		V_{CC}=0.5V			
Planar Si	186	0.251	0.066	101	113
Tapered Si Tri-Gate	158	0.431	0.138	74	64
Rectangular Si Tri-Gate	151	0.472	0.150	70	53
UTB SOI	179	0.440	0.123	94	110
$In_{0.53}Ga_{0.47}As$ Tri-Gate	148	0.577	0.239	66	31

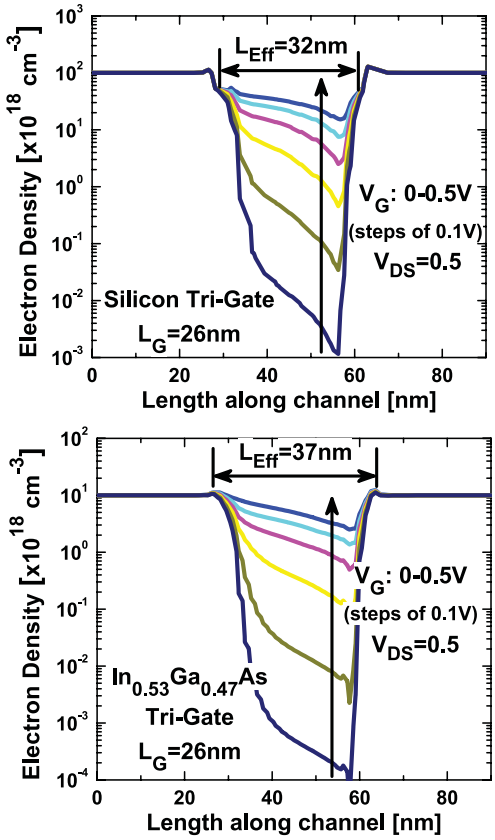

Fig. 3. Electron density along the channel region in Si and $In_{0.53}Ga_{0.47}As$ trigate with increasing gate bias. L_{Eff} is defined as the length over which the gate modulates the channel electron density. L_{Eff} is higher in $In_{0.53}Ga_{0.47}As$ trigate than silicon.

The direct bandgap material, $In_{0.53}Ga_{0.47}As$, has low electron effective mass in the Γ valley thus giving higher mobility than silicon. By increasing the applied voltage, the conduction of electrons in $In_{0.53}Ga_{0.47}As$ transfers to heavier L valley that lowers the electron mobility [11]. Thus $In_{0.53}Ga_{0.47}As$ devices are suitable for low voltages. In this paper, we study silicon

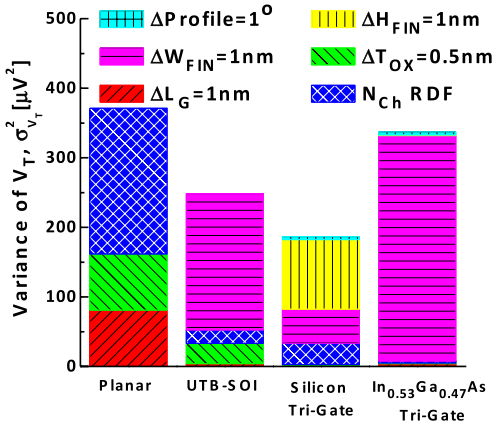

Fig. 4. Variance of V_T of planar, silicon trigate, UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate with L_G of 26 nm for all sources of variation except SWR/SR.

devices at V_{CC} of 0.8 V for different architectures (Section III) whereas comparison with $In_{0.53}Ga_{0.47}As$ devices is done at V_{CC} of 0.5 V (Section IV).

Fig. 4 plots the variance of V_T due to all process parameter variations except SWR/SR. For 1 nm change in W_{FIN}, H_{FIN}, and L_G parameters and 0.5 nm change in T_{OX}, the variance of V_T is shown. The estimation of ΔV_T due to RDFs is determined using the impedance field method [12]. Though there is an increase in the number of variation sources in trigate and UTB SOI structures yet they show lower overall V_T variation than the planar transistor. Variation due to H_{FIN} in bulk Si trigate is much higher than $In_{0.53}Ga_{0.47}As$ trigate. This can be explained using the electrostatic potential contors shown in Fig. 5. Below the S/D junction, the potential contor spreading ends at the high barrier $In_{0.52}Al_{0.48}As$ buffer layer in $In_{0.53}Ga_{0.47}As$ trigate but the spreading continues in Si bulk of Si trigate. With H_{FIN} variation (assuming the S/D doping profile to be constant), the channel sees more variation in potential in Si trigate than in $In_{0.53}Ga_{0.47}As$ trigate. Thus leading to higher ΔV_T in the former.

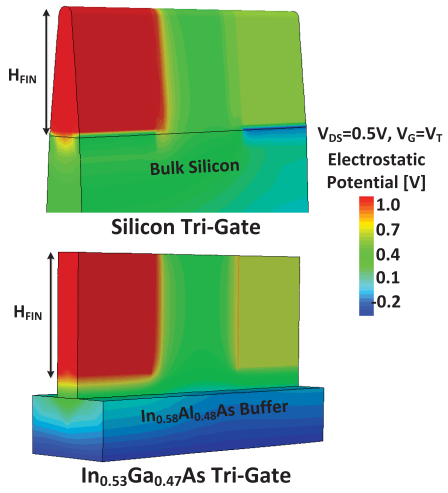

Fig. 5. Electrostatic potential contor at threshold voltage condition of Si and $In_{0.53}Ga_{0.47}As$ trigates. Si trigate shows higher H_{FIN} variation because of the continued spreading of potential in the bulk region below S/D junction unlike the $In_{0.53}Ga_{0.47}As$ trigate.

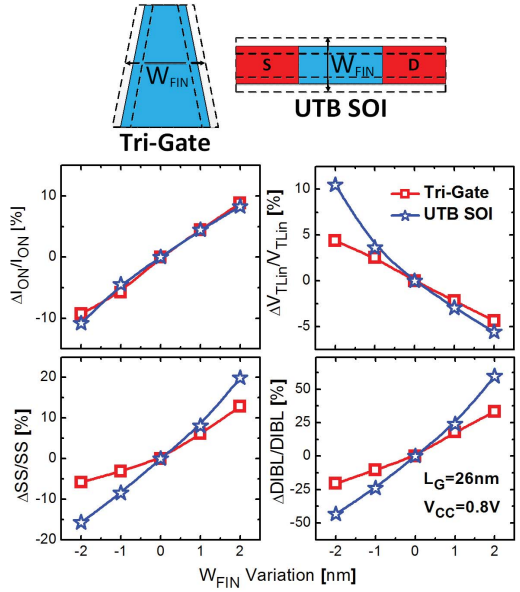

Fig. 6. Sensitivity comparison of 3-D trigate with UTB SOI shows higher variation in electrical parameters of UTB than Si trigate.

Further in this paper, we do not investigate the variation effects in planar transistor because higher variation and weak channel control makes it unsuitable for future technology nodes. The current analysis (Fig. 4) does not include the SWR/SR variations. SWR or SR causes local variations in the fin or body thickness, W_{FIN} of trigate or UTB SOI. A Monte Carlo simulation-based study of SWR/SR variations using full 3-D device simulation is presented in the next section.

III. Transistor Architecture SWR/SR Study

In this section, we will study the effect of variation on Si trigate and UTB SOI devices. In both these architecture, increasing the gate control on the channel to reduce the SCEs was the important motivation. Confining the electrons in the channel by thinning W_{FIN} is the most effective method to achieve this. But due to process variations, the devices

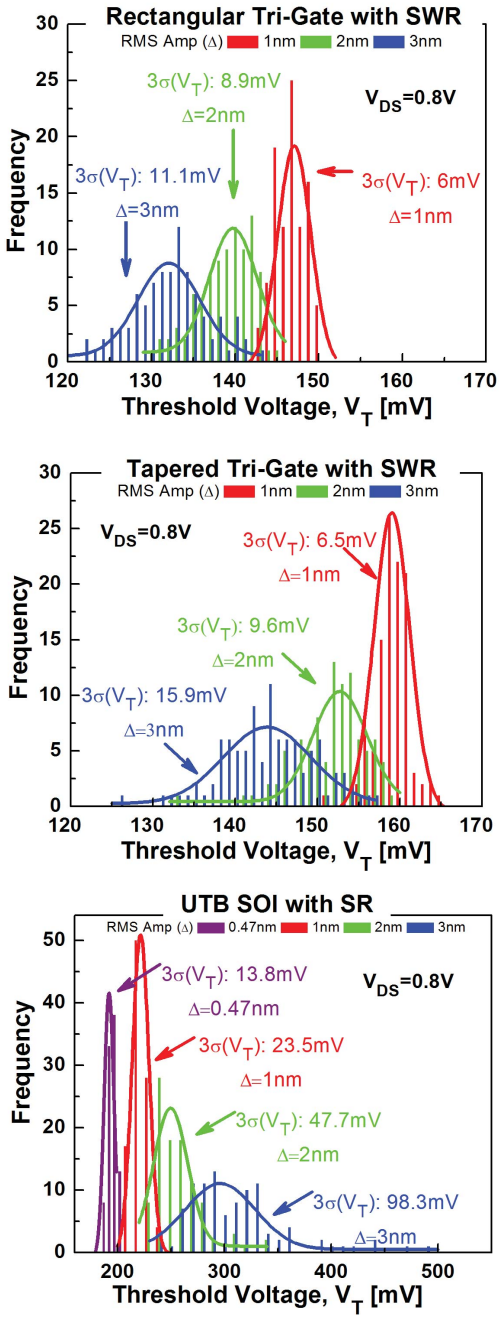

Fig. 7. Monte Carlo simulation of SR in rectangular, tapered Si trigates and UTB SOI. Reducing rms amplitude reduces $3\sigma(V_T)$ for all the three devices. With decreasing rms amplitude, mean of V_T increases for Si trigate but decreases for UTB SOI because thicker regions dominated in trigate and thinner in UTB SOI devices. Rectangular trigate gives least variation due to SR.

become very sensitive to variations in W_{FIN}. We performed a sensitivity analysis by uniformly varying W_{FIN} of trigate and UTB SOI as shown at the top on Fig. 6. Fig. 6 plots the W_{FIN} sensitivity study of variations in ON current (I_{ON}), linear threshold voltage (V_{TLin}), subthreshold slope (SS) and DIBL of Si trigate and UTB SOI devices. It is seen that the UTB SOI is more sensitive than the trigate transistor to W_{FIN} variation.

In today's devices, the critical dimension of W_{FIN} (8 nm for trigate and 5 nm for UTB SOI) is comparable with the

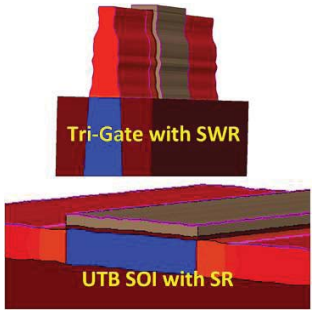

Fig. 8. 3-D structure of silicon trigate and UTB SOI with SWR/SR implementation.

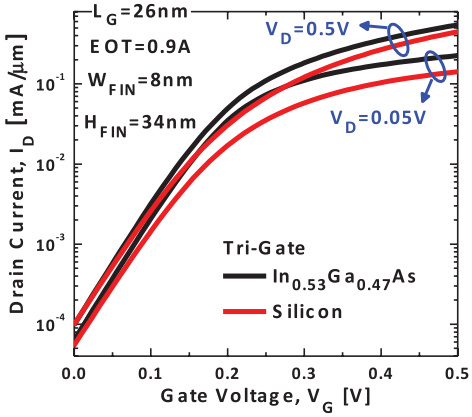

Fig. 9. Comparison of $I_D V_G$ of Si and $In_{0.53}Ga_{0.47}As$ trigates at 0.5 V V_{CC}. $In_{0.53}Ga_{0.47}As$ trigate shows higher performance than Si because of its higher injection velocity. Electrostatics is also better in the former owing the higher effective channel length due to lower SD doping.

state-of-the-art SWR/SR parameters (Δ of 0.5-3 nm, Λ of 20 nm). To study the SWR/SR effect, we implemented a 1-D Fourier synthesis of Gaussian autocorrelation function that is used to generate random roughness on the sidewalls of trigate Fin and the Si body of UTB SOI [8], [13]. The implementation flow of developing SR on device structure is similar to [10]. A total of 100 3-D device samples with randomly generated SWR and SR on Si trigate (rectangular and tapered fins) and UTB SOI for Δ of 1, 2, and 3 nm and Λ of 20 nm were simulated. We have also considered 0.47 nm Δ and 1.4 nm Λ case for UTB SOI as reported in [13].

Fig. 7 shows the histogram of V_T variation of these ensembles of devices. As the rms amplitude of SWR/SR increases, we see that: 1) the 3σ of V_T increases for all the three cases since the local variation in W_{FIN} also increases and 2) the mean value of V_T ($\mu(V_T)$) decreases for trigate while it increases for UTB SOI. This can be explained using Fig. 8 that shows an example of SWR/SR in Si trigate and UTB SOI. With thinner W_{FIN}, V_T of the transistor increases due to the increase in confinement (Fig. 6). With SWR/SR in a device, there will always be regions that are thicker or thinner than the nominal W_{FIN} in the channel. In 3-D trigate with SWR, the thicker regions dominate the subthreshold characteristics by forming a parallel path of conduction from source to drain and thus reducing the mean of V_T. In UTB SOI, these thicker regions are electrically coupled in series with the thinner channel

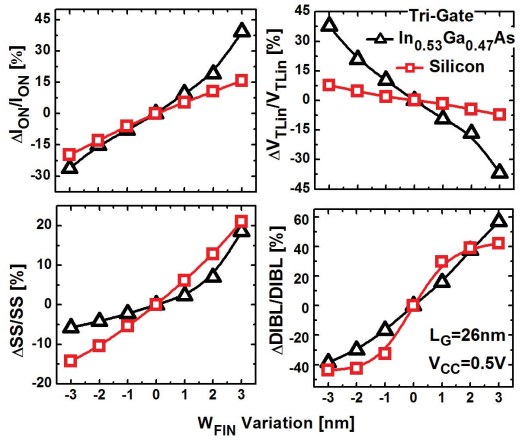

Fig. 10. W_{FIN} sensitivity analysis of Si and $In_{0.53}Ga_{0.47}As$ trigate. $In_{0.53}Ga_{0.47}As$ trigate being a low mass system show higher quantization effects giving higher V_T variation than Si trigate.

regions. So in UTB SOI, thinner channel regions dominate the subthreshold characteristics and increase the mean of V_T. Si trigate with rectangular cross section shows less $3\sigma(V_T)$ than the tapered cross section. In the next section, we present a material comparison between Si and III–V trigates with SWR variation.

IV. Silicon Versus III–V Trigate SWR Study

III–V compound semiconductors like $In_{0.53}Ga_{0.47}As$ are expected to replace Si as channel material in CMOS technology in the near future because of its excellent transport properties [6]. In this section, we will compare the variation results between Si and $In_{0.53}Ga_{0.47}As$ trigate (both with rectangular fins) using the calibrated model presented in Section II. Since the results in the previous section indicate that rectangular cross-sectional fins are least sensitive to SWR variation, we consider only rectangular fin for Si and $In_{0.53}Ga_{0.47}As$ trigates in this section. Fig. 9 shows the $I_D V_G$ of both the trigates with $L_G = 26$ nm, EOT = 0.9 nm, $W_{FIN} = 8$ nm, and $H_{FIN} = 34$ nm at V_{CC} of 0.5 V and fixed I_{OFF} of 100 nA/μm. Because of higher injection velocity and L_{Eff}, $In_{0.53}Ga_{0.47}As$ trigate gives higher I_{ON} and better electrostatics than Si trigate [inset of Figs. 2(b) and 3].

As the transistor channel is confined further, the bands start splitting into sub-bands. The separation between conduction band and the first sub-band and also among sub-bands is inversely proportional to the electron effective mass, m_e^*, and $(W_{FIN})^2$. $In_{0.53}Ga_{0.47}As$ being a lower effective mass system than Si has higher quantum confinement effect. Fig. 10 plots the variation in the electrical parameters due to W_{FIN} fluctuation in Si and $In_{0.53}Ga_{0.47}As$ trigates. Due to higher quantum confinement, variation in I_{ON} and V_{TLin} is more in $In_{0.53}Ga_{0.47}As$ trigate. The variation in SS and DIBL is less in $In_{0.53}Ga_{0.47}As$ trigate because of the better electrostatics as discussed in Section II (Fig. 3).

Using the same algorithm scheme as shown in [10], we simulate an ensemble of 100 variant Si and $In_{0.53}Ga_{0.47}As$ devices with SWR at V_{CC} of 0.5 V. SWR with rms amplitude, Δ, of

TABLE II
SUMMARY OF ΔV_T DUE TO ALL THE SOURCES OF VARIATION IN RECTANGULAR Si TRIGATE, TAPERED Si TRIGATE, UTB SOI, AND $In_{0.53}Ga_{0.47}As$ TRIGATE

Source	Rectangular Si Tri-Gate	Tapered Si Tri-Gate	$In_{0.53}Ga_{0.47}As$ Tri-Gate	UTB SOI
All Others except ΔW_{FIN} (Fig 4)	11.6	11.6	3.3	7.3
SWR/SR (Δ=1nm, Λ=20nm)	6	6.5	7.8	23.5
Total ΔV_T(mV)	**13.1**	**13.3**	**8.5**	**24.6**

TABLE III
SUMMARY OF 3σ RSNM (mV) OF 6T SRAM CELLS WITH RECTANGULAR Si TRIGATE, TAPERED Si TRIGATE, $In_{0.53}Ga_{0.47}As$ TRIGATE, AND UTB SOI DEVICES AT 0.5 V V_{CC}, $L_G = 34$ nm, AND $I_{OFF} = 10$ nA/μm

W_{FIN} variation (Δ)	Rectangular Si Tri-Gate	Tapered Si Tri-Gate	$In_{0.53}Ga_{0.47}As$ Tri-Gate	UTB SOI
1nm	12.9	15.6	31.1	22.1
2nm	26.2	25.4	60.1	24.5
3nm	39.4	40.5	91.8	40.9

1, 2, and 3 nm and correlation length, Λ, of 20 nm give $3\sigma(V_T)$ of 5.5, 8.2, and 12.7 mV in Si trigate, respectively. Whereas the $3\sigma(V_T)$ values for SWR with Δ of 1, 2, and 3 nm in $In_{0.53}Ga_{0.47}As$ trigate are 7.8, 15, and 15.3 mV, respectively. Because of the higher quantum confinement effect, the $3\sigma(V_T)$ of $In_{0.53}Ga_{0.47}As$ is higher than that of Si and also it progressively increases with the rms amplitude.

Table II summarizes variation study done for all the devices in this paper. Assuming all the sources of variation are uncorrelated, the overall V_T variation is given by the rms of ΔV_T due to individual sources [14] as given by (1). $In_{0.53}Ga_{0.47}As$ trigate shows the least total variation effect than Si trigate while the total ΔV_T of UTB SOI is 28.3 mV. Higher performance and better electrostatics of $In_{0.53}Ga_{0.47}As$ trigate makes it a promising replacement of Si with greater control in SWR of $In_{0.53}Ga_{0.47}As$ fins

$$\Delta V_T(mV) = \sqrt{(\Delta V_{T1})^2 + (\Delta V_{T2})^2 + \cdots + (3\sigma V_{T,\mathrm{SWR/SR}})^2}. \quad (1)$$

V. SRAM VARIATION STUDY

In this section, we will discuss the Monte Carlo study of fin width variation impact on circuits with 6T SRAM cells using the small signal variation model presented in [15]. The targeted SRAM devices at 22 nm technology node must have an I_{OFF} of 10 nA/μm with gate length of 34 nm [1]. Using the calibrated devices of Section II, we simulated nominal devices with the SRAM target specifications for Si trigate (rectangular and tapered fins), UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate. An ensemble of 6T SRAM cells with increasing rms amplitude of fin width variation in Si trigate (rectangular and tapered fins), $In_{0.53}Ga_{0.47}As$ trigate, and UTB SOI were simulated at V_{CC} of 0.5 V. Table III summarizes the 3σ of read static noise margin (RSNM) values for all the devices at the three rms amplitude conditions. Si rectangular trigate SRAM cell gives least 3σ RSNM. UTB SOI SRAM cell gives comparable 3σRSNM with Si trigate.

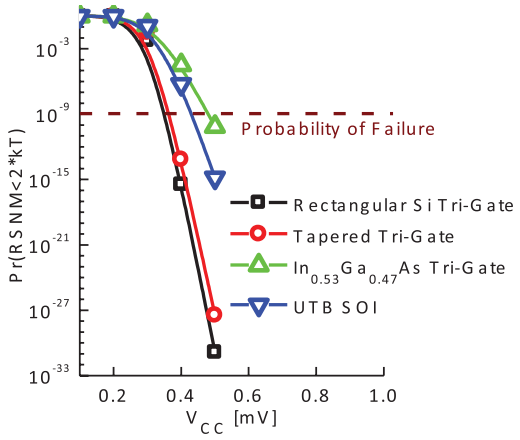

Fig. 11. Read failure probability versus supply voltage, V_{CC} for Si trigate (tapered and rectangular), UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate SRAM cells. W_{FIN} variation of rms amplitude. 1 nm is considered for all cases. Rectangular Si trigate gives V_{CCmin} below 0.4 V.

Read failure probability of an SRAM cell can be defined as the probability at which the RSNM is less than two times the thermal noise, i.e., 2 kT = 52 mV ((2) [16])

$$Pr_{\mathrm{read-failure}} = \mathrm{Pr}(\mathrm{RSNM} < 2\mathrm{kT}). \quad (2)$$

We generated 200 Monte Carlo samples of variant SRAM cells with fin width variation of $\Delta = 1$ nm at different supply voltages. Using the mean and sigma values of each of the fitted gaussian curves for RSNM we calculate the $Pr_{\mathrm{read-failure}}$. The probability that one in a billion SRAM cell will fail, i.e., $Pr_{\mathrm{read-failure}}$ = 1e-9 gives the V_{CCmin} of the SRAM cell. Fig. 11 shows the $Pr_{\mathrm{read-failure}}$ versus V_{CC} for Si trigate (tapered and rectangular), $In_{0.53}Ga_{0.47}As$ trigate, and UTB SOI 6T SRAM cells. Among all the devices considered, Si trigate is the most suitable candidate for 6T SRAM cell to give V_{CCmin} below 0.4 V. From Fig. 11, we can conclude that

six transistors are not enough to form a stable SRAM circuit with UTB SOI or $In_{0.53}Ga_{0.47}As$ trigate to operate below 0.4 V. We need higher transistor count SRAM architecture (8T or 10T) as presented in [15] to overcome this shortcoming.

VI. Conclusion

To investigate the impact of process variations, we did a 3-D numerical simulation study on Si trigate (rectangular and tapered cross section), UTB SOI, and $In_{0.53}Ga_{0.47}As$ trigate. Rectangular Si trigate shows a total ΔV_T of 13.1 mV while UTB SOI shows 24.6 mV. Between Si and III–V semiconductors, $In_{0.53}Ga_{0.47}As$ trigate shows 1.5 times less ΔV_T than Si trigate. Higher performance with controlled SWR makes $In_{0.53}Ga_{0.47}As$ trigates promising replacement for Si. 3σ RSNM for 6T SRAM cell with fin width variation is the least in Si rectangular trigate. In terms of V_{CCmin} of a 6T SRAM cell, Si trigate is the suitable candidate with V_{CCmin} below 0.4 V. To build a variation tolerant SRAM cell with UTB SOI and $In_{0.53}Ga_{0.47}As$ trigate, we need higher transistor count SRAM architecture.

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Authors' biographies and photographs not available at the time of publication.