Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States 
Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio

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Abstract: Staggered tunnel junction (GaAs\textsubscript{0.35}Sb\textsubscript{0.65} /In\textsubscript{0.7}Ga\textsubscript{0.3}As) is used to demonstrate heterojunction tunnel FET (TFET) with the highest drive current, I\textsubscript{on}, of 135\textmu A/\mu m and highest I\textsubscript{on}/I\textsubscript{off} ratio of 2.7x10\textsuperscript{4} (V\textsubscript{gs}=0.5V, V\textsubscript{off}-V\textsubscript{eff}=1.5V). Effective oxide thickness (EOT) scaling (using Al\textsubscript{2}O\textsubscript{3}/HfO\textsubscript{2} bilayer gate stack) coupled with pulsed I-V measurements (suppressing D\textsubscript{g} response) enable demonstration of steeper switching TFET.

Introduction: Mixed arsenide-antimonide based lattice-matched heterojunction provides a wide range of compositionally tunable effective tunneling barrier height (E\textsubscript{b}\textsubscript{eff}), from 0.5eV to 0eV [4,7]. With increasing Sb and As composition, E\textsubscript{b}\textsubscript{eff} reduces and TFET I\textsubscript{on} can approach MOSFET level without compromising the high I\textsubscript{on}/I\textsubscript{off} ratio [3-5]. However, engineering an abrupt change from Sb rich to As rich interface is a significant growth challenge [3]. The objectives of this work are three fold: 1) we explore proper growth switching conditions to control the atomic termination at the GaAs\textsubscript{0.3}Sb\textsubscript{0.65} /In\textsubscript{0.7}Ga\textsubscript{0.3}As interface to reduce defects and demonstrate TFET with higher I\textsubscript{on}/I\textsubscript{off} ratio than reported before [3]; 2) we demonstrate the effect of EOT scaling on TFET switching slope (SS) enhancement; 3) finally, we employ ultra-fast pulsed I-V measurement to mitigate the interface state (D\textsubscript{g}) response in order to improve the TFET SS and I\textsubscript{on}/I\textsubscript{off} ratio over a specified gate voltage (V\textsubscript{gs}) swing.

Materials Characterization: Figs. 1(a-c) show the schematic layer structures for In\textsubscript{0.7}Ga\textsubscript{0.3}As HomJ, as well as GaAs\textsubscript{1-x}Sb\textsubscript{x}/In\textsubscript{0.7}Ga\textsubscript{0.3}As Moderate and High HetJ TFETs for x=0.6,0.65 and y=0.65,0.7 respectively, grown on semi-insulating InP substrate using solid-source molecular beam epitaxy. For the High HetJ TFET structure, two wafers were grown to study the impact of (a) GaAs-like and (b) InAs-like surface termination while switching from Sb-rich GaAs\textsubscript{0.35}Sb\textsubscript{0.65} to As-rich In\textsubscript{0.7}Ga\textsubscript{0.3}As layer. For the latter case, while ramping up the As flux from 35% to 100%, 1-2 ML of Indium (In) was added prior to In\textsubscript{0.7}Ga\textsubscript{0.3}As layer. Figs. 2 (a,b) show asymmetric (115) reciprocal space maps of the High HetJ TFET structures. In both cases, the growth of the metamorphic buffer results in an In\textsubscript{0.65}Al\textsubscript{0.35}As “virtual” substrate with \geq90\% strain relaxation. However, the subsequent GaAs\textsubscript{0.35}Sb\textsubscript{0.65} and In\textsubscript{0.7}Ga\textsubscript{0.3}As active device layers differ in their strain with respect to the “virtual” substrate. With the GaAs terminated heterointerface, the active layers are strain relaxed and susceptible to defect formation, whereas the device layers on the InAs terminated interface are pseudomorphic to the In\textsubscript{0.65}Al\textsubscript{0.35}As “virtual substrate” and likely “defect-free”. This is evident in Fig. 2 (c,d) where atomic force microscopy (AFM) images reveal lower surface roughness (4.5nm) and 2D cross-hatch pattern for InAs terminated wafer compared to the GaAs terminated one (with roughness of 5.6nm and no cross-hatch pattern).

Device Characterization: The vertical TFET fabrication process is described in [4]. Fig. 1(d) shows the cross-sectional TEM micrograph of the fabricated High HetJ TFET. Figs. 2 (e,f) compare the I\textsubscript{on}-V\textsubscript{gs} and I\textsubscript{on}/V\textsubscript{off} characteristics for the High HetJ TFET with GaAs and InAs surface termination. More than 3 orders in magnitude improvement in I\textsubscript{on}/I\textsubscript{off} Ratio is achieved with the latter due to the reduction in defect assisted conduction. The improvement in heteroepitaxy with InAs termination is reflected in the improved electrostatics (smaller SS and DIBT) for the same device geometry. Figs. 1(e-i) compare the performance of the High HetJ TFET with Mod. HetJ and HomJ TFETs. First, I\textsubscript{on} progressively increases by 325% with decreasing E\textsubscript{b}\textsubscript{off} (from 0.58eV to 0.25eV) due to the increase in tunneling transmission coefficient. Second, the drain induced barrier thinning (DIBT) improves with reducing E\textsubscript{b}\textsubscript{off} due to inter-band generation occurring closer to the source/channel junction, thus improving device electrostatics [5]. The SS vs I\textsubscript{on} curve also shifts with reducing E\textsubscript{b}\textsubscript{off}, with the minimum SS occurring at higher I\textsubscript{on} which is excellent for TFET operation with MOSFET like performance. To further enhance performance, we scaled the EOT for the High HetJ TFET, from 2nm to 1.75nm, and reduced the V\textsubscript{gs} window by 0.5V for the same I\textsubscript{on} (Fig. 3a). Figs. 3(b,c) summarize the improvement in both I\textsubscript{on} (tunneling transmission) and DIBT (electrostatics) as a function of E\textsubscript{b}\textsubscript{off} and EOT. The switching slope, SS, in all fabricated devices is greater than 60mV/dec at room temperature and is caused by the presence of interface states (D\textsubscript{g}) at the high-k/channel interface [1,3-5]. We perform ultra-fast pulsed I\textsubscript{on}, V\textsubscript{gs} measurements on the HomJ TFET with input gate voltage pulses having rise time (t\textsubscript{r}) of 10ns, to suppress D\textsubscript{g} response. The TFET I\textsubscript{on} response was then reliably sampled after 150ns (t\textsubscript{meas}). The pulsed I\textsubscript{on}, V\textsubscript{gs} measurement (Figs. 4(a,b)) show marked steepening of the switching slope (SS) with minimum SS of 100mV/decade and matches the theoretical I\textsubscript{on}, V\textsubscript{gs} for D\textsubscript{g} \sim 8x10\textsuperscript{11}/cm\textsuperscript{2} [7]. The pulsed I\textsubscript{on}, V\textsubscript{gs} study allows us to accurately predict the performance realizable in High HetJ TFET with similar D\textsubscript{g} \sim 8x10\textsuperscript{11}/cm\textsuperscript{2} and EOT of 1nm (Figs. 5(a,b)). Two dimensional device simulations show that high HetJ TFET can maintain sub kT/q SS over two orders of magnitude of drain current (10\textsuperscript{9} to 10\textsuperscript{7} A/\mu m). Heterojunction Tunnel FET can deliver MOSFET-like performance with better I\textsubscript{on}/I\textsubscript{off}, making them a promising post CMOS candidate for low power, high performance applications.

Summary: Table 1 benchmarks the on current (I\textsubscript{on}), off-on ratio (I\textsubscript{on}/I\textsubscript{off}) and effective switching slope (SS\textsubscript{eff}) of TFETs, demonstrated till date. The High HetJ TFET in this work shows I\textsubscript{on} of 135\mu A/\mu m and I\textsubscript{on}/I\textsubscript{off} >4x at V\textsubscript{gs}=0.5V and V\textsubscript{off}-V\textsubscript{eff}=1.5V. This is the highest ever reported I\textsubscript{on}/I\textsubscript{off} ratio for I\textsubscript{on}> 100\mu A/\mu m in the category of TFETs.

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References
[1] Zhao et al., EDL, 2011 
**Fabrication and Electrical Characterization**

(a) HomJ TFET  
(b) Moderate HetJ TFET  
(c) High HetJ TFET

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<td>W=100µm</td>
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- **Figure 1**: (a-c) TFET layer structures. (d) High HetJ TFET cross-section TEM micrograph. (e-f) Measured Ids-Vgs, Ids-Vds and extracted switching slope (SS) vs Igs characteristics for the three fabricated devices.

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<td>Lg=150nm</td>
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**Materials Growth Improvement**

(a) GaAs terminated  
(b) InAs terminated

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**Minimizing Dit response using Fast I-V (HomJ TFET)**

- **Figure 2**: (a,b) Asymmetric (115) reciprocal space map and (c,d) 20x20 µm² atomic force microscopy image of High HetJ TFET layers for the cases with GaAs and InAs terminated hetero-interfaces; (c) Improvement in Ids-Vgs and Ids-Vds characteristics with InAs terminated hetero-interface.

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**Further EOT scaling in high HetJ TFET (Exp., Model & Projection)**

- **Figure 3**: (a) Improved Ids-Vgs characteristics of the high HetJ TFET with EOT scaling. (b,c) Summary of improvement in measured Ion and Drain Induced Barrier Thinning (DIBT) with Ebff and EOT scaling. DIBT improves with increasing stagger due to interband generation occurring closer to the source-channel interface [5].

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**Table 1**: Benchmarking Ion and Ion/Id(s) at Vds=0.5V, Ion=5nA/µm [ITRS-2010], where SS_m=|Voff-Von|/2log(Ion/Ioff)[6]

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**Figure 4**: (a) Pulsed Ids-Vgs measured on HomJ TFET showing steeper switching by avoiding slow Ds response. Inset shows simplified pulsed I-V set-up. (b) SS vs Ids showing improved SS minimum with pulsing. Inset shows Ds profile used to model DC and pulsed Ids-Vgs measurements.

- **Figure 5**: (a,b) An improvement in high-k/channel interface (Dk ~8x1011/cm²/eV) combined with further EOT scaling would enable MOSFET-like TFET operation at low Vcc with higher Ion/Ioff ratio.