Asymmetric Tunnel Field-Effect Transistors as Frequency Multipliers

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***Abstract*—This letter proposes a novel application of asymmetric (double-gate) tunnel field-effect transistors (asymmetric TFETs) as a frequency multiplier. Work-function tuning of an asymmetric TFET was used to demonstrate symmetric ambipolar transfer characteristics by TCAD simulation. Unlike the conventional balanced FET-based multiplier, the asymmetric TFET design needs only one transistor for rejecting odd harmonics. Advanced design system simulations are used to compare the performance of an n-type FET and an asymmetric TFET frequency multiplier.**

***Index Terms*—Ambipolar TFET, asymmetric TFET, band-to-band tunneling, frequency multiplier, mixer.**

I. Introduction

THE availability of a stable distortion-free RF local source is the inherent upper limit of operating frequency in microwave and millimeter-wave applications. The lack of high-power, high-frequency, and compact frequency sources makes a frequency multiplier in conjunction with reliable low-frequency crystal oscillators a potential candidate for the RF local source. Diodes, RF MOSFETs, and high-electron mobility transistors are the obvious choice for the design of a frequency multiplier circuit. However, the operation of these devices in the nonlinear regime not only gives the desired frequency multiplication but also results in high-order harmonic distortion to the system. These unwanted harmonics and their subsequent mixing are of great concern as the order of cascade stages in multipliers is increased. For a single-ended multiplier topology, a filtering and matching circuit is added to reject the unwanted harmonic components. This limits the multiplier to a narrow-band frequency operation. Traditionally, balanced multiplier designs are used to reject odd harmonics by mixing out-of-phase signals from two or more individual single-ended mixers. Recently, mixer applications of graphene-based FETs have generated a lot of interest due to their inherent ambipolar transfer characteristics [1]. Here, the ambipolar characteristics essentially eliminate the odd harmonic components in the output.

The sub-K_BT/q switching slope makes TFETs an attractive design for low-voltage logic application. Recently, [2] has demonstrated record ON-current characteristics using vertical heterojunction TFETs. Here, we explore the analog application of a TFET. The drain-side doping in a TFET dictates the ambipolar leakage in its transfer characteristics [see Fig. 1(c)]. For logic application, the drain doping is limited to avoid and limit the ambipolar leakage current. By increasing the drain-side doping, one can essentially increase the reverse leakage and obtain near-symmetric transfer characteristics. However, for significant frequency multiplication, the turn-on voltage of the reverse ambipolar conduction branch and the forward current characteristics need to be independently tuned. Here, we propose a dual-work-function (WF) asymmetric TFET to obtain ideal ambipolar transfer characteristics for mixer application.

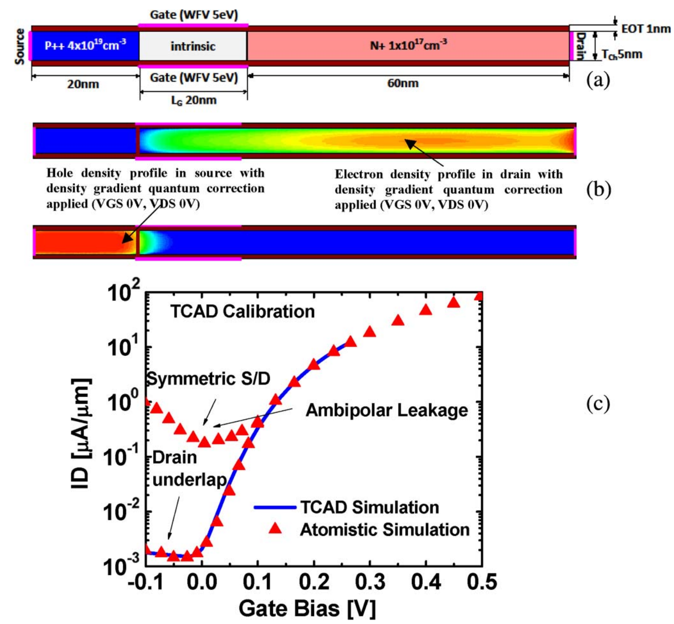

Fig. 1. (a) Schematic of an InAs homojunction DG TFET. (b) Contour plot showing the electron and hole densities in the device for $V_{gs} = 0$ V and $V_{ds} = 0$ V. (c) TCAD transfer characteristic simulation compared with atomistic simulation showing a very good match.

II. TCAD Simulation

In this letter, we have employed a Sentaurus TCAD simulator for the device simulation. Fig. 1(a) shows the schematic of an InAs homojunction dual-gate (DG) TFET. The DG TFET structure shown here is similar to that in [3], where the drain region is lightly doped with 1×10^{17} cm^{-3} n-dopants in order to reduce the strong leakage current resulting from drain-side tunneling at negative gate bias. Fig. 1(b) shows the electron and hole density profiles in the DG TFET obtained from TCAD simulations under neutral conditions (gate and drain biases of 0 V). The electrons and holes in this ultrathin-body DG TFET are heavily quantized, and quantum correction is applied in our TCAD simulations using the density-gradient correction model, as shown in Fig. 1(b). Fig. 1(c) shows the calibration of the DG

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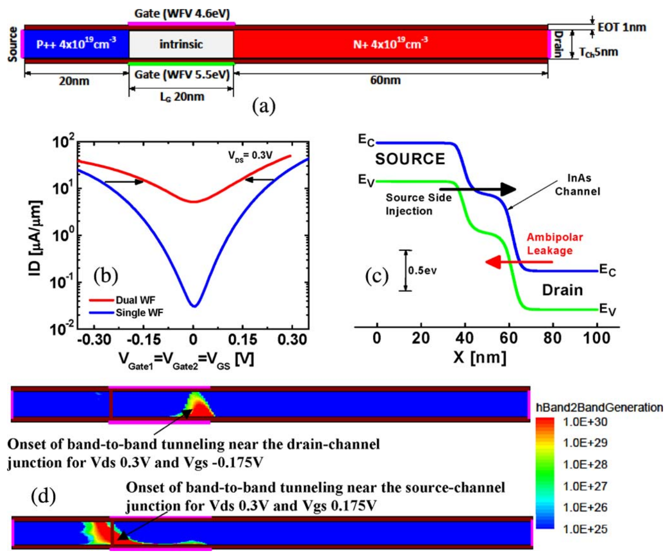

Fig. 2. (a) Schematic of a dual-WF InAs homojunction TFET. (b) Transfer characteristics showing ambipolar transfer characteristics by using a dual-WF TFET. (c) Band diagram across the channel showing the source-side and ambipolar leakage tunneling regions. (d) Contour plots showing band-to-band tunneling at the source–channel and drain–channel junctions for positive and negative gate biases, respectively.

TFET TCAD model with the atomistic non-equilibrium Greens function (NEGF) simulations from [3]. The TCAD simulation uses a nonlocal band-to-band tunneling model based on Kane's two-band dispersion (prefactor $A = 2 \times 10^{20}$ $\mathrm{cm^{-3} \cdot s^{-1}}$ and exponential factor $B = 2.24 \times 10^6$ V/cm) and shows good agreement with the atomistic NEGF simulation.

Fig. 2(a) shows the schematic of a dual-WF TFET. As compared with the design in Fig. 1(a), the WF of the two gates of the TFET is different, and the drain is heavily n-doped (4×10^{19} $\mathrm{cm^{-3}}$) so that the drain-side tunneling current becomes significant. Fig. 2(b) compares the I_d–V_g characteristics of dual- and single-WF TFETs (both with heavily doped drain regions) for an applied drain bias of 0.3 V. The use of dual-WF values causes the turned-on regions of the I_d–V_g of the single-WF TFET to shift, as shown in Fig. 2(b), thereby causing the early onset of tunneling for both positive and negative V_g in the dual-WF TFET. The parabolic shape of the I_d–V_g resulting from the use of dual WFs can be used for analog mixer application as described later. Fig. 2(c) shows the band diagram of the TFET showing the source- and drain-side tunneling regions. Fig. 2(d) shows the onset of tunneling (band-to-band generation rate of holes) for positive and negative gate biases in the dual-WF TFET.

III. Nonlinear Distortion

Fig. 3 shows the transfer characteristics for a 32-nm-gate-length ambipolar TFET and an nMOS transistor. For low frequencies, output current i_D can be expressed by power-series expansion in terms of gate bias v_G as

$$i_D = g_{m0} + g_{m1} v_G + g_{m2} v_G^2 + g_{m3} v_G^3 + g_{m4} v_G^4 + \cdots.$$

The proportionality coefficient of the power series is

$$g_{mn} = \frac{1}{n!} \frac{d^n I_D}{d V_G^n}.$$

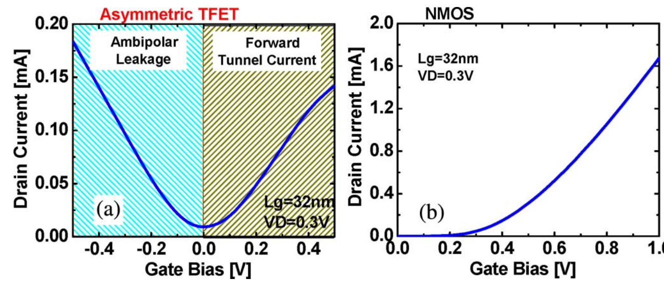

Fig. 3. Transfer characteristics of the (a) asymmetric TFET and (b) nMOS transistor biased at $V_d = 0.3$ V.

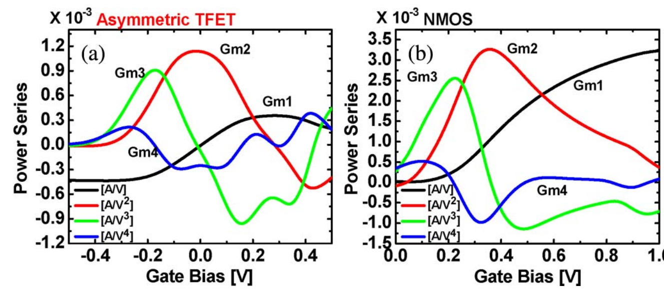

Fig. 4. Power-series components of the transfer characteristics of the (a) asymmetric TFET and (b) nMOS transistor. One can clearly see that, in the case of a TFET, at zero bias, the odd harmonics are zero.

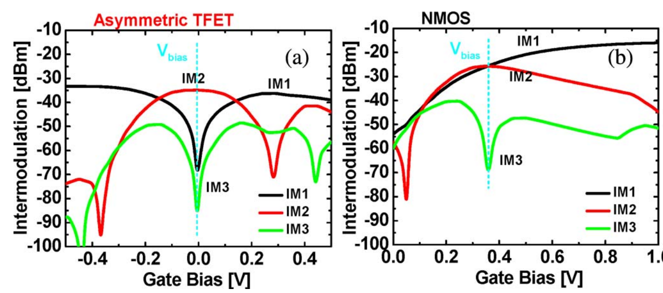

Fig. 5. Output intermodulation component of the (a) asymmetric TFET and (b) nMOS transistor for a 0-dBm input signal.

The g_{m0} component represents the dc component; g_{m1} is the linear component, whereas g_{m2}, g_{m3}, and g_{m4} represent the second-, third-, and fourth-order distortion terms, respectively. Fig. 4 shows the power-series components for the transfer characteristics shown in Fig. 3. For a TFET, the vanishing of g_{m1} and g_{m3} and the maxima of g_{m2} at the minimum conduction point give the maximum conversion gain and rejection of the odd harmonics.

For a sinusoidal input $v_G = v_0 \sin(\omega t)$, the fundamental frequency component of the current output is given as $i_{\mathrm{fun}} = g_{m1} v_0 + (3/4) g_{m3} v_0^3$. The second- and third-order harmonic components are given as $i_2 = g_{m2} v_0^2$ and $i_3 = (3/4) g_{m3} v_0^3$, respectively. Fig. 5 shows the intermodulation component for a 0-dBm RF input. For an asymmetric TFET, all the odd harmonic components are null at zero gate bias ($g_{m1}, g_{m3} = 0$). In the case of an nMOS, we can bias the transistor only for the selective null harmonic component, which still leaves a significant amount of harmonic distortion in the system. Hence, the design of an nMOS frequency multiplier will still mandate the need for a narrow-band filter or a balance design configuration. On the other hand, the absence of odd harmonics essentially enables designers to use an asymmetric TFET in a single-ended wideband configuration or in a cascade design.

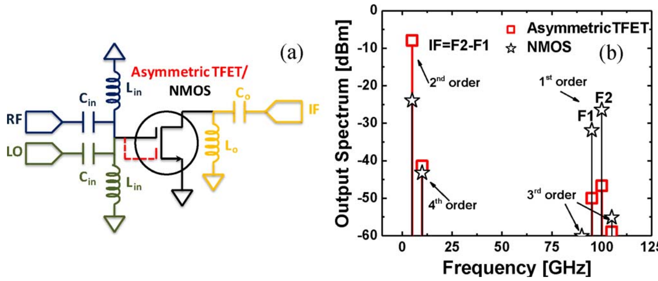

Fig. 6. (a) Schematic of a mixer using an asymmetric TFET/nMOS. (b) Output spectrum of the mixer with the TFET/nMOS biased at $V_g = 0\ \mathrm{V}/0.35\ \mathrm{V}$. The output is simulated using an ADS simulator with small-signal parameters obtained from TCAD simulations.

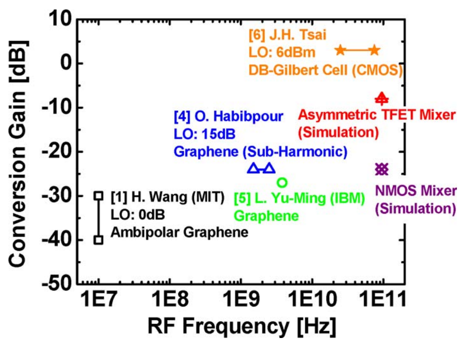

Fig. 7. Comparison of the conversion gain versus RF frequency for the fabricated graphene [1], [4], [5], CMOS [6], and simulated asymmetric TFET mixers.

Small-signal parameters were obtained for both an asymmetric TFET and an nMOS from mixed-mode TCAD simulation. These parameters were used to model a high-frequency mixer in an Agilent advanced design system (ADS) simulator. The biasing of a TFET at the minimum conduction point places it in a region of low C_{gs} and C_{gd} contribution and hence avoids the penalty due to high Miller capacitance. The circuit-level schematic of the harmonic balance simulation is shown in Fig. 6(a). The current gain was modeled as a nonlinear voltage-controlled current source. The nonlinear terms for the current source were evaluated by polynomial fitting of the transfer characteristics at the bias points. The bias point is at the null point for the third-order harmonics in both cases (marked in Fig. 5).

For the mixer simulation, a local oscillator (LO) frequency of 100 GHz is mixed with a 95-GHz RF frequency. Fig. 6(b) shows the output spectrum of the mixer from the harmonic balance simulation. The clear difference in the two cases can be seen in the reduced output at the funddamental frequency for the asymmetric TFET. This confirms that, for an asymmetric TFET, all the odd harmonics at the mixer output are rejected.

Fig. 7 shows the comparison of the asymmetric TFET conversion gain with the fabricated graphene and CMOS mixers. The graphene transistor is a promising candidate for ambipolar mixers. The current state-of-the-art graphene mixer still suffers from high density of interface states at the graphene high-κ interface and large contact resistance, leading to degraded performance. In addition, the bulk disorder and edge states in graphene influence the minimum conductivity of a graphene FET. Since they are biased at the Dirac point (minimum conductivity point) for the ambipolar mixing, the conversion gain will be significantly influenced by these defects. While graphene-based mixers have significant potential to improve in the future, III–V-based asymmetric TFET RF mixers offer an attractive alternative and could be incorporated into a III–V-based system-on-a-chip configuration. On the other hand, the double-balanced (DB) Gilbert cell needs a ten-transistor configuration (100$\times$ higher area) to achieve such a high conversion gain. Increasing the TFET transistor width and band-gap engineering of the tunnel junction will further increase the conversion gain.

IV. Challenges

The main challenges in implementation of an asymmetric TFET as a frequency multiplier are WF engineering and overcoming interface state density D_{it} at the oxide and semiconductor interface. For a symmetric forward current branch and reverse ambipolar leakage, it is essential to be able to fine-tune the WF independently. Lack of symmetry will degrade the conversion gain and would result in nonzero odd-order harmonics at the minimum conduction point. Furthermore, a practical design (gate WF < 5 eV) will have a dc shift and would require a negative dc bias to operate the mixer at the minimum conduction point. D_{it} at the oxide interface will degrade g_{m1} and, in turn, the conversion gain.

V. Conclusion

In summary, we have proposed an asymmetric TFET model with ambipolar transfer characteristics. Symmetric ambipolar I_d–V_g transfer characteristics were obtained by tuning the WF of the two gates independently. The study of the nonlinear components shows the elimination of odd intermodulation terms in the output. Mixer simulation by ADS confirms the absence of odd harmonics in the output spectrum.

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