Compressively Strained InSb MOSFETs with High Hole Mobility for P-Channel Application

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Antimonide based (Sb) compound semiconductors are promising for complementary logic applications due to their advantageous electron and hole transport properties. Ultra-thin device layers of compressively strained InSb are of particular interest for p-channel MOSFETs due to their reduced hole transport mass and higher mobility compared to strained InGaSb quantum well (QW) two dimensional hole gas (2DHG) and Si inversion layers (Fig. 1). Schottky gated p-channel 1.9% strained InSb QW-FETs have been previously demonstrated [1]. High gate leakage through the Schottky gate results in high power dissipation and limits the ON-state performance. The natural evolution is to integrate a high-k insulator between the gate electrode and InSb channel to reduce the gate leakage, while preserving the superior hole transport properties. Sb-based materials are particularly reactive in atmosphere resulting in poor high-k dielectric/antimonide interface. In this work, we demonstrate a high mobility p-channel strained InSb pMOSFET with 5 nm Al_2O_3 high-k dielectric integrated using a composite InP/ $Al_{0.35}In_{0.65}Sb$ barrier.

Fig. 2 (a) shows the schematic of the strained InSb MOSFET with composite InP/ $Al_{0.35}In_{0.65}Sb$ barrier. The p++ $Ga_{0.5}$ $In_{0.5}Sb$ layer was incorporated to reduce the source/drain series resistance. Shown in Fig. 2 (b), (c) are the TEM cross-sectional micrograph of the gated region and energy band diagram of the 5 nm thick compressively strained InSb QW simulated using 6-band k.p Schrodinger-Poisson self-consistent solver. Compressive strain in the quantum well results in splitting of HH-LH bands, reduction of in-plane transport effective mass. As shown in Figs. 3-4 an effective mass of $m^*=0.08m_o$ was extracted using Shubnikov-de Haas measurements. Figs. 5-6 show the experimental and modeled Hall measurement results on strained InSb/$Al_{0.35}In_{0.65}Sb$ quantum well heterostructure. Scattering analysis using Relaxation Time Approximation (RTA) [4] formalism is performed to analyze the temperature dependent experimental hole transport. The analysis indicates the dominance of polar optical phonon scattering at room temperature and interface roughness scattering limiting mobility at T=20K. Hole density modeling as function of temperature shown in Fig.5 indicates major contribution from 1st subband in strained InSb QW from 20K-300K, along with less than 10% contribution from the $Al_{0.35}In_{0.65}Sb$ buffer at room temperature. High hole mobility of 680 cm^2/Vs in the QW was obtained at a hole sheet density of $5x10^{12}$ /cm^2 at 300K. At 150K and 77K, hole mobilities of 2,500 cm^2/Vs and 4,500 cm^2/Vs were obtained at carrier densities of $2.3x10^{12}$ /cm^2 and $2.0x10^{12}$ /cm^2 ,respectively, indicating superior transport.

The InSb p-channel MOSFET was fabricated using Pd/Pt/Au alloyed source/drain contacts, followed by a selective recess etch of the $Ga_{0.5}$ $In_{0.5}Sb$ layer. Plasma Enhanced Atomic Layer Deposition (PEALD) at 200℃ was used to deposit 5 nm of Al_2O_3 on the exposed InP barrier yielding an equivalent oxide thickness, EOT, of 5.4 nm. The fabrication process flow is detailed in Fig.8. Circular TLM measurements after PEALD Al_2O_3 deposition and Forming Gas Anneal (FGA) yielded a contact resistance of 1300 Ω-µm (Fig. 9). Fig. 10 shows the measured and corrected for D_{it} [5] split CV characteristics at various temperatures for InSb QW-MOSFET with 5 nm Al_2O_3 and composite InP/$Al_{0.35}In_{0.65}Sb$ barrier. The poor CV modulation at 300K is indicative of high density of traps within the bandgap of InP/$Al_{0.35}In_{0.65}Sb$. As the temperature is decreased, the trap response in the depletion region is significantly slowed, essentially causing freeze out. The reduced contribution of traps results in improved CV modulation at T=150 and 77K.

Fig. 8 shows the transistor drain current I_D-V_G characteristics for an L_G =5 µm InSb QW-MOSFET with PEALD Al_2O_3. The transistor exhibits an I_{ON} (V_G= V_T +0.5V) of 2.0 µA/µm, a peak G_m of 6.8 µS/µm and a SS of 58 mV/dec at T=77K. Fig. 9 shows the transistor drain current I_D-V_G characteristics for an L_G =5 µm InSb QW-MOSFET as a function of temperature. At T=300K the parallel conduction from the buffer limits the I_{ON}/I_{OFF} ratio. As temperature is decreased, the contribution of parallel conduction is reduced, the I_{ON}/I_{OFF} ratio improves from 100 at T=150K to over 10^4 at T=77K. Fig. 10 shows the experimentally extracted maximum effective hole mobility as a function of carrier density after correcting for series resistance [6]. The peak effective hole mobility was 2,000 cm^2/(Vs) and 1,000 cm^2/(Vs) for T=77K and T=150K.

Conclusion: We demonstrate synthesis of p-channel InSb MOSFET with 1.9% compressive biaxial strain with outstanding room temperature and 150K Hall mobility of 680 cm^2/Vs and 2,500 cm^2/Vs at hole sheet density of $5x10^{12}$ /cm^2 and $2.3x10^{12}$ /cm^2, respectively. The incorporation of an InP layer on top of $Al_{0.35}In_{0.65}Sb$ barrier allows for integration of a high-k dielectric and demonstration of InSb pMOSFET with significantly reduced gate leakage. Parallel conduction limits the on-off ratio of the InSb MOSFET above 150K. Refinement of the InP barrier to reduce interface states and buffer layer to reduce parallel conduction is expected to improve InSb pMOSFET characteristics at 300K.

References: [1] M. Radosavljevic, *IEDM Technical Digest IEEE International Electron Devices Meeting*, 2008. [2] Z. Yuan *VLSI Technology (VLSIT), 2012 Symposium on, 2012* [3] R. Pillarisetty, *IEEE International Electron Devices Meeting*, 2010. [4] A. Agrawal *Device Research Conference*, pp.27–28, 2011. [5] A.Ali *IEEE Trans. Electron Devices,* vol.58, no. 5, pp.1397-1403, 2011 [6] E. Simoen *Solid-State Electronics*, vol. 41, no. 4, pp. 659–661, Apr. 1997.

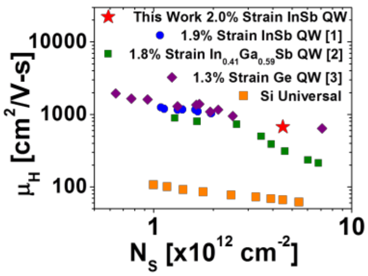
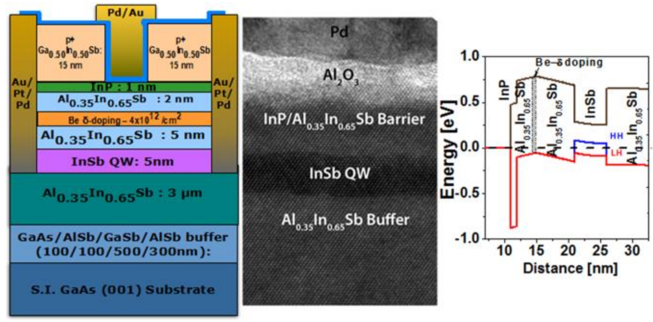


Fig.1: Hall hole mobility versus hole sheet density at T=300K for Si, Ge, QW, InGaSb, and InSb QWs heterostructures.



a. b. c.

Fig.2: (a) Schematic of InSb QW-MOSFET on S.I. GaAs substrate with 5nm PEALD Al_2O_3 (b) Cross-sectional TEM micrograph on InSb- MOSFET gated region (c) Energy band diagram of the quantum well hetorstructure. Simulated using 6-band k.p Schrodinger-Poisson self-consistent solver.

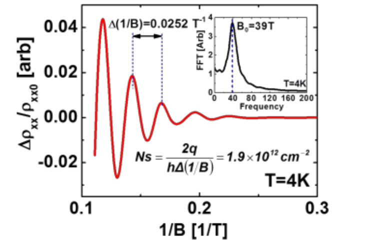


Fig.3: **Shubnikov-de Haas oscillations in sheet resistance as a function of 1/B at T=4 K, inset shows FFT of the oscillations showing single frequency peak at 39 T, indicating that only one hh subband is occupied at this sheet charge.**

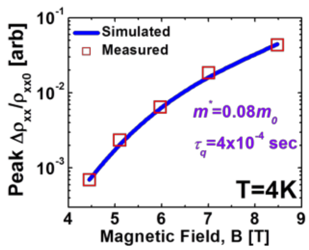


Fig.4: **Modeled and experimental peak $\Delta\rho_{xx}/\rho_{xx0}$ as a function of magnetic field used to extract the effective mass and quantum lifetime for the InSb QW heterostructure.**

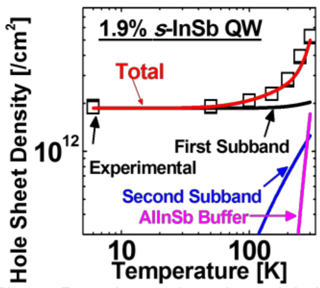


Fig.5: Experimental and modeled hole sheet density as a function of temperature for InSb QW heterostructure. Showing contributions from first and second lh subband and AlInSb buffer layer conduction at room temperature.

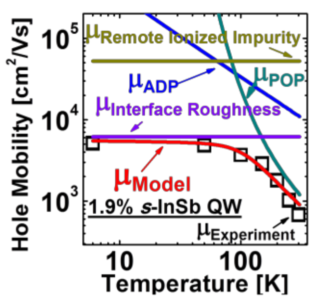


Fig 6: Experimental and modeled hole hall mobility as a function of temperature for InSb QW heterostructure.

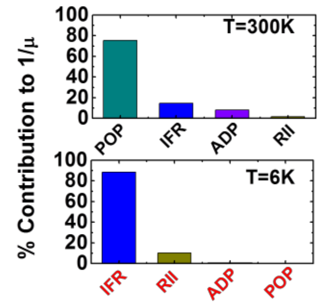


Fig.7: Pareto plot showing % contribution and dominant scattering mechanisms at T=300K and T=6K.

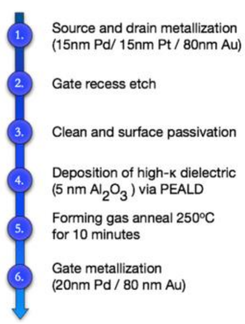


Fig.8: Fabrication process flow for InSb QW-MOSFET.

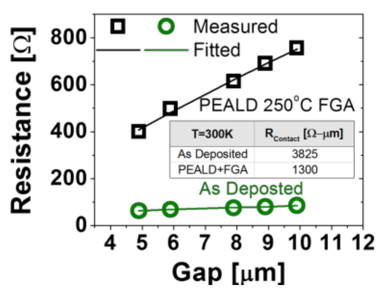


Fig.9: Circular TLM measurements following contact deposition, after PEALD Al_2O_3 deposition and FGA.

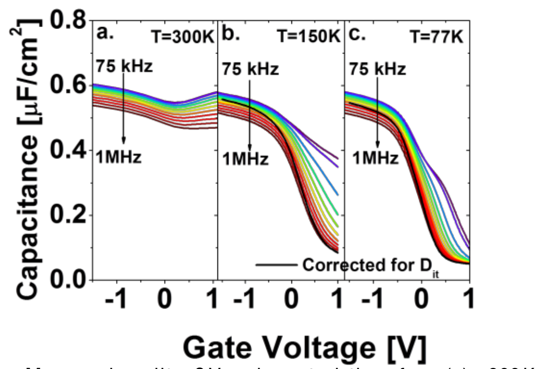
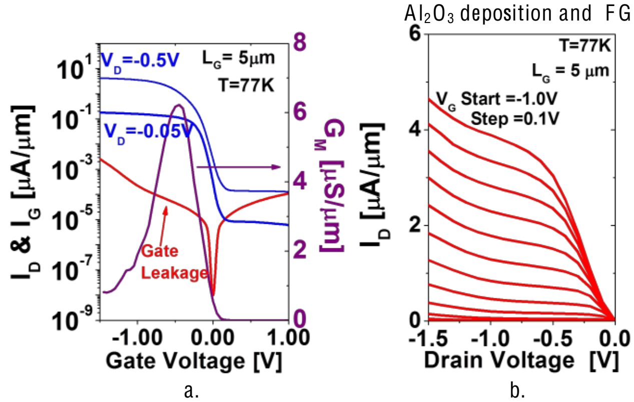


Fig.10: Measured split CV characteristics for (a) 300K. Measured split CV and corrected for D_{it} split CV characteristics for (b) 150K , and (c) 77K.



a. b.

Fig.11: (a) I_D-V_G characteristics for L_G =**5 μm InSb QW-**MOSFET at T=77K. The device exhibits I_{ON} **of 2.0 μA/μm, a peak** G_{mSat} of 6.8 **μS/μm and a** SS of 58 mV/dec. (b) I_D-V_D characteristics for L_G =**5 μm** InSb QW-MOSFET at T=77K

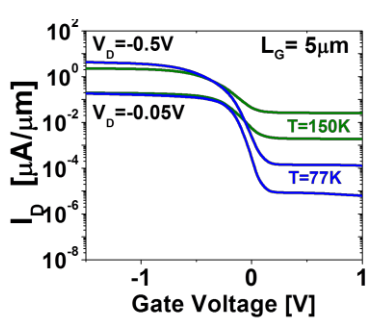


Fig12: I_D-V_G characteristics for L_G =5 **μm InSb QW-**MOSFET as a function of temperature for V_D=-50mV and V_D=-0.5V.

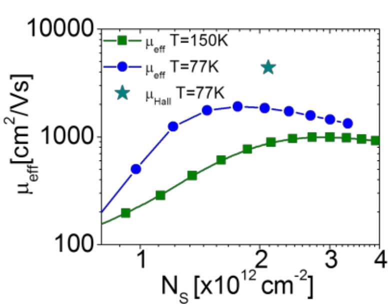


Fig.13: Extracted effective mobility as a function of carrier density at T=77K and T=150K compared with Hall mobility at 77K.