Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors

Lu Liu, *Student Member, IEEE*, Dheeraj Mohata, *Student Member, IEEE*, and Suman Datta, *Senior Member, IEEE*

***Abstract*—A scaling theory of double-gate interband tunnel field-effect transistors (TFETs) using a physics-based 2-D analytical model is presented. Ignoring the mobile charge in the channel, the electrostatic potential profile and electric field are analytically solved, and the current is calculated by integrating the band-to-band tunneling generation rate over the volume of the device. The analytical model has excellent agreement with the numerical results obtained from a commercial simulator and atomistic nonequilibrium Green function simulations for both heterojunction and homojunction TFETs. The analytical model allows us to quantitatively extract the electrostatic scaling lengths in TFETs and compare the short-channel effect of TFETs with that of MOSFETs. We conclude that double-gate TFETs exhibit superior short-channel performance than their MOSFETs counterparts at a longer gate length (greater than four times the scaling length), but the scalability of the TFETs degrades at a faster rate than MOSFETs do at smaller gate lengths (less than four times the scaling length).**

***Index Terms*—Analytical model, drain-induced barrier lowering (DIBL), drain-induced barrier thinning (DIBT), scalability, short-channel effect, tunnel field-effect transistor (TFET).**

I. Introduction

TUNNEL FIELD-EFFECT TRANSISTORS (TFETs) are ultralow-power devices that have attracted a lot of interests in recent years [1]–[4]. TFETs, in principle, can exhibit sub-kT/q subthreshold slope near OFF-state, which may achieve a higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio with the reduced gate voltage range. Numerical simulations of TFETs using nonlocal interband tunneling model capture the transfer characteristics of TFETs [1], [2], [5]. However, a physics-based analytical study of TFET is essential toward the understanding of the device operation and its immunity to short-channel effects. Numerical simulations of TFETs not only are time consuming but also frequently suffer from convergence issues. The analytical model not only boosts the computation efficiency but also provides us with a generalized scaling theory for interband TFETs, enabling a better understanding of the physical design space of TFETs. While a limited number of 1-D analytical calculations have been reported to date, the influence of drain bias on the transistor transfer characteristics has not been included in these models [6], [7]. In this letter, we present a 2-D analytical model of ultrathin-body double-gate TFETs taking into consideration the influence of the drain bias. This view stems from a 2-D analytical electrostatic study and Kane's tunneling calculation formalism adopting Flietner's $E(k)$ for the vicinity of the forbidden gap of a III–V semiconductors. Based on the analytical model, we compare the short-channel effect of TFETs with that of MOSFETs.

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The authors are with the Department of Electrical Engineering, Pennsylvania State University, University Park, PA 16802 USA (e-mail: lul137@psu.edu; dkm154@psu.edu; sdatta@engr.psu.edu).

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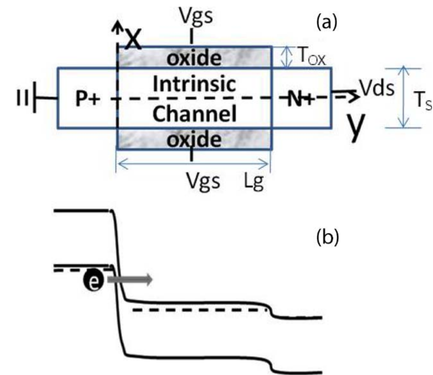

Fig. 1. (a) $x-y$ coordinate system and schematic of a double-gate TFET with symmetric-gate work function ($T_s = 10$ nm; $T_{\mathrm{ox}} = 6$ nm, $\varepsilon_{\mathrm{ox}} = 9$). (b) Illustration of gate-induced BTBT in a TFET.

II. Analytical Model

The typical structure of a double-gate TFET, along with the relevant coordinate system, is shown in Fig. 1(a). The working principle of the TFET is that the onset of current conduction is triggered by interband tunneling of electrons originating in the source region from the occupied valence-band states to the unoccupied conduction-band states in the channel region, as shown in Fig. 1(b). In this letter, an accurate analytical approach is used to solve for eigenvalues λ_n to determine the 2-D potential profile $\psi(x,y)$. Since the mobile charge term in the Poisson equation is negligible in the subthreshold operation, the equation becomes

$$\frac{\partial}{\partial x}\left(\varepsilon\frac{\partial}{\partial x}\varphi\right)+\frac{\partial}{\partial y}\left(\varepsilon\frac{\partial}{\partial y}\varphi\right)=0. \tag{1}$$

ε is the material dielectric constant, and φ is the electrostatic potential. Unlike the MOSFET structure, the source boundary condition in a TFET is $\varphi(x,0)=V_S-\varphi_{\mathrm{SC}}$, in which φ_{SC} is the work function difference between the source and the

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channel. According to [8], the solution of the Poisson equation in a symmetric double-gate MOSFET is written as

$$\varphi(x,y) = v(x) + u_L(x,y) + u_R(x,y) \tag{2}$$

$$v(x) = V_g - \phi_{\mathrm{GS}} \tag{3}$$

where ϕ_{GS} is the built-in voltage between the gate metal and the channel semiconductor, i.e.,

$$u_L = \sum_{n=1}^{\infty} u_{\mathrm{Ln}}(x,y) = \sum_{n=1}^{\infty} b_n \frac{\sinh(\pi(L_G - y)/\lambda_n)}{\sinh(\pi L_G/\lambda_n)} \sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n}\right) \tag{4}$$

$$u_R = \sum_{n=1}^{\infty} u_{\mathrm{Rn}}(x,y) = \sum_{n=1}^{\infty} c_n \frac{\sinh(\pi y/\lambda_n)}{\sinh(\pi L_G/\lambda_n)} \sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n}\right). \tag{5}$$

$u_L(u_R)$ is the potential solution as a summation of eigenfunctions $u_{\mathrm{Ln}}(u_{\mathrm{Rn}})$ with the source (drain) boundary condition and zero boundary condition at the gate and the drain (source). L_G is the gate length. Coefficients b_n and c_n in (4) and (5) are solved with a series of conjugate functions $g_n(x,y)$ and $h_n(x,y)$ introduced in [8]. For the symmetric double-gate MOSFET case, the even order eigenfunctions vanish [8]. Eigenvalues λ_n are solved from

$$\varepsilon_s \tan\left(\frac{\pi T_{\mathrm{ox}}}{\lambda_n}\right) = \varepsilon_{\mathrm{ox}} \tan\left(\frac{n\pi}{2} - \frac{\pi T_s}{2\lambda_n}\right). \tag{6}$$

T_s is the semiconductor body thickness, and T_{ox} is the oxide thickness. λ_1 is a natural length of this structure and reflects the scalability of the MOSFET. λ_1/π is approximated as the scaling length in Suzuki's discussion on double-gate MOSFETs [9], i.e.,

$$\lambda_1/\pi \approx \sqrt{\frac{\varepsilon_s}{2\varepsilon_{\mathrm{ox}}}\left(1 + \frac{\varepsilon_{\mathrm{ox}} T_s}{4\varepsilon_s T_{\mathrm{ox}}}\right) T_s T_{\mathrm{ox}}}. \tag{7}$$

For transport calculations, in our analytical model, we treat nonlocal band-to-band tunneling (BTBT) using a 3-D transmission coefficient based on Kane's calculation formalism [equivalent to Wentzel–Kramers–Brillouin (WKB)] adopting Flietner's two-band dispersion. This BTBT model has shown excellent agreement with quantum transport calculations in InGaAs and InAs [10]. In this analytical modeling part, we will take a $\mathrm{In_{0.53}Ga_{0.47}As}$ homojunction TFET for calculation. In the next part, different material systems and heterojunction TFETs will be discussed. The BTBT probability is determined by the wave vector $k(E(y))$ in the tunneling trajectory though the band gap, which has strong electric-field dependence. Using Flietner's two-band $E(k)$ [13] shown in Fig. 2, i.e.,

$$\frac{\hbar^2 k^2}{2m_C^*} = \frac{E(E/E_g - 1)}{(1 - \alpha + \alpha(E/E_g))^2} \tag{8}$$

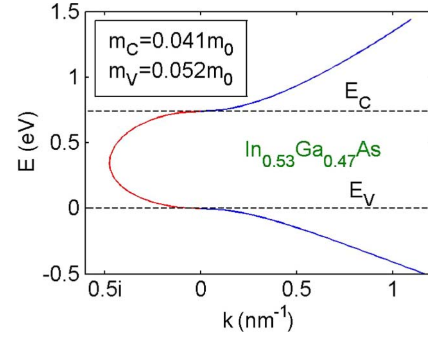

Fig. 2. Flietner's two-band $E(k)$ that is used in this analytical model.

in which

$$\alpha = 1 - \sqrt{m_C^*/m_V^*}. \tag{9}$$

This imaginary band structure is in agreement with the sp3s $*$ d5 tight-binding model [11].

The 1-D tunneling probability is

$$T(E) = C \times \exp\left\{-2\int_{y_i}^{y_f} \mathrm{Im}\left[k\left(E(y)\right)\right] \cdot dy\right\} = C \times \exp\left\{-\frac{\pi\left(2m_C^*\right)^{1/2}}{q\hbar\left[1+\left(m_C^*/m_V^*\right)^{1/4}\right]^2} \times \frac{E_g^{3/2}}{F}\right\} \tag{10}$$

in which C may vary according to different approximations ($C = 1$ for WKB and $C = \pi^2/9$ in Kane [10]).

According to Kane's formalism to calculate the 3-D tunneling rate and the carrier generation rate from the 1-D tunneling probability [12], for $\varphi(x,y) \geq \varphi(x,0) + E_g/q$, the interband tunneling generation rate is expressed as

$$G(x,y) = A\overline{F}^D/\sqrt{E_g}\exp\left(-BE_g^{3/2}/\overline{F}\right). \tag{11}$$

Otherwise

$$G(x,y) = 0 \tag{12}$$

where $A = 6.38 \times 10^{14}\ \mathrm{c(kg)^{0.5}J^{-2}s^{-2}}$, $B = \pi(2m_C^*)^{1/2}/\{q\hbar[1 + (m_C^*/m_V^*)^{1/4}]^2\} = 1.6 \times 10^{37}\ \mathrm{kg^{0.5}J^{-1}s^{-1}}$, and the integration factor $D = 2$ [13].

The electric field $\overline{F}$ in (11) is regarded as the average parallel electric field along the tunneling trajectory. For an ultrathin-body double-gate TFET with the symmetric-gate work function, the tunneling trajectory is nearly parallel to y-axis, and $\overline{F}$ is approximated as

$$\overline{F}(x,y) = \frac{\int_0^y -\frac{\partial\varphi(x,y')}{\partial y'}dy'}{y}. \tag{13}$$

In MOSFETs, the influence of the drain bias on the electrostatic potential barrier at the source/channel junction determines the subthreshold current. In TFETs, the influence of the drain bias on the electric field at the source/channel tunnel junction determines the tunneling current. The first-order eigenfunction typically works well to capture the electrostatics in the

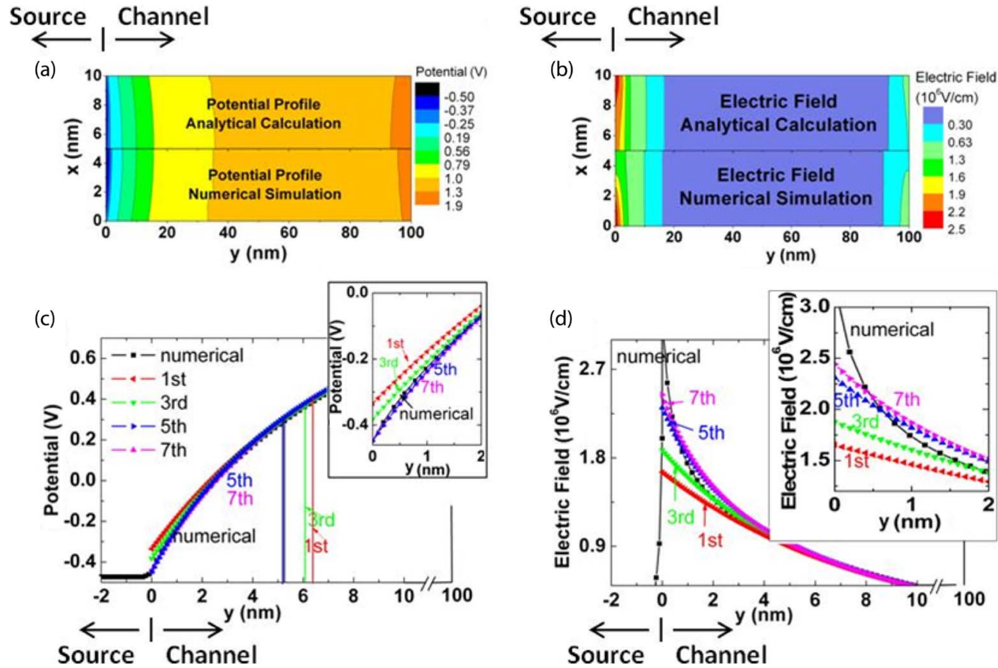

Fig. 3. Analytical calculation and numerical simulation of 2-D (a) electrostatic-potential and (b) electric-field profile in the TFET channel. In the TFET, $T_S = 10$ nm, $T_{\mathrm{OX}} = 6$ nm, $\varepsilon_S = 14$, $\varepsilon_{\mathrm{OX}} = 9$, and there is no gate–source or gate–drain overlap/underlap. (c) The electrostatic potential and (d) the electric field (y-component) near the source/channel junction at $x = 0.1$ nm, and the numerical simulation versus the analytical calculation truncating the eigenvalue solution series at the first, third, fifth, seventh orders are plotted. The vertical lines in (d) indicate the distance at which the potential changes by E_g/q. The 23% and 16% errors occur if the solution is truncated at the first and third terms, respectively, whereas the error is less than 1% if the solution is truncated at the fifth and seventh terms.

channel region away from the source/channel and drain/channel junctions. Thus, the first-order eigenfunction solution works well to describe the short-channel electrostatics in MOSFETs. However, the higher order terms become relevant in order to capture the sharp potential variation at the source/channel boundary, which directly affects the electric field. The electric field at the source/channel boundary, in turn, strongly influences the TFETs short-channel effects. In Fig. 3, analytical solutions considering the first-, third-, fifth-, and seventh-order terms in (2)–(5) are compared with those from the numerical solution of the 2-D Poisson equation for a TFET. It is evident that the terms up to the fifth order must be included to correctly estimate the average electric field (x, y) for the shortest tunneling trajectory with the E_G/q potential change, near the source/channel junction in a TFET. The point where the potential changes by E_G/q is significant because it is here that the electrons are able to quantum–mechanically tunnel from the valence band of the source to the conduction band of channel, resulting in electron-and-hole pair generation. In other words, the electrons can only generate at a point where the electrostatic potential drops by an amount equal or greater than E_g/q. If the analytical solution is truncated at the first and third terms, the error would be 23% and 16%, whereas the accuracy is much improved to error less than 1% with retaining the fifth term, particularly near the source junction. Fig. 3(a) and (b) shows the 2-D electrostatic potential profile and the electric-field profile in the channel region of the double-gate TFET under gate and drain biases of $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1$ V, providing excellent agreement of the analytical model with the numerical simulation. We use the simulation result from OMEN (Purdue University), which is a ballistic, multidimensional, atomistic, and full-band quantum simulator [14], and Sentaurus [15] to verify our analytical calculation. In OMEN, the Schrödinger equations are solved in a nearest-neighbor tight-binding basis using an efficient wave function approach equivalent to the popular nonequilibrium Green function (NEGF) formalism. The nonlocal tunneling model using dynamic mesh is used in Sentaurus. Fig. 4(b) shows the I_d–V_g characteristic of a TFET with $T_S = 7$ nm, $T_{\mathrm{OX}} = 2.5$ nm, $\varepsilon_{\mathrm{OX}} = 9\varepsilon_0$, and $L_g = 30$ nm calculated by OMEN, Sentaurus, and this analytical model. It is evident that the analytical model well captures the subthreshold current. Yet, the ON-current in the analytical model increases faster than that calculated via the numerical approach. Fig. 4(c) and (d) compares the electron density and the electron velocity between OMEN and Sentaurus and provides good agreement. It turns out that we neglected the mobile charge term in the Poisson equation, the effect of which is significant at high V_{GS}. Once the inversion of the channel sets in at high V_{GS}, the mobile charge tends to pin the potential in the channel to the drain voltage and prevent further band bending with increasing gate voltage. Since our goal is to develop a generalized scaling theory for TFETs and understand the short-channel effect in TFETs, this issue of ON-current does not influence the subsequent discussions.

III. Model Validation: Materials, Heterojunction, and Doping Variation

There are different semiconductor system options for TFETs, and they may have different carrier tunneling mechanisms. The nonlocal BTBT model using Flietner's two-band dispersion is more suitable for direct band-gap materials such as InGaAs and InAs. For silicon and germanium, the tunnel mechanisms are different, and phonon-assisted tunneling plays an important role. The tunnel generation rate could be treated using similar

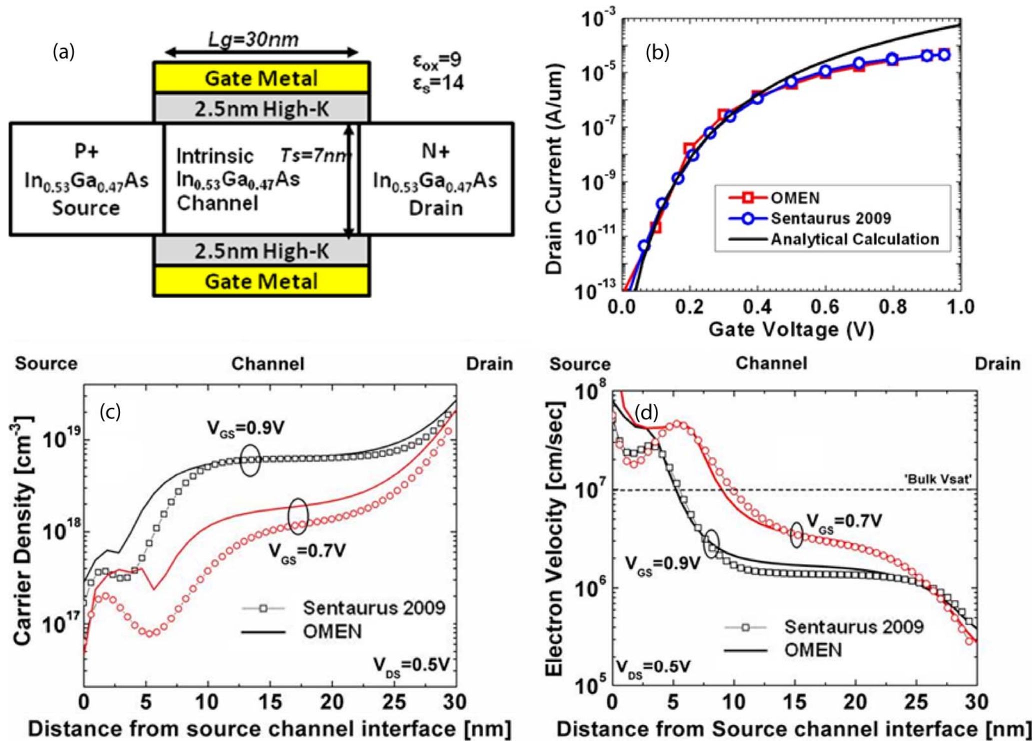

Fig. 4. (a) Schematic of the device structure ($In_{0.53}Ga_{0.47}As$ homojunction TFET). In the TFET, the source is constantly 8×10^{19} cm^{-3} p-type doped, and the drain is constantly 1×10^{19} cm^{-3} n-type doped in Sentaurus and OMEN. There is a 1-nm source/gate overlap in Sentaurus and OMEN. In Sentaurus, the tunneling model based on dynamic meshes is applied. Sentaurus and the analytical model are calibrated by OMEN, in which the Schrödinger equations are solved in a nearest-neighbor tight-binding basis using an efficient wave function approach equivalent to the popular NEGF formalism. (b) I_d–V_g calculations from OMEN, Sentaurus, and this analytical model at $V_{\rm DS} = 0.5$ V. The analytical model has good agreement with OMEN and Sentaurus in the subthreshold regime. The ON-current increases faster than the numerical simulation is due to the absence of mobile charge in the Poisson equation, which tends to partially pin the channel potential to the drain bias at high $V_{\rm GS}$. (c) Carrier density profile from Sentaurus and OMEN. (d) Electron velocity profile from Sentaurus and OMEN.

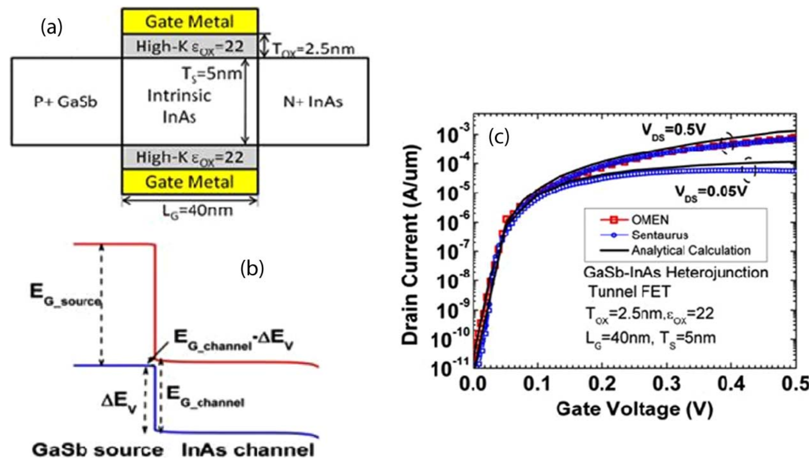

Fig. 5. (a) Schematic of a GaSb–InAs heterojunction TFET. The source is 4×10^{19} cm^{-3} p-type constantly doped, and the drain is 1×10^{18} cm^{-3} n-type constantly doped. (b) The effective tunneling barrier is reduced to $E_{G_\rm channel} - \Delta E_V$ for the staggered heterojunction TFET. (c) The analytical calculation is compared with results from OMEN [14] and Sentaurus, showing good agreement.

methods in [16]. Yet, the silicon TFETs are supposed to exhibit enhanced Miller capacitances, resulting in large voltage overshoot/undershoot in its large-signal switching characteristics [17]. Also, germanium TFETs are supposed to have worse low-power performance, as compared with InGaAs and InAs system [18]. TFETs based on lower band-gap and lower density-of-states materials such as InGaAs and InAs show significant improvement in switching behavior due to its lower capacitance and higher ON-current at reduced voltages.

Due to relative large tunneling barrier height and width, even low band-gap III–V homojunction TFETs still face challenge in demonstrating high drive current like MOSFETs, which is a prime requirement for high-performance logic applications. A staggered heterojunction TFET, such as GaAs(p+)-InAs(i)-InAs(n+), can effectively reduce tunnel barrier height and width, resulting in significant ON-current enhancement [14], [19]. The staggered heterojunction TFET can be conveniently incorporated into this analytical model by

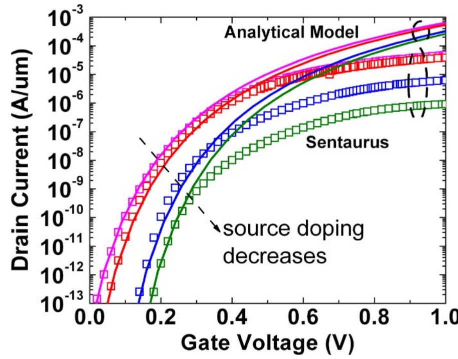

Fig. 6. Transfer characteristic of an $In_{0.53}Ga_{0.47}As$ homojunction TFET with different source doping concentrations 8×10^{19}, 5×10^{19}, 1×10^{19}, and 5×10^{18} cm^{-3}. The device structure and geometry are shown in Fig. 4(a).

modifying the tunnel barrier and the length of tunnel trajectory. For example, in a GaAs(p+)-InAs(i)-InAs(n+) heterojunction TFET [see Fig. 5(a)], the band diagram is shown in Fig. 5(b). The effective barrier height is $E_{g_\text{channel}} - \Delta E_V$, for the tunneling trajectory starting from the source boundary, rather than $(E_{g_\text{channel}}$ in the homojunction system. By replacing E_g/q with $(E_{g_\text{channel}} - \Delta E_V)/q$, we analytically calculated the transfer characteristic, which agrees with the simulation results from OMEN [14] and Sentaurus [15] in Fig. 5(c).

Aside from materials and heterojunctions, it is also valuable to test the model with different doping concentrations. If the source doping concentration is reduced under 1×10^{19} cm^{-3}, the depletion in the source becomes significant, and this assumption of boundary conditions in this analytical model might be less accurate. The transfer characteristic of the device structure in Fig. 4(a) is plotted in Fig. 6 with source doping concentrations 8×10^{19}, 5×10^{19}, 1×10^{19}, and 5×10^{18} cm^{-3}. The turn-on voltage shift is induced by the change of source/channel built-in voltage. The accuracy of the analytical model becomes worse if using a low source doping concentration. Yet, in the TFET design, to enhance the tunneling current, the source is usually heavily p-type doped to achieve higher junction electric field. Thus, this model is still able to capture most of the high-performance TFET design.

IV. Short-Channel Effect and Scalability

Using the analytical model, which includes the effect of drain bias, the short-channel effect of the TFET is studied and compared with that of the MOSFET. While the short-channel effects in MOSFETs are directly related to the phenomenon of drain-induced potential barrier lowering (DIBL), a similar phenomenon called drain-induced barrier thinning (DIBT) exists in the TFET. Fig. 7(a) and (b) shows the I_d–V_g characteristics of the TFET with $L_g = 20$ and 40 nm using the analytical and numerical approaches. When the gate length is scaled to less than four times λ_1/π, the drain bias leads to the significant thinning of the source-side tunnel barrier shifting the transfer characteristics, as shown in Fig. 7. It is to be noted that, in the TFET, the drain bias does not lower the barrier but causes the thinning of the barrier, and the term DIBT for TFETs indicates the threshold-voltage shift phenomenon as a function of drain bias. For short-channel MOSFETs and

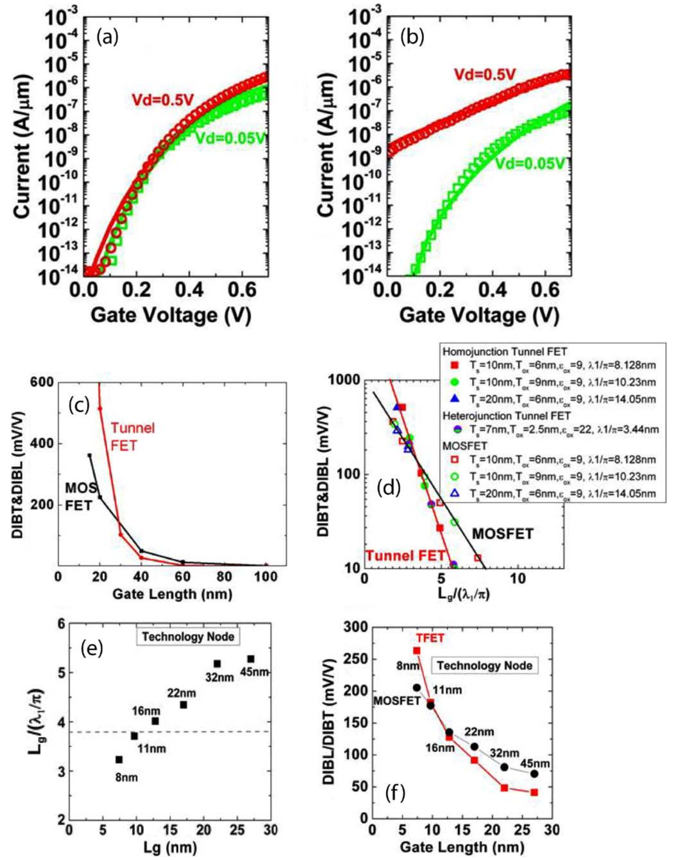

Fig. 7. I_d–V_g curve at $V_{\text{DS}} = 0.5$ and 0.05 V from (dots) numerical simulation and (line) analytical calculation for double-gate $In_{0.53}Ga_{0.47}As$ homojunction TFET with $T_s = 10$ nm, $T_{\text{ox}} = 6$ nm, and $\varepsilon_{\text{ox}} = 9$ for (a) $L_g = 40$ nm and (b) $L_g = 20$ nm. The source is constantly 8×10^{19} cm^{-3} p-type doped, and the drain is constantly 1×10^{19} cm^{-3} n-type doped. (c) DIBL (MOSFET) and DIBT (TFET) plotted as a function of gate length L_g for double-gate $In_{0.53}Ga_{0.47}As$ MOSFET and $In_{0.53}Ga_{0.47}As$ homojunction TFET with $T_s = 10$ nm, $T_{\text{ox}} = 6$ nm, and $\varepsilon_{\text{ox}} = 9$. (d) Scalability comparison of TFETs ($In_{0.53}Ga_{0.47}As$ homojunction and GaSb–InAs heterojunction) and $In_{0.53}Ga_{0.47}As$ MOSFETs. (e) Calculated $L_g/(\lambda_1/\pi)$ for $In_{0.53}Ga_{0.47}As$ MOSFETs and TFETs with L_g, EOT, and T_S dictated by the guideline in the ITRS. (f) DIBL/DIBT for $In_{0.53}Ga_{0.47}As$ MOSFETs and TFETs against L_g and the corresponding technology node.

TFETs, the threshold voltage is simply defined as the gate voltage for a specific drain current of 0.1 $\mu A/\mu m$. The DIBL (MOSFET) and the DIBT (TFET) as a function of gate voltage are compared in Fig. 7(c) for the double-gate MOSFET and TFET with $T_s = 10$ nm, $T_{\text{ox}} = 6$ nm, and $\varepsilon_{\text{ox}} = 9$. The scalability of MOSFETs is well covered in [20], [9], and [21], and the DIBL values obtained from our MOSFET simulations with various body thicknesses, gate oxide dielectric constants, and gate oxide thicknesses obey the universal scaling curve of DIBL versus L_g/Λ, where the natural length Λ is defined using the potential profile near the source/channel region as $\psi(x, y) \approx [\psi_s(y) - \psi_c(y)] \exp(-x/\Lambda)$. Λ can be estimated as λ_1/π from the first-order eigenfunction approximation. With more significant influence on the DIBT from the higher order terms in TFETs caused by the drain influence on the electric-field profile near the tunnel junction, the DIBT relationship with λ_1/π is not as universal as the DIBL in MOSFETs but roughly fall on one curve [see Fig. 7(d)] when the device dimensions such as gate stack thickness and body thickness are

varied. For gate lengths longer than four times λ_1/π, the DIBT is smaller in TFETs than the DIBL in MOSFETs indicating superior short-channel effects but degrades faster in TFETs than MOSFETs when the gate lengths are scaled below four times λ_1/π [see Fig. 7(d)]. The DIBL and the DIBT are both short-channel effects with similar behavior. However, the DIBL in MOSFETs arises from source-to-channel barrier potential being lowered by the drain potential, whereas the DIBT in TFETs is due to the source-to-channel junction electric field influenced by the drain bias. The change in the electric field, which is the derivative of the electric potential, has more influence on the TFET characteristic. Therefore, the DIBT in TFETs is more sensitive to gate length scaling compared with the DIBL in MOSFETs resulting in a steeper slope. In Fig. 7(e), $L_g/(\lambda_1/\pi)$ is calculated for MOSFETs and TFETs and plotted against L_g and the corresponding technology node. The DIBL/DIBT for these MOSFETs and TFETs is plotted in Fig. 7(f). The equivalent oxide thickness (EOT) and T_S values at each technology node are dictated by the guideline specified in the International Technology Roadmap for Semiconductors (ITRS) [22]. Based on the ITRS scaling trends, we observe that the electrostatic length λ_1/π is scaling at a much slower pace than the physical L_g, and thus, TFETs are viable only up to the 11-nm technology node, where the gate length stays above the critical electrostatics scaling length of four times λ_1/π. Therefore, a more aggressive λ_1/π (EOT or T_S) scaling than that specified in the ITRS node is needed for TFETs to outperform their MOSFETs in terms of short-channel effects, if they are to be deployed for the 8-nm technology node and beyond. Device geometries and material properties are included in the tunnel probability coefficient and λ_1/π calculation. Since the TFET DIBT is plotted as a function of $L_g/(\lambda_1/\pi)$, we get a scaling curve when we vary $T_{\rm ox}$, T_s, and the dielectric constant. Thus, we can conclude that the crossover point represents a fundamentally critical threshold where the TFETs can and will outperform or underperform MOSFETs. We have verified that this critical threshold holds true for both homojunction and heterojunction TFETs. It is noted that, although the heterojunction TFET has much larger tunnel probability compared with the homojunction TFET at the same bias condition, the DIBT scaling curve as a function of $L_g/(\lambda_1/\pi)$ is similar. This suggests that the DIBT mostly depends on the electrostatics, which is consistent with [19]. It is shown in Fig. 8(a)–(c) that the physical gate oxide thickness $T_{\rm ox}$ has the strongest influence on TFETs scaling over a large range of gate lengths, whereas the body thickness T_S has a comparable influence as $T_{\rm OX}$ for ultrashort gate lengths. Fig. 8(d) shows an empirical scaling length $\lambda_{\rm emp} = 0.86\lambda_1/\pi + 0.31\lambda_3/\pi + 0.27\lambda_5/\pi$ for TFETs. The DIBT values of TFETs versus the gate length normalized by $\lambda_{\rm emp}$ are aligned on one universal scaling curve.

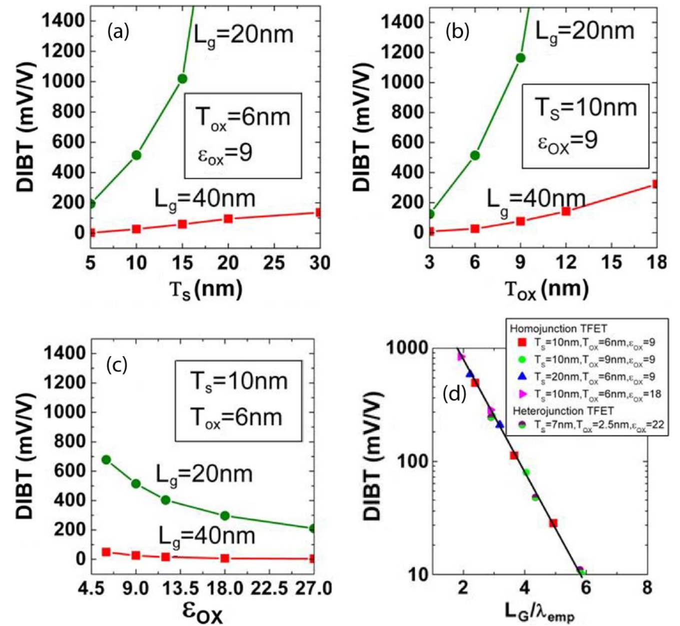

Fig. 8. DIBT versus (a) T_s, (b) $T_{\rm ox}$, and (c) $\varepsilon_{\rm ox}$ in TFET. $T_{\rm ox}$ has the strongest influence on TFET scaling over all gate lengths. For ultrashort gate lengths, T_s has comparable influence on scaling as $T_{\rm ox}$. (d) Empirical scaling length of TFETs. $\lambda_{\rm emp} = 0.86\lambda_1/\pi + 0.31\lambda_3/\pi + 0.27\lambda_5/\pi$.

V. Conclusion

We have developed here a generalized scaling theory for double-gate interband TFETs using a 2-D physics-based analytical model including the influence of the drain bias. Based on this model, we have derived an empirical scaling length for TFETs and have compared the short-channel performance between MOSFETs and TFETs. We have shown that the double-gate TFETs exhibit markedly reduced shift in their transfer characteristic due to drain bias than their double-gate MOSFETs counterparts at longer physical gate lengths (gate length longer than four times their natural scaling length), but the scalability of the TFETs degrades at a faster rate than MOSFETs with aggressive gate length scaling (gate length shorter than four times their natural scaling length).

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Lu Liu (S'09) received the B.S. degree in physics from Peking University, Beijing, China, in 2008. He is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical Engineering, Pennsylvania State University, University Park.

His research interests include design, fabrication, and characterization of novel ultralow-power nanoscale devices.

Dheeraj Mohata (S'09) received the B.S. degree in electrical engineering from College of Engineering and Technology, Bhubaneswar, India, and M.S. degree in electrical engineering from the Indian Institute of Technology Kanpur, Kanpur, India. He is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical Engineering, Pennsylvania State University, University Park.

His research interests include design, fabrication, and characterization of interband tunnel FET for next generation of information processing applications.

Suman Datta (SM'06) received the B.S. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1995 and the Ph.D. degree in electrical and computer engineering from the University of Cincinnati, Cincinnati, OH, in 1999.

From 1999 to 2007, as a Member of the Logic Technology Development Group, Intel Corporation, he was instrumental in the demonstration of indium–antimonide-based quantum-well transistors operating at room temperature with a record energy-delay product, the first experimental demonstration of metal gate plasmon screening and channel strain engineering in high-κ/metal gate CMOS transistors, and the investigation of the transport properties in nonplanar "trigate transistors." In 2007, he was the Joseph Monkowski Associate Professor of electrical engineering with Pennsylvania State University, University Park, where he is currently a Professor of electrical engineering. He is the holder of more than 130 U.S. patents. His group is exploring new materials and novel device architecture for CMOS "enhancement" and "replacement" for future energy-efficient computing applications.

Dr. Datta is a Distinguished Lecturer of the IEEE Electron Devices Society.