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A programmable ferroelectric single electron transistor

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We experimentally demonstrate a programmable ferroelectric single electron transistor using direct monolithic integration of a multi-gate III-V ($In_{0.7}Ga_{0.3}As$) quantum well field effect transistor with a composite ferroelectric (lead zirconium titanate) and high-k (hafnium dioxide) gate stack. A split gate electrode configuration allows electrical tuning of the tunnel barrier profile and reconfigurable programming of the device to operate in both classical and Coulomb blockade mode. The ferroelectric gate stack under the split gate electrode further allows non-volatile operation in both modes. This demonstration is a significant step towards realization of a non-volatile, programmable binary decision diagram logic circuit for ultra low power operation. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4791601]

Nanoscale devices that transport and store few or single electron, already implemented in low supply voltage memory, have also attracted recent research interests for sub 300 mV logic applications.[1–5] Yet majority of these few electron devices suffer from low transconductance, degraded output resistance, and, often, from a lack of complementary logic (n and p-channel device) solution,[3,5] making it essential to co-explore the device design in conjunction with a non-complementary metal-oxide-semiconductor but preferably Boolean logic architecture. The binary decision diagram (BDD) logic architecture has been proposed as a suitable candidate for implementing logic with these single electron transistors (SETs).[2] Due to potentially high defect rate and variability in the devices operating close to the limit of scaling, reconfigurability is vital to SET architecture.[3,5] Reconfigurable BDD architecture requires the SET to be programmed not only to perform as a decision node edge using its Coulomb blockade functionality and execute the path switching function but also to implement a short or an open path along certain edges of the two-dimensional hexagonal fabric.[1,3,5] There are several reported SET configurations as shown in Figure 1. In the simplest construct, the tunnel barriers can be a few nanometer thick insulator films physically situated between the source/drain and the nanodot acts as the Coulomb island.[6–8] The disadvantage of physical insulator barrier is that the tunnel resistance is determined by the film thickness and the conduction band barrier height, which cannot be modulated once the device is fabricated. To achieve a programmable operation, one can harness the depletion created by two negatively biased split gates region as an electrically tunable tunnel barrier.[1–5,9–12] The coupling strength between the source/drain reservoirs and the Coulomb island can be continuously modulated by the split gate voltage. With an independent control gate to modulate the Coulomb island potential, these devices have been shown to have the required programmability feature and allow implementation of reconfigurable BDD logic.[1,5,11] However, in this case, the tunnel barriers become volatile and programming mode is not retained once the split gate bias is removed. In this letter, we report the experimental demonstration of a programmable non-volatile SET using direct monolithic integration of a multi-gate III-V ($In_{0.7}Ga_{0.3}As$) quantum well field effect transistor with a composite ferroelectric (lead zirconium titanate) and high-k (hafnium dioxide) gate stack. A non-volatile device that retains the states can achieve zero-static power consumption in idle mode without loss of state. Such a scenario is vital in low-activity and ultra low standby power logic circuits employed in applications such as power-constrained distributed sensor nodes or implantable electronics.[13,14]

The non-volatile, reconfigurable SET was fabricated on a strained $In_{0.7}Ga_{0.3}As$ quantum well heterostructure. The layer structure consists of InP substrate/$In_{0.52}Al_{0.48}As$ (300 nm) buffer layer/2×10^{12} cm^{-2} of Si (n-type) modulation doping/$In_{0.52}Al_{0.48}As$ (3 nm) spacer layer/$In_{0.7}Ga_{0.3}As$ (12 nm) quantum well/$In_{0.52}Al_{0.48}As$ (2 nm) upper barrier layer/InP (2 nm) cap layer. The device fabrication flow is described in Figure 2(a). An array of fins 40 nm wide is first defined with electron beam lithography and etched by low power BCl_3/Ar dry etch. 10 nm thick hafnium dioxide (HfO_2) high-k dielectric was deposited using atomic layer deposition at 250 °C. 130 nm thick $Pb[Zr_{0.52}Ti_{0.48}]O_3$ (PZT) ferroelectric dielectric was deposited in the Kurt Lesker CMS-18 RF sputtering system. The single PZT sputtering target is comprised of PbO, TiO_2, and ZrO_2 in the stoichiometric composition. The sputtering process is kept at low deposition rate (around 1.2 nm/min). The amorphous PZT was crystallized at 550 °C for 2 min in oxygen ambient in All-Win 610 rapid thermal annealing system. After etching the dielectric in the contact region, a tri-layer metal stack comprising of Ni (10 nm)/Ge (30 nm)/Au (80 nm) was deposited to form the source/drain contact using an evaporation and lift-off process. The split gate (SG) electrode pattern with separation distance ranging from 60 nm to 500 nm was defined by e-beam lithography. The split gate stack comprising of Ti (40 nm)/Au (40 nm)/Cr (150 nm) tri-layer metal stack was formed using evaporation and lift-off process. A well-controlled CHF_3/CF_4 PZT dry etch was conducted

Device configuration	Schematic	Features
gated nanodot with thin insulators [6-8]	control gate / thin insulator	non-volatile not programmable
nanowire with split gate [1-5,9-12]	control gate / split gate	volatile programmable
nanowire ferroelectric split gate (this work)	control gate / ferroelectric split gate	non-volatile programmable

FIG. 1. Comparison of various device configurations of SET.

using split gate metal as a mask and stopped at HfO_2 layer. Typically, the chromium mask was consumed and less than 5 nm HfO_2 was over-etched. Another 20 nm HfO_2 thick was deposited and a top control gate (CG) consisting of Ti (40 nm)/Au (40 nm) thick metal stack was patterned using. Finally, the source/drain contacts were opened through the oxide using Cl_2 dry etch. Figure 2(b) shows the tilted scanning electron microscope image of a fabricated SET. There is only one active central fin width connecting source and drain. The neighboring dummy fins are used to reduce electron deflection into the central fin during patterning. The control gate width was extended around 100 nm to compensate for the possible alignment error. The transmission electron microscope image of the plane along the transport direction is shown in Figure 2(c). The magnified view of the outlined region of Figure 2(c) is shown in Figure 2(d).

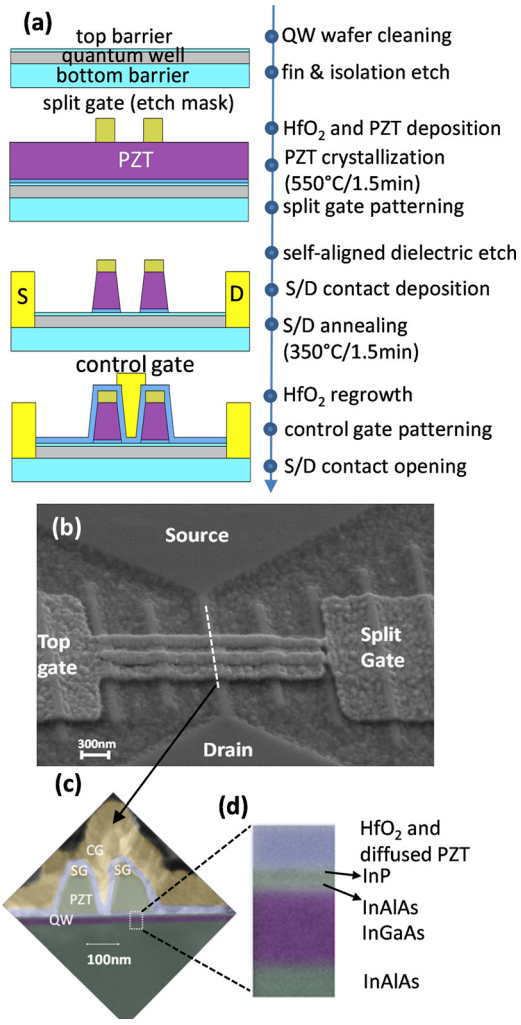
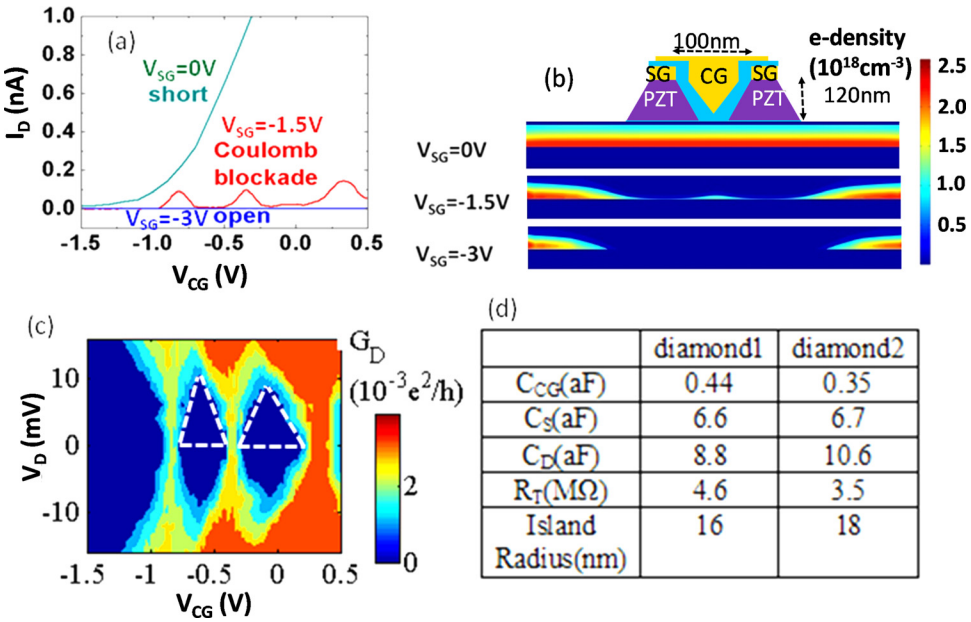


FIG. 2. (a) Fabrication flow of ferroelectric single electron transistor; (b) Tilted scanning electron microscope image of a single electron transistor; (b) Cross-section schematic along transport direction; (c) False colored transmission electron microscope image of cross-section indicated in (b); (d) A magnified view of the outlined region in (c).

From the split gate separation, fin width and quantum well thickness, the dimension of Coulomb island was estimated to be $60\,\text{nm} \times 40\,\text{nm} \times 12\,\text{nm}$, which results in approximately 20 meV of Coulomb charging energy. Thus, the measurement was conducted in a cryogenic probe station at 4.2 K using liquid helium, sufficiently low to observe the Coulomb blockade in our devices. For the measured eight devices of the same dimension on the same substrate, six of them show I_D-V_{CG} oscillations at $V_D = 1\,\text{mV}$ and $V_{SG} = -1.5\,\text{V}$. The standard deviations of I_D and V_{CG} for the first oscillation peak are 0.021 nA and 0.18 V. In Figure 3(a), the I_D-V_{CG} of one functional device for three different V_{SG} values was plotted for $V_D = 1\,\text{mV}$. Both the split gate and control gate leakage were negligible (around 10^{-12} A). We experimentally confirmed the open, Coulomb blockade and short device operation modes programmed by the split gate voltage. With the device geometry, as confirmed by the transmission electron microscope image Figure 2(c), the corresponding electron density was calculated using a self-consistent Schrödinger Poisson approach in Next**Nano**® simulator as shown in Figure 3(b). We could identify the three modes of operation: (1) At $V_{SG} = 0\,\text{V}$, the tunnel barriers collapsed and the device behaved like a classical metal-oxide-semiconductor field effect transistor gated by the control gate electrode CG (short mode); (2) For $V_{SG} = -1.5\,\text{V}$, the moderate depletion from the split gate resulted in a few mega Ohm of tunneling resistance, and CG modulated the Coulomb island leading to SET operation (Coulomb blockade mode); (3) At $V_{SG} = -3\,\text{V}$, the split gates heavily depleted the narrow fin resulting in only background leakage current (open mode). Figure 3(c) shows the drain conductance contour as a function of V_D and V_{CG} at $V_{SG} = -1.5\,\text{V}$. The diamond shape contour provides further confirmation that the oscillations at $V_{SG} = -1.5\,\text{V}$ indeed come from the Coulomb Blockade. A Coulomb blockade energy around 12 meV is observed. The Coulomb diamond width ΔV_{CG} is used to calculate the control gate capacitance $C_{CG} = e/V_{CG}$, and the slope of the diamond left and right edge given by $C_{CG}/(C_{CG} + C_S)$ and $C_{CG}/(C_D)$ determine C_S and C_D. From the current outside the Coulomb diamond, the coupling resistance can be estimated as $0.5 \times dV_D/dI_D$. The gate coupling factors C_G/C_Σ are estimated to be 2.8% and 1.7% for the first and second Coulomb diamond, where $C_\Sigma = C_{CG} + C_S + C_D$ is the total capacitance. The total capacitance provides a rough estimate of the island diameter of 32 nm and 36 nm from the first and second diamonds, respectively, if we approximate the Coulomb island as an isolated disc of radius $r = C_\Sigma/8\varepsilon$. The simulated electron density profile in Figure 3(b) shows the Coulomb island diameter to be around 40 nm in extent along the transport direction, which



	diamond1	diamond2
C_{CG}(aF)	0.44	0.35
C_S(aF)	6.6	6.7
C_D(aF)	8.8	10.6
R_T(MΩ)	4.6	3.5
Island Radius(nm)	16	18

FIG. 3. Programmability of the fabricated SET. (a) I_D-V_G for open, Coulomb blockade and shot mode at $V_D = 1$ mV; (b) self-consistent Poisson-Schrodinger simulation shows the electron density within the device geometry in Figure 2(c) ($V_{CG} = 0$ V); (c) Drain conductance contour as a function of V_{CG} and V_D at $V_{SG} = -1.5$ V and $T = 4$ K (Coulomb oscillation diamond). (d) Device parameters extracted from Coulomb diamond size (e/C_{CG}) and edge slopes (left: $C_S/(C_S + C_{CG})$; right: C_D/C_{CG}).

is in agreement with estimation from the measured Coulomb diamond. The extracted device parameters are listed in Figure 3(d). The Coulomb island size, which is mainly controlled by the split gate bias and separation, does not change much with control gate modulation.

Due to the ferroelectric split gate stack, the fabricated SET can be operated in a non-volatile fashion after removal of the split gate bias. Below the Curie temperature, the displacement of Ti or Zr from the central position in the PZT unit cell creates an electric dipole. The dipoles are initially randomly oriented in PZT film after crystallization and cooling. A programming voltage forces these individual dipoles to reorient along the electric field direction (electrical poling). When the programming electric field is removed, the dipoles remain fairly aligned resulting in remnant polarization. The remnant polarization in the PZT ferroelectric dielectric layer will maintain the depletion region in the access region thus retaining the tunnel resistance values. Figures 4(a)–4(c) illustrate the program, retention, and reset modes of operation of the non-volatile SET. During the programming stage ($t < 0$), the selected programming pulses of amplitude 0 V, −7.5 V, and −12 V were applied to the split gate. For non-volatile operation, in order to sufficiently polarize the PZT, a much larger programming voltage needs to be applied on the split gate as compared to the volatile operation in Figure 3. During the retention stage, the activated remnant polarization maintained the device mode after the programming voltage was removed. In the recovery stage, a split gate voltage of amplitude 2 V was used to erase the remnant polarization and to reset the device to its initial state. In Figures 4(a)–4(c), the extracted tunnel resistance is plotted as a function of time for three modes at $V_D = 1$ mV and $V_{CG} = 0$ V. Less than 20% change in the

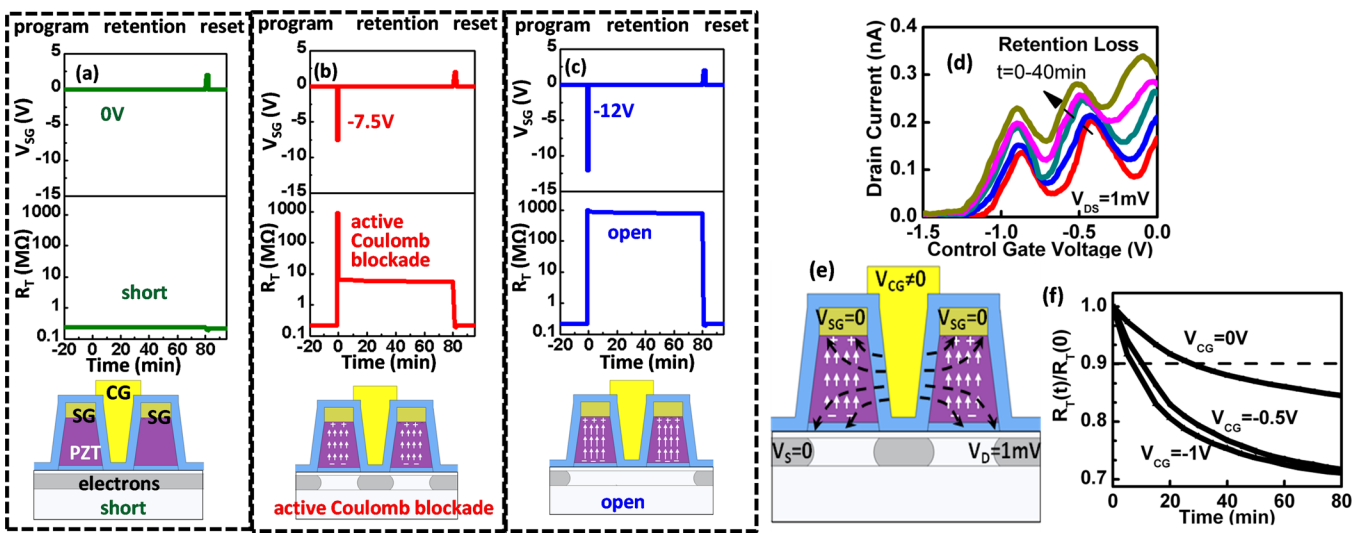


FIG. 4. Non-volatility of the ferroelectric single electron transistor. (a-c) The split gate bias V_{SG} and measured coupling resistance R_T is plotted as a function of time for short, Coulomb blockade and open mode. The schematics below show the remnant polarizations in the ferroelectric layer and electron density distribution in the quantum well. The measurement was done with $V_{DS} = 1$ mV, $V_{CG} = 0$ V, and $T = 4$ K. (d) Coulomb oscillations I_D-V_{CG} are measured for different times in retention stage. (e) The fringing electric field from V_{CG} bias tends to disturb the remnant polarizations, leading to degradation of the retention time. (f) Tunnel resistance is plotted as a function of time for different V_{CG}. The tunnel resistance reduction is less than 10% for more than 5 min over V_{CG} range from −1 V to 0 V range for the first and second Coulomb diamond.

tunnel resistance was observed during the entire 80 min retention measurement period for the Coulomb blockade and short operating modes, and no discernible change in tunnel resistance was observed for the open mode. In this work, we use tunnel resistance extracted from time dependent drain current measurements as the metric to characterize the device retention time. However, the tunnel resistance cannot be directly calculated simply as $V_D/2I_D$ for Coulomb blockade devices. Thus, for the tunnel resistance extraction, we used a transistor with the same structure and dimension, but with a larger split gate separation (500 nm), fabricated alongside the SET. It has the same tunnel resistance with the SET, but does not operate in Coulomb blockade regime due to the large separation distance between the split gate electrode pair. In the Coulomb blockade mode, the ferroelectric depolarization effects result in loss of remnant polarization over time leading to weaker depletion,[15] which enlarges the Coulomb island and reduces the coupling strength to the source/drain reservoirs. This is observed in the form of both reduced Coulomb oscillation period and reduced tunnel resistance as shown in Figure 4(d). The drain current is only affected by the tunneling resistance which is a function of V_{CG}, V_D and remnant polarization, and is independent of the Coulomb period change. In Figure 4(d), the I_D-V_{CG} characteristic of the SET Coulomb blockade mode plotted at different times in the retention stage shows that the SET maintained non-volatile Coulomb blockade characteristic for more than 40 min. It is noted that the current level change over time in Figure 4(d) is faster than the tunnel resistance change in Figure 4(b) with no control gate bias. This is due to effect of the fringe electric field emanating from the control gate and terminating on the ferroelectric sidewall. Hence, in addition to the self-depolarization in the split gate stack, any fringing electric field from the control gate bias (either V_{CG} sweep in the device measurement or logic input in circuits topology) tends to disturb the remnant polarization and degrade the retention characteristics as shown in Figure 4(e). Figure 4(f) shows the tunnel resistance as a function of time at different control gate biases. It is observed that over a control gate voltage range of the first and second coulomb diamond (−1 V to 0 V), the tunnel resistance reduction is less than 10% for a period larger than 5 min. The key improvement to avoiding the control gate disturbance in future devices will be the pursuit of reduction of the ferroelectric layer thickness so as to reduce the control gate modulation on the PZT sidewall. Further, recent material innovations in ultra-thin (less than 10 nm) ferroelectric dielectrics such as $Zr_{0.5}Hf_{0.5}O_2$ will mitigate the disturbance effect from the control gate and increase the retention time.[16] The PZT ferroelectric gate stack needs relatively high supply voltage to perform the programming operation. This could be circumvented by using the complementary ferroelectric capacitor structure where the voltage swing generated by the capacitive coupling effect of the capacitor pair is large enough to perform the programming action at low supply voltages.[17]

In conclusion, we have demonstrated the experimental feasibility of a programmable non-volatile SET. The SET utilizing ferroelectric split gate is experimentally realized based on a multi-gate InGaAs nanowire configuration. The SET exhibits both programmable characteristics and reasonable retention time, which provides a suitable platform for realizing ultra low power reconfigurable BDD logic. Binary decision diagram implemented with programmable non-volatile SETs presents an interesting opportunity for designing future ultra-low power logic circuits The transistor level reconfigurability using split gate concept that we have demonstrated in this work is essential to realize reconfigurable BDD architecture to address device to device variation, while the non-volatility feature stemming from incorporating a ferroelectric dielectric in the split gate stack is paramount for addressing static power consumption.

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