A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter

Moon Seok Kim, *Student Member, IEEE*, Huichu Liu, *Student Member, IEEE*, Xueqing Li, *Member, IEEE*, Suman Datta, *Fellow, IEEE*, and Vijaykrishnan Narayanan, *Fellow, IEEE*

Abstract— This paper explores the energy efficiency advantage of a 6-bit III-V heterojunction tunnel field-effect transistor (HTFET) based successive-approximation register (SAR) analog-to-digital converter (ADC) with 20-nm gate length. Compared with the Silicon FinFET (Si FinFET) ADC, the HTFET SAR ADC achieves approximately 3 times power consumption reduction and 6 times size reduction. Signal-to-noise and distortion ratio is 31.4 dB for the HTFET SAR ADC, which is 2.81 dB higher than the Si FinFET ADC due to the decreased quantization noise rising from the high ON-current characteristic of HTFET at low supply voltage. The energy per conversion step for both HTFET and Si FinFET ADC designs are 0.43 and 1.65 fJ/conversion-step, respectively, at a fixed supply voltage of 0.30 V.

Index Terms— Analog-to-digital converter (ADC), heterojunction tunnel FET (HTFET), successive-approximation register (SAR), ultra-low-power.

Fig. 1. ADC data survey showing current technology limit and a noise limit in current CMOS ADC designs [4], [7].

I. INTRODUCTION

ULTRA-LOW-POWER circuit design techniques have brought in growing interest in power-constrained applications, such as energy harvesting systems, sensor networks, and biomedical implants [1]–[3], where the energy efficiency and area cost to convert analog signal to digital data have profound impact on the overall system performance. Tremendous progress has been made to leverage the power consumption, chip area, and data conversion speed in analog-to-digital-converter (ADC) designs to enable the low-power mixed-signal/RF applications [2]–[5]. For digital circuits in ADCs, technology scaling companied with the supply voltage (V_{DD}) reduction provides continuous improvement of energy efficiency [4]. However, the diminished signal-to-noise ratio (SNR) at a lower V_{DD} can be detrimental for analog
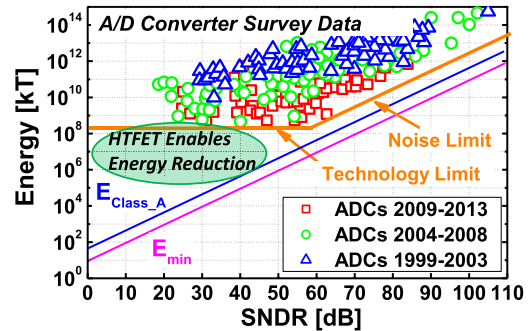
circuits [4], [5]. Recently, the near/subthreshold CMOS technologies have been applied to ADC designs with digital assisted blocks to explore the optimal energy efficiency albeit with sacrificing certain degree of speed, matching, noise performance, and area [4], [6]. However, the minimum energy achieved in current ADC designs, as shown in Fig. 1 [4], is still limited by the energy efficiency of CMOS technology, especially in the low-resolution [low signal-to-noise and distortion ratio (SNDR)] regime, where the innovations of device technology are required to enable further energy reduction beyond CMOS limit [4], [7].

Tunnel field-effect transistor (TFET) [8] has emerged as a strong candidate for various low voltage digital applications [9]–[11] due to its superior energy efficiency arising from the subthermal switching characteristics at a low V_{DD}. The work on TFET analog/RF circuit designs in [12] and [13] further explored its unique device characteristics, such as asymmetrical source/drain design, steep switching, and low voltage operation, to construct the ultra-low power energy harvesting systems. The recent work in [14] demonstrated the high-frequency switching of the fabricated $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken-gap heterojunction tunnel FET (III–V HTFET) with intrinsic cutoff frequency (f_T) of 22 and 39 GHz achieved at 0.30 and 0.50 V, respectively, which highlighted the desired RF characteristics and significant power reduction projection with channel-length scaling. Therefore, TFET technology can be potentially applied to overcome the growing challenge in energy efficiency using the conventional CMOS technology for ultra-low power mixed-signal applications.

The goal of this paper is to explore the advantages of 20-nm HTFET device characteristics in mixed-signal domain and to

design energy efficient HTFET ADC operating below 0.50 V. For the first time, we explore the design, analysis and performance benchmarking of the III–V HTFET 6-bit successive-approximation register (SAR) ADC (HTFET SAR ADC) against the Si FinFET SAR ADC for ultra-low power/energy-efficient systems. Among various ADC designs, we choose the SAR ADC topology due to its desired energy efficiency in low to moderate resolution regime and medium bandwidth application ranges [4], [15], where low-power devices are desired for energy saving purpose (Fig. 1). We also investigate the device noise impact on the HTFET SAR ADC performance compared with the Si FinFET SAR ADC. This paper is organized as follows. Section II presents the advantage of the HTFET for ultra-low power SAR ADC and the device modeling methodology for the HTFET circuit implementations. The design of individual modules of both HTFET and Si FinFET SAR ADCs are described in Section III. Section IV presents the energy and performance evaluation for both HTFET and Si FinFET SAR ADCs. The conclusion is provided in Section V to summarize our results.

II. TFET Advantages and Modeling Methodology for Low-Power ADC Application

A. Low-Power CMOS ADC Design Challenges

In digital circuits, the dynamic power consumption $P_{Digital}$ is quadratic related to V_{DD}, as shown in (1), hence, V_{DD} scaling can enable the power reduction with the effective control of the OFF-state leakage power [5]. Unlike the digital circuits, the analog circuit performance is primarily limited by the thermal noise kT/C (k is the Boltzmann constant, T is the absolute temperature, and C is the overall capacitance), which is inversely proportional to the current I_{DS} at a given bias point ($kT/C \propto 1/I_{DS}$) [4], [5]. The power dissipation in the SNR limited analog circuits can be expressed as (2) assuming the signal power is $(\beta \cdot V_{DD})^2$ [4], [5]

$$P_{Digital} \propto C \times V_{DD}^2 \times \alpha \times f_s \qquad (1)$$

$$P_{Analog} \propto \frac{1}{\beta} \times \frac{1}{V_{DD}} \times \frac{1}{\frac{g_m}{I_{DS}}} \times kT \times SNR \times f_s. \qquad (2)$$

Assuming

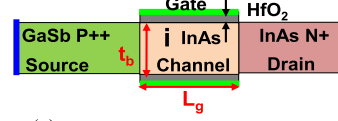$$f_s \propto \frac{g_m}{C}, \quad SNR \propto \frac{(\beta V_{DD})^2}{kT/C}$$

where α is the activity factor, which indicates the ratio of the internal clock frequency f_c over sampling frequency f_s, β is the ratio of signal peak voltage V_{pp} to V_{DD}, g_m is the transistor transconductance, and the transistor bias point is indicated by g_m/I_{DS}. Therefore, in a fixed design with constant g_m/I_{DS} and f_s diminishing V_{DD}, while maintaining SNR will worsen the power consumption in analog components.

Today's analog system designs normally employ digital components to assist the performance and functionality [4], [5], e.g., SAR ADCs. The total power consumption can be expressed as $P_{ADC} = P_{Analog} + P_{Digital}$, which leads to the total energy consumption E_{ADC} as (at $\beta = 1$)

$$E_{ADC} = \frac{P}{f_s} \propto \left(\frac{1}{V_{DD}} \times \frac{1}{\frac{g_m}{I_{DS}}} \times kT \times SNR \right) + \left(C \times V_{DD}^2 \times \alpha \right). \qquad (3)$$

(a) Double-Gate III-V n-HTFET Schematic

(b) I_{DS}-V_{GS} Characteristics

(c) n-HTFET Device Parameters

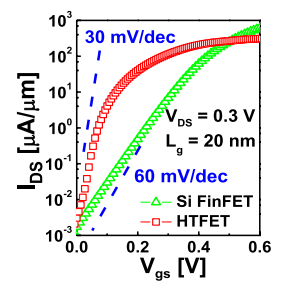| Gate Length (L_g) | 20 nm |
EOT (HfO$_2$)	0.7 nm
Body Thickness (t_b)	5 nm
Si FinFET S/D Doping	1×10^{20} cm^{-3}
n-HTFET S (GaSb) Doping	4×10^{19} cm^{-3}
n-HTFET D (InAs) Doping	2×10^{17} cm^{-3}
HTFET: $E_{g,GaSb}$=0.845 eV, $E_{g,InAs}$=0.49 eV, ΔE_c=0.439eV, Gate Workfunction: 4.85 eV	

Fig. 2. (a) 2-D TCAD simulation schematic of the double-gate GaSb-InAs HTFET [10]. (b) I_{DS}–V_{GS} characteristics comparing Si FinFET and HTFET at $L_g = 20$ nm obtained from calibrated TCAD models in [10] and [16], respectively. (c) n-HTFET device parameters for TCAD simulation. For HTFET, 1-nm gate-source overlap and 1-nm gate-drain underlap are used in the model.

In CMOS technology, g_m/I_{DS} has the maximum value of 40 V^{-1} achieved in the subthreshold region as

$$g_{m,MOSFET} = \frac{I_{D0}}{nV_t} \left(1 - \exp\left(-\frac{V_{DS}}{V_t} \right) \right) \cdot \exp\left(\frac{V_{GS} - V_{th}}{nV_t} \right) \qquad (4)$$

$$\frac{g_{m,MOSFET}}{I_{DS}} \propto \frac{1}{nV_t} < \frac{1}{26 \text{ mV}} \approx 40 \text{ V}^{-1} \qquad (5)$$

where V_{th} is the threshold voltage and V_t is the thermal voltage. However, subthreshold operation of CMOS can significantly reduce the transistor f_T, which limits the sampling frequency f_s due to the requirement of $f_s < f_T/80$ [4]. Fig. 1 shows the energy consumption of various ADC designs versus SNDR (with the consideration of signal-distortion effect in ADCs) with the fundamental noise limit given by the minimum energy of the idealized amplifier E_{min} and practical amplifier E_{class_A} [4], which reveals the energy efficiency challenge in CMOS ADC design. The high-resolution design (SNDR > 60 dB) is limited by the noise-limited power efficiency and nonlinearity matching, while the low-resolution design (SNDR < 60 dB) is limited by state-of-the-art CMOS technology. The limited g_m/I_{DS} and practical tradeoff of g_m/I_{DS} versus f_T pose the fundamental challenge for V_{DD} reduction in ultra-low power CMOS ADCs.

B. TFET Advantages for Low-Power ADC Design

TFET overcomes the 60 mV/dec subthreshold slope (SS) limit of MOSFET [8] due to the tunneling induced carrier injection mechanism. With improved tunneling probability and high ON-current at a low V_{DD} achieved by the III–V HTFET [11], [17], V_{DD} scaling can be further enabled to mitigate the challenge between the leakage power constrain and V_{th} scaling in the TFET digital circuits. Here, we setup the GaSb-InAs HTFET model using technology computer-aided design (TCAD) Sentaurus [16], which has been calibrated [10] with full-band atomistic simulation in [18]. The Si FinFET is used as baseline for performance comparison, which has also been calibrated with experimental data in [19]. As shown in Fig. 2, an effective SS of 30 mV/dec (over two
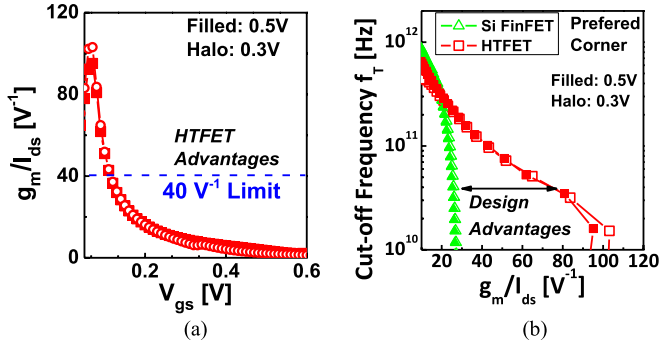
Fig. 3. (a) g_m/I_{DS} versus V_{GS} of HTFET showing HTFET overcoming 40 V^{-1} CMOS limit due to steep switching at a low V_{GS}. (b) f_T versus g_m/I_{DS} comparison of HTFET and Si FinFET, showing improved design space of HTFET considering the tradeoff between high frequency and g_m/I_{DS}.

Fig. 4. III–V p-HTFET simulation structure and device parameters for circuit simulations.

TABLE I
DEVICE CHARACTERISTICS COMPARISON

	n-HTFET	p-HTFET	Si FinFET
Threshold Voltage $|V_{th}|$	0.12 V	0.13 V	0.25 V
Subthreshold slope (SS)	30 mV/dec	55 mV/dec	65 mV/dec
$|g_{ds}|$ ($|V_{GS}|=|V_{DS}|=0.30V$)	177 µS/µm	23.2 µS/µm	8.97 µS/µm
$|g_m|$ ($|V_{GS}|=|V_{DS}|=0.30V$)	1.57 mS/µm	1.04 mS/µm	0.18 mS/µm
$|g_m|/I_{DS}$ ($|I_{DS}|=10\mu A/\mu m$, $|V_{DS}|=0.30V$)	43 V^{-1}	35 V^{-1}	27 V^{-1}
On-current I_{on} ($V_{DD}=0.30V$)	114 µA/µm	52.7 µA/µm	6.20 µA/µm
Off-current I_{off} ($V_{DD}=0.30V$)	2.4 nA/µm	1.35 nA/µm	3.3 nA/µm
f_T ($V_{DD} = 0.30$ V)	377 GHz	331 GHz	140 GHz
Noise Power S_{Id}/i_D^2 ($|V_{GS}|=|V_{DS}|=0.30$ V) @10 GHz	9.07e-15 Hz^{-1}	2.02e-14 Hz^{-1}	1.15e-13 Hz^{-1}

Fig. 5. Lookup table based Verilog-A model schematic for double-gate HTFET and Si FinFET. Both dc and transient characteristics can be captured.

decades change of I_{DS} from 10^{-2} to 1 $\mu A/\mu m$) and 7 times improvement of I_{DS} at 0.30 V can be achieved in the modeled HTFET over Si FinFET at gate-length $L_g = 20$ nm, which is consistent with the reported simulation results in [11]. The device parameters for our modeling are listed in Fig. 2(c) for the HTFET and the baseline Si FinFET n-type devices.

Fig. 3(a) shows the g_m/I_{DS} versus V_{GS} for HTFET and Si FinFET at $V_{DS} = 0.30$ and 0.50 V, respectively. The steep slope of the HTFET provides significant improvement of g_m/I_{DS} to overcome the CMOS limit (40 V^{-1}) given

$$\frac{g_{m,HTFET}}{I_{DS}} = \frac{\partial I_{DS}}{\partial V_{GS}}\frac{1}{I_{DS}} = \frac{\partial \ln I_{DS}}{\partial V_{GS}} = \frac{\ln 10}{SS} > 40 \text{ V}^{-1}. \quad (6)$$

As discussed in Section II-A, high g_m/I_{DS} of HTFET can mitigate the power increase with V_{DD} scaling in analog components. Moreover, the tradeoff between g_m/I_{DS} (40 V^{-1} achieved in subthreshold regime) and f_T (peak f_T achieved in super-threshold regime) of CMOS [4], [5] can be further eliminated in HTFET due to the high g_m/I_{DS} (energy efficiency) and desired f_T (f_s requirement) can be achieved simultaneously.

Fig. 3(b) shows the f_T versus g_m/I_{DS} comparing between HTFET and Si FinFET, where f_T is calculated from $g_m/2\pi(C_{gs} + C_{gd})$. C_{gs} and C_{gd} are the gate-source and the gate-drain capacitances, respectively. Therefore, the HTFET can provide energy saving in both digital and analog components for low V_{DD} in terms of circuit speed, drive strength, and improved design space between operation point and bandwidth requirement, which is highly desirable for ultra-low power ADC design.

C. Device-Circuit Modeling Methodology

P-type TFET is required for complementary circuit design. However, the challenge in realizing III–V p-type HTFET (p-HTFET) still remains due to the low density of states in the conduction band of III–Vs, which leads to a large portion of the temperature dependent part of the source Fermi function participating in tunneling and a temperature dependent SS [20]. Here, we model a complementary III–V p-HTFET with symmetrical material system as III–V n-HTET, as shown in Fig. 4. The modeled p-HTFET shows degraded SS
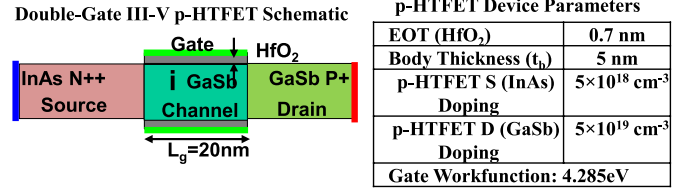
of 55 mV/dec over 2 decades of current change comparing with the n-HTFET at $V_{DD} = 0.30$ V (Table I).

To implement the HTFET based circuits, we have developed device-circuit co-design framework based on the Verilog-A models in Fig. 5 [9], [10], [12], [13], [21]. The HTFET Verilog-A model is built from 2-D lookup tables including I_{DS} (V_{GS}, V_{DS}), C_{gs} (V_{GS}, V_{DS}), and C_{gd} (V_{GS}, V_{DS}), which are obtained from fine-granularity simulation across a wide range of V_{DS} and V_{GS} using TCAD Sentaurus. Considering the circuit complexity and number of transistors (over 1100) in an ADC simulation, we omitted the drain–source capacitances C_{sd} given its relatively small value compared with C_{gs} and C_{gd} [28]. This simplification allows us to simulate the ADC within the simulation capability of the lookup table-based model [29]. In addition, the source and drain terminal charges, Q_S and Q_D, are computed with respect to the terminal voltages and capacitances, respectively, in transient analysis that preserves the charge conservation. Therefore, both dc and transient characteristics can be captured using this modeling method, which has also been applied by other works in [13], [23], and [24]. Furthermore, the recent work in [25] has reported the transient characteristics of the fabricated Si TFET inverter, showing enhanced ON-state

Fig. 6. (a) Principle block of 6-bit SAR ADC. (b) SAR ADC design transistor sizing: total transistor count versus device width and sizing strategy for critical analog and digital blocks.

Fig. 7. Sizing strategies of the logic gates. (a) HTFET. (b) Si FinFET.

Fig. 8. (a) HTFET and Si FinFET comparator schematic. (b) Delay with respect to input difference (LSB). (c) C_{gd} variations according to input difference (LSB). (d) Power consumption versus input difference (LSB).

Miller capacitance effect in TFET agreed with [26] from TCAD simulation. Bijesh *et al.* [14] have also confirmed the feasibility of the HTFET TCAD model for high-frequency performance analysis, showing good agreement of extracted capacitance values and f_T between simulation results and RF measurements.

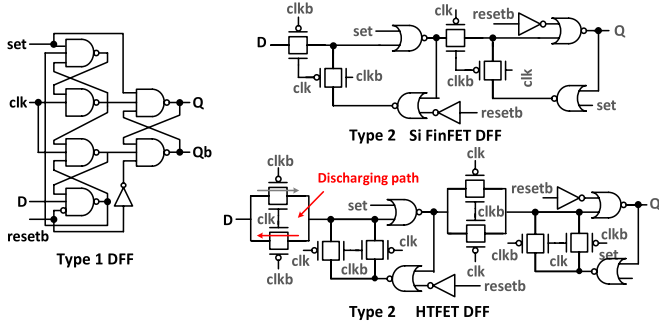Note that the frequency of the input signal, f_{in}, in our ADC design is between 50 and 400 KHz, and a sampling frequency, f_s, of 10 MS/s, which are significantly below the f_T of the transistor. Hence, the quasi-static assumption is fulfilled for our modeling technique.

To analyze the device noise effect on the SAR ADC performance (e.g., SNDR and power), we use the noise models developed in [21] for the HTFET and the baseline Si FinFET, including thermal, shot, and flicker noise. Table I shows the key device metrics for the ADC designs. We use the effective V_{th} of HTFET from the linear extrapolation of I_{DS}−V_{GS} for and overdrive voltage and transistor sizing estimation in the analog component. In the following sections, we implement the HTFET SAR ADC and perform the performance evaluation based on this Verilog-A model. We vary the transistor width W, while keeping L_g constant (20 nm) for transistor sizing.

III. HTFET 6-BIT SAR ADC DESIGN

Circuit design using HTFET requires certain modifications due to the change in the device architecture and characteristics [9], [10], [12]–[14]. The asymmetrical source/drain of the HTFET results in the unidirectional conduction characteristic, which requires the modification of pass transistor logic, latches, flip-flops, and so on [9], [10]. The low effective V_{th} due to the steep SS of HTFET also requires redesign of the comparator reference voltage and bias current circuitry to fulfill the timing difference. In this section, we will present the detailed design modification, sizing strategies, and performance analysis of each digital and analog block for the HTFET 6-bit SAR ADC.

A. Circuit Implementation of HTFET SAR ADC

Fig. 6(a) shows the principal blocks of HTFET 6-bit SAR ADC including the sample-and-hold (S/H) circuit, comparator, self-determined SAR control logic, and switched capacitor array operating as the feedback digital-to-analog converter (DAC).

The key challenge of designing SAR ADC using Si FinFET at a low V_{DD} is the accurate operation of the analog blocks (comparator and DAC) with the insufficient drive current at near/subthreshold. In addition, to meet the timing requirement in digital blocks and to compensate the voltage headroom reduction due to a low V_{DD} [4], [5], the new size strategy for Si FinFET has been adopted to use a smaller fan-out factor between logic gates, as shown in Fig. 7. To drive the same analog load (switches), the Si FinFET logic gates have an average size of around 6–7 times larger than the HTFET gates with given the device characteristics in Fig. 2(b). Some sizing adjustment in certain transistors is applied to realize the circuit functionality.

Circuit-level implementation and performance analysis are performed using Cadence Spectre [27] based on the Verilog-A modeling technique in Section II-C. The device models include the electrical noise (flicker, shot, and thermal) for both HTFET and Si FinFET. To explore the HTFET benefits at a low V_{DD}, as described in Section II-B, we focus on V_{DD} = 0.30, 0.40, and 0.50 V for circuit implementation at fixed f_s = 10 MS/s.

B. HTFET Comparator Design

A two-stage dynamic comparator in Fig. 7(a) is used due to its zero static biasing with double-gain stage to operate at a low V_{DD} [3]. Due to the steep slope characteristic of HTFET at a low V_{DD}, the simulated input offset voltage of the HTFET comparator is only 0.9 mV, which is much less than 9.5 mV in the Si FinFET comparator.

Fig. 8(b) shows two orders of magnitude reduction in delay and less delay variation over a wide range of input voltage are

Fig. 9. Two types of DFF schematics; standard and new design schematic.

Fig. 10. (a) Delay and (b) power consumption comparison between two types of both HTFET and Si FinFET DFFs.

observed in the HTFET comparator due to faster node voltage transition that reduces the nonlinearity and the quantization error in ADC. With comparable OFF-state leakage for the Si FinFET and HTFET. The Si FinFET comparator consumes higher dynamic power due to the increased capacitance from the up-sizing. Even though the enhanced ON-state Miller capacitance effect of HTFET [26] in Fig. 8(b) causes slightly dynamic power increase overall 3.5 times power reduction is achieved in the HTFET comparator over the Si FinFET comparator.

C. Feedback DAC

The feedback DAC is implemented with a binary-scaled charge-distribution topology [28]. Digital bits (D_0–D_5) from SAR drive the bottom of capacitors to generate the output of DAC. An overall capacitance 76.6 fF is used in our design to meet the thermal noise (kT/C) limitation [3], [4], [30], [31].

D. HTFET SAR Logic

Fig. 6(a) shows the SAR logic block as the main digital block, which generates the relevant control bits (D_0–D_5) from tracing the output of comparator. To avoid using an external frequency generator, SAR is constructed with D flip-flops (DFFs), and the clock-manage logic is utilized to set the enable signal from/to the comparator to generate internal clock signals [28]. Binary decoder in Fig. 6(a) is used to convert binary-scaled control bits into binary codes. It accepts control bits and an internal synchronous clock signal f_c (from SAR logic to generate the binary outputs).

Since DFF is the main component of digital blocks in SAR logic, the power reduction of the HTFET DFF dominates the overall power reduction of ADC. Two types of DFF designs are evaluated for energy efficiency optimization for SAR logic, as shown in Fig. 9. The HTFET logic gate DFF (Type 1) requires no design change, while the HTFET transmission gate DFF (Type 2) requires additional transistors for charging/ discharging of internal nodes due to its unidirectional conduction. Still, the HTFET DFF outperforms the Si FinFET DFF with lower power and delay. Between two types of DFF designs, type 1 DFF was utilized in this ADC design because type 1 DFF exhibits balanced performance, as shown in Fig. 10, in terms of delay and power consumption. Due to the 20 times current improvement of HTFET over Si FinFET at the low V_{DD} limit, both analog and digital blocks show
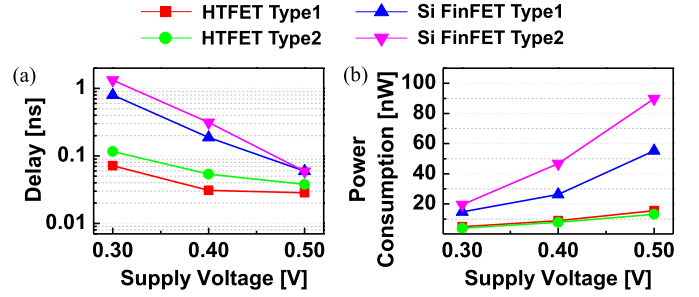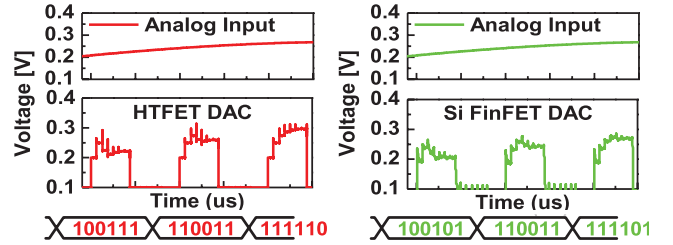

Fig. 11. ADC analog input. DAC output waveform analysis and output digits evaluation comparison between HTFET and Si FinFET ADCs at $V_{DD} = 0.30$ V.

the average 6 times reduction in transistor size and 3 times reduction in power consumption.

IV. ENERGY AND POWER EVALUATION

The single-ended SAR ADC design accepts an analog input ranging from 0 V to V_{DD} as a full-scaled input voltage. Fig. 11 shows the input waveform and digitized DAC output of both HTFET and Si FinFET ADCs at 0.30 V, where the HTFET ADC shows clear transitions of voltage steps as compared with Si FinFET ADC. An improved effective number of bits (ENOB) and SNDR with respect to the analog input frequency and supply voltage are achieved in the HTFET ADC, as shown in Fig. 12, due to the improved device drive strength at a low V_{DD} as compared with the Si FinFET ADC design. A continuous degradation with respect to the input frequency is observed for the Si FinFET design, due to the increased quantization errors with the increased nonlinearity, and the existence of electrical noise. Since flicker noise is dominant in megahertz frequency range (where white noise can be neglected), the reduced flicker noise in HTFET [21] leads to a slower degradation of ENOB and SNDR at lower input frequency than the Si FinFET ADC.

Energy per conversion-step has been widely used as figure of merit (FoM) of ADCs [3], [6], [28], [30]. As shown in Fig. 12(d), a FoM of 0.43 fJ/conversion-step is achieved in the HTFET ADC at 0.30 V, which is 3.8 times lower than 1.65 fJ/conversion-step of the Si FinFET ADC. Fig. 13 shows the differential nonlinearity (DNL) and the integral nonlinearity (INL) performance. The HTFET ADC shows the maximum +0.90/−2.1 LSB (DNL) and +1.0/−2.5 LSB (INL), which are 35.2% (DNL) and 5.2% (INL) lower compared with the Si FinFET ADC. This comes from the improved bit decisions
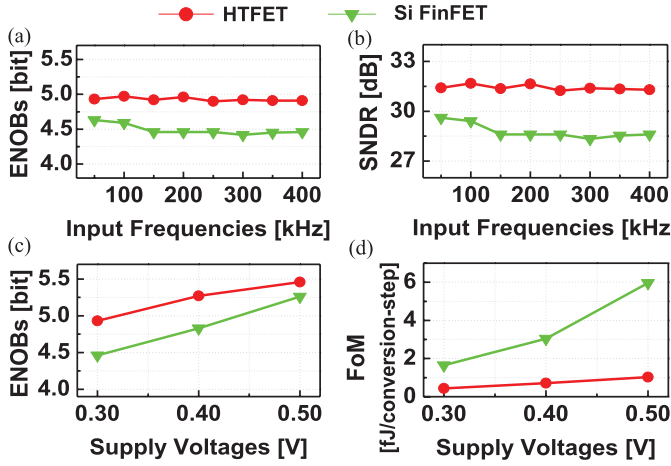
Fig. 12. Comparison of (a) ENOB and (b) SNDR versus input frequency. (c) ENOB and (d) FoM versus supply voltage for both HTFET and Si FinFET ADCs. The HTFET ADC shows higher ENOB and SNDR compared with Si FinFET ADC.
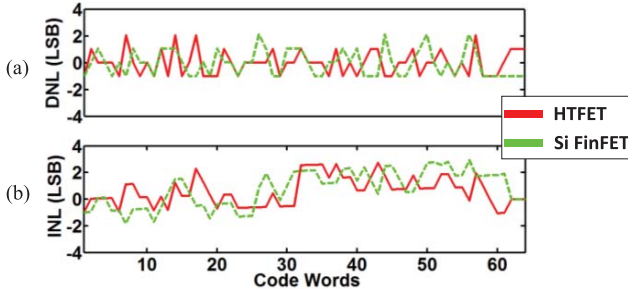

Fig. 13. (a) DNL and (b) INL analysis comparisons.

TABLE II
PERFORMANCE METRICS OF HTEFT AND Si FinFET SAR ADCs

	HTFET SAR ADC			Si FinFET SAR ADC		
V_{DD} [V]	0.30	0.40	0.50	0.30	0.40	0.50
Power [μW]	0.25	0.51	0.90	0.67	1.52	3.15
SNDR [dB]	31.4	33.5	34.6	28.6	30.9	33.5
ENOB [bit]	4.93	5.29	5.46	4.46	4.83	5.26
FoM [fJ/conversion-step]	0.43	0.71	1.03	1.65	3.04	5.26
P/fs [×10⁶]	3.19	6.76	11.0	8.84	21.0	49.0

of the HTFET comparator at very low input offset, as well as improved linearity due to the high drive current strength of HTFET. It is consistent with Fig. 11, where the output of DAC of HTFET shows reduced nonlinearity during sampling and amplification [1], [3], [30]. The static nonlinearity can be further improved with the calibration block and differential autozeroing DAC topology for the reduction of offset. The performance metrics are summarized in Table II at different V_{DD}.

Power analysis (Fig. 14) shows 3 times power reduction in majority of the digital and analog blocks in the HTFET over the Si FinFET ADCs, with SAR logic block being the most power hungry component. Energy (P/f_s) metrics for HTFET and Si FinFET ADCs are presented in Fig. 15. The energy for both ADC designs is lower than current technology boundary due to scaling and device performance improvement (for the Si FinFET and the HTFET). The energy consumption is between 8.84×10^6 and 49.0×10^6 kT in the range of
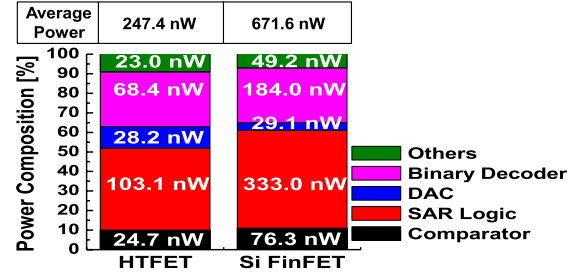

Fig. 14. HTFET and the Si FinFET SAR ADCs power analysis for analog and digital blocks at $V_{DD} = 0.30$ V. Digital blocks consume major power for the HTFET and Si FinFET ADCs. The HTFET ADC shows up to 3 times power reduction for each block comparing with Si FinFET ADC.
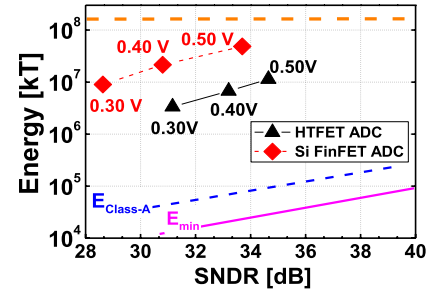

Fig. 15. Zoomed-in view of Fig. 1. Both HTFET and Si FinFET 6-bit SAR ADCs' energy versus SNDR evaluation for $V_{DD} = 0.30$, 0.40, and 0.50 V.

28.6 and 33.5 dB of SNDR, respectively, for the Si FinFET ADC design. The HTFET ADC shows remarkable reduction in energy ranging from 3.19×10^6 to 11.0×10^6 kT with higher a SNDR range of 31.4–34.6 dB, resulting from resizing of devices and higher g_m/I_{DS} at a low V_{DD}. The HTFET ADC design offers promise for further energy reduction capability and SNDR improvement toward the noise limit with improved energy efficiency.

V. CONCLUSION

Steep-slope HTFET based energy efficient 6-bit SAR ADC has been evaluated from the device to the circuit level. HTFET ADC shows significant improvement in energy efficiency compared with the Si FinFET ADC design baseline. We demonstrate the HTFET SAR ADC with 2.81 dB higher SNDR, 0.47-bit larger ENOB, 63% lower average power consumption and 26% lower energy per conversion-step (FoM). This performance advantage stems from increasing current strength due to steep-slope transistor characteristics and transistor size reduction, which is desirable for ultra-low power ADCs at $V_{DD} < 0.50$ V.

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Moon Seok Kim (S'13) received the B.S. degree in electronic engineering from Inha University, Incheon, Korea, in 2009, and the M.S. degree in electrical engineering from Northeastern University, Boston, MA, USA, in 2012. He is currently pursuing the Ph.D. degree with the Department of Computer Science and Engineering, Pennsylvania State University, University Park, PA, USA.
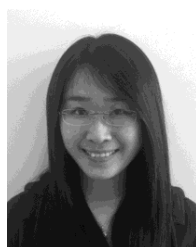
Huichu Liu (S'11) received the B.S. degree in microelectronics from Peking University, Beijing, China, in 2009. She is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Pennsylvania State University, University Park, PA, USA.

She has been a Research Assistant with Pennsylvania State University since 2009, and with the Nanoelectronic Devices and Circuits Laboratory and the Microsystem Design Laboratory since 2011.
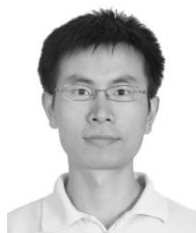
Xueqing Li (M'14) received the B.S. and Ph.D. degrees in electronics engineering from Tsinghua University, Beijing, China, in 2007 and 2013, respectively.

He has been a Post-Doctoral Researcher with the Department of Computer Science and Engineering, Pennsylvania State University, University Park, PA, USA, since 2013.

Suman Datta (F'13) received the B.S. degree in electrical engineering from IIT Kanpur, Kanpur, India, in 1995, and the Ph.D. degree in electrical and computer engineering from the University of Cincinnati, Cincinnati, OH, USA, in 1999.

He was the Joseph Monkowski Associate Professor of Electrical Engineering with Pennsylvania State University, University Park, PA, USA, in 2007, where he is currently a Professor of Electrical Engineering.
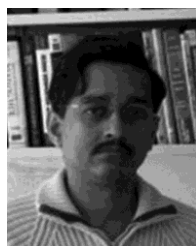
Vijaykrishnan Narayanan (F'11) received the B.S. degree in computer science and engineering from the University of Madras, Chennai, India, in 1993, and the Ph.D. degree in computer science and engineering from the University of South Florida, Tampa, FL, USA, in 1998.

He is currently a Professor of Computer Science and Engineering and Electrical Engineering with Pennsylvania State University, University Park, PA, USA.