HKMG Process Impact on N, P BTI: Role of Thermal IL Scaling, IL/HK Integration and Post HK Nitridation

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***Abstract*—NBTI and PBTI are studied in IL/HK/MG gate stacks having EOT down to $\sim 6\mathring{A}$ and fabricated using low T RTP based thermal IL and a novel IL/HK integration. At equivalent EOT, proposed stacks provide improved NBTI and similar PBTI when compared to conventional Chem-Ox IL based HKMG stacks. EOT scaling achieved by RTP thermal IL scaling shows lower rate of increase in NBTI and PBTI when compared to Chem-Ox IL scavenged stacks. Impact of Nitrogen and role of post HK nitridation are studied. Physical mechanism of improved BTI in proposed stacks is discussed in detail.**

***Index Terms*—HKMG, Chem-Ox IL, thermal IL, EOT scaling, IL scaling, gate leakage, mobility, NBTI, PBTI, flicker noise, DCIV, SILC, trap generation, charge trapping**

I. Introduction

Equivalent oxide thickness (EOT) scaling of MOSFET gate stacks, consisting of interfacial layer (IL), High-k (HK) and Metal Gate (MG), shown in Fig. 1, is necessary to maintain the electrostatic integrity of sub 20nm node CMOS devices [1]. EOT scaling is feasible only if scaled gate stacks show good gate leakage and mobility, as well as gate oxide reliability. To achieve desired reliability, qualities of IL, IL/HK interface and HK have to be carefully controlled. Scaling Atomic Layer Deposition (ALD) based Hafnium Oxide (HfOx) HK below its present thickness of $\sim 17\mathring{A}$ is not beneficial. Therefore, further EOT scaling must be achieved by IL thickness scaling.

Conventional Chemical Oxide (Chem-Ox) IL is formed by wet chemistry at near room temperature (RT) [2]. EOT scaling is achieved via the scavenging technique [3], and those stacks show good gate leakage and mobility. However, IL scaling by Chem-Ox scavenging shows drastic increase in Negative (N) and Positive (P) Bias Temperature Instability (BTI) [4], as 2X increase in V_T shift (ΔV_T) is observed for every $1\mathring{A}$ reduction in EOT. This poses a critical challenge to EOT scaling for sub 20nm technology nodes and must be addressed. Recently, gate stack fabrication has been demonstrated [5] in a cluster tool system that integrates RTP based thermal IL [6] and ALD HfOx without air-break. These stacks show EOT scaling down to $6\mathring{A}$, with similar gate leakage and mobility but much improved BTI as compared to Chem-Ox IL scavenged stacks. In this work, NBTI and PBTI of these novel gate stacks are further studied in detail, and the impact of different gate insulator processes are explored. The physical mechanisms responsible for NBTI and PBTI improvement are analyzed. The paper is divided into seven sections. Details of device fabrication, physical characterization and time-zero electrical measurements for gate leakage and mobility are discussed in section II. NBTI and PBTI measurements and related analysis are discussed in section III, and basic N, P BTI models are discussed. The impact of gate insulator processes on N and P BTI are discussed in Sections IV and V respectively. The impact of IL scaling is discussed in section VI, followed by conclusions in section VII.

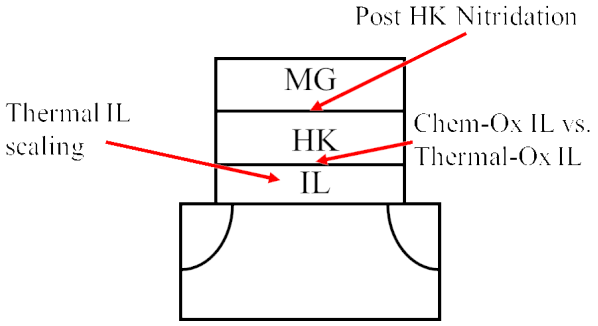

Fig. 1. Different gate insulator processes studied in this work: (a) Comparison of Chem-Ox IL versus Thermal IL, and impact of (b) Post HK Nitridation and (c) IL Scaling.

II. Fabrication Details

Full flow CMOS devices with different IL and ALD HfOx HK, as shown in Fig. 2, have been fabricated in the Gate First integration scheme. As a reference, Chem-Ox IL devices were processed by using RT wet chemistry followed by standard 8 hour air-break prior to ALD HfOx deposition. Other stacks were processed in a novel cluster tool system, which includes

low T RTP based thermal IL and ALD HfOx under controlled vacuum environment. Low T RTP is used for the formation of ultra-thin IL (UT-IL) down to $3\mathring{A}$ and mono-layer IL (ML-IL) having thickness below $3\mathring{A}$. ML-IL stacks have novel Si top surface passivation using nitrogen (N), and different N species have been used in ML-IL 1 and ML-IL 2 stacks. Extreme EOT scaling down to $\sim 6\mathring{A}$ is achieved by ML-IL process. Post HK nitridation (PHKN) of Chem-Ox and UT IL stacks has been done using Decoupled Plasma Nitridation (DPN) followed by Post Nitridation Anneal (PNA) [7]. Gate stack formation is completed by TiN MG and poly-Si deposition, and is followed by gate patterning and Source/Drain formation to complete the transistor process.

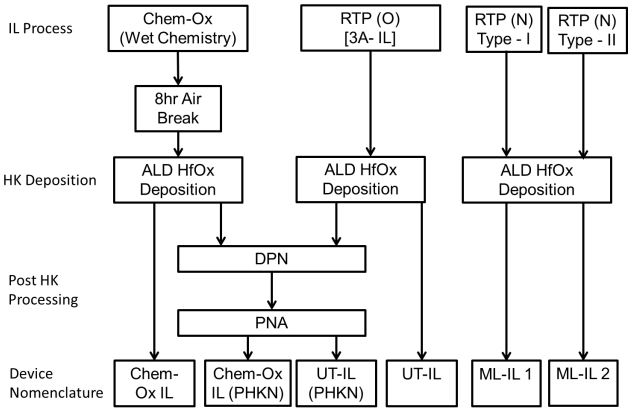

Fig. 2. Block diagram of different gate insulator process flows.

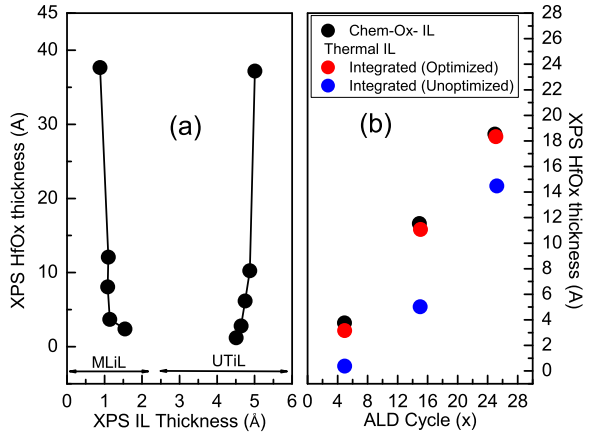

Fig. 3. XPS measurements of (a) UT-IL and ML-IL thickness growth during subsequent ALD HfOx deposition and (b) ALD HfOx growth on Chem-Ox, un-optimized and optimized UT-IL. All thermal ILs are grown in a cluster tool with no vacuum break between IL and HK.

Integration of IL and HK without air-break in a cluster tool system helps avoid the commonly encountered problem of IL thickening during ALD HK deposition. It is evident from X-ray Photoelectron Spectroscopy (XPS) measurements shown in Fig. 3(a) that UT-IL and ML-IL thicknesses remain constant with subsequent ALD HK deposition. The cluster tool system has a novel in-situ IL top surface hydration that

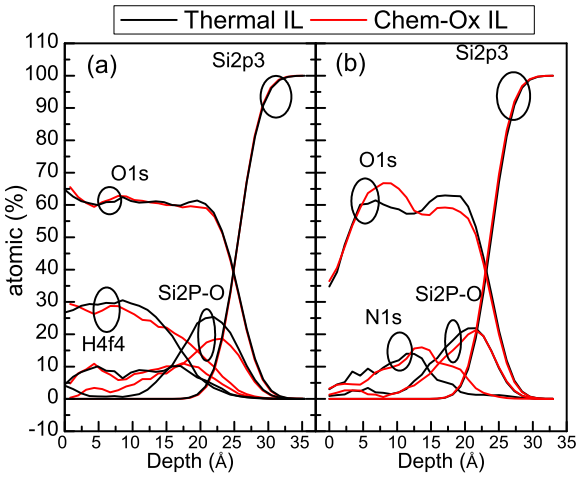

Fig. 4. ARXPS measurements to demonstrate (a) Hf and O intermixing and (b) N penetration following PHKN for Chem-Ox and UT-IL stacks.

ensures proper ALD HK growth on thermal IL similar to that on Chem-Ox. As evident from XPS measurements shown in Fig. 3(b), Chem-Ox and optimized thermal IL has identical ALD HK growth, while non-optimized thermal IL shows lower HK growth, with increase in ALD cycles. Thermal IL has reduced Hf and O intermixing compared to Chem-Ox IL, as evident from Angle Resolved (AR) XPS measurements shown in Fig. 4(a), where both Si2P-O and H4f4 signals show lower peak and larger tail for Chem-Ox IL compared to thermal IL. Chem-Ox IL is more porous in nature w.r.t thermal IL, evident from ARXPS shown in Fig. 4(b), where Chem-Ox IL+PHKN stack shows larger N1s tail compared to thermal IL+PHKN stack. Due to this porous nature, higher N penetration into IL is expected from TiN gate for Chem-Ox IL compared to thermal IL, even when not subjected to PHKN. Transmission Electron Micrograph (TEM) shows clear transition from SiO_2 to HfOx for both UT-IL and extremely scaled ML-IL stacks as evident from Fig. 5. UT-IL & ML-IL stacks show similar time-zero performance as Chem-Ox IL, evident from inversion gate leakage (J_{INV}) versus Capacitance Equivalent Thickness (CET) trend as shown in Fig.6(a) and mobility versus CET trend as shown in Fig.6(b).

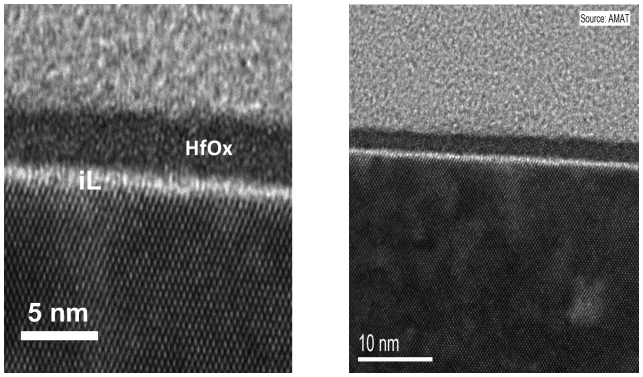

Fig. 5. XTEM of (left) UT-IL/HfOx and (right) ML-IL/HfOx stacks.

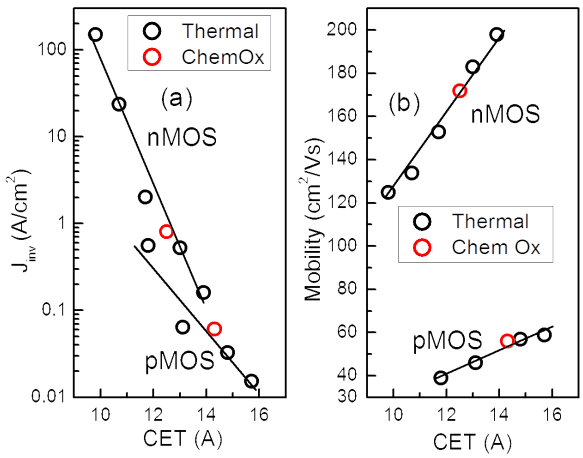

Fig. 6. (a) Gate leakage and (b) mobility as a function of CET measured in n- and p- MOSFETs having differently processed gate stacks. Mobility extraction is done at E_{OX} = 0.8MV/cm.

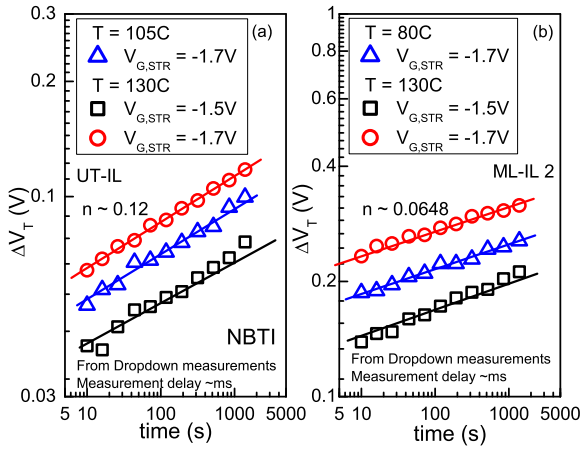

Fig. 7. Time evolution of ΔV_{IT} for (a) UT-IL and (b) ML-IL 2 stacks under NBTI stress at different $V_{G,STR}$ and T. UT-IL thickness is 3Å, ML-IL thickness is below 3Å.

III. BTI Measurement and Analysis

Time evolution of ΔV_T during N and P BTI stress is studied using the single-point drop down (from stress V_G ($V_{G,STR}$) to $V_G = V_{DD}$) method [8] with a measurement delay of 1ms. Note that ΔV_T during N and P BTI can generally be attributed to trap generation (TG) and trapping in pre-existing defects (TP) [5], [9]–[11]. TG at or near the Si/IL interface during N, P BTI stress is studied using Direct Current IV (DCIV) method [12] in measure-stress-measure (MSM) mode with a measurement delay of seconds. Transconductance degradation (Δg_m) due to TG at or very close to the Si/IL interface and its correlation to ΔV_T is extracted from transfer IV measured in MSM mode. Stress Induced Leakage Current (SILC) during PBTI stress, presumably due to TG near the IL/HK interface [13] or in the HK bulk [14], is measured using carrier separation technique [15] in MSM mode. Process induced (pre-stress) gate insulator traps in N and P MOSFETs (that facilitates TP) are estimated using flicker noise [5], [16], [17].

Figs. 7 and 8 show the time evolution of ΔV_T respectively during N and P BTI stress for different stress voltage ($V_{G,STR}$) and temperature (T) for (a) UT-IL and (b) ML-IL gate stacks. ΔV_T shows power law time dependence for both N and P BTI and also for both UT-IL and ML-IL gate stacks. For a given device, time exponent (n) remains invariant across different stress conditions ($V_{G,STR}$ and T), which is true for both N and P BTI. However, ML-IL stacks show lower n compared to UT-IL for both N and P BTI stress. Reduction in n for the ML-IL stacks is due to its relatively higher density of pre-existing defects (higher TP) and is discussed later in this paper.

Figs. 9 and 10 show the time evolution of $\Delta I_{DCIV}/I_{DCIV0}$ from DCIV measurements respectively during N and P BTI stress for different $V_{G,STR}$ and T for (a) UT-IL and (b) ML-IL gate stacks. DCIV current (I_{DCIV}) arises out of recombination of electrons and holes in traps [12] at or near the Si/IL interface, and increase in I_{DCIV} after stress clearly

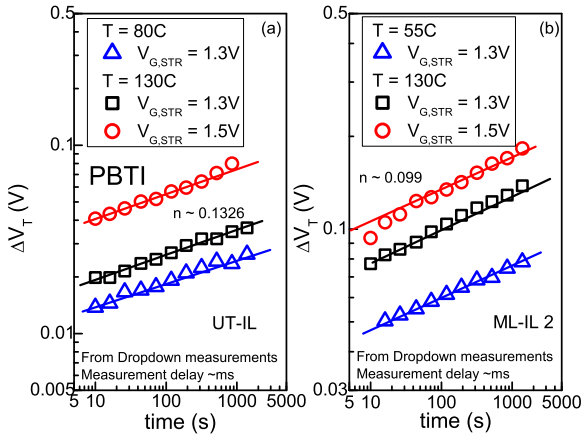

Fig. 8. Time evolution of ΔV_T for (a) UT-IL and (b) ML-IL 2 stacks under PBTI stress at different $V_{G,STR}$ and T. IL thicknesses are mentioned in Fig.7.

indicates the presence of TG during both N and P BTI, and also for both UT-IL and ML-IL gate stacks. Once again, power-law time dependence is observed, with similar n across different $V_{G,STR}$ and T for a particular device, and lower n for ML-IL compared to UT-IL stacks, for both N and P BTI. Note, as DCIV measurements are done in the MSM mode, recovery during measurement (stress-off) time results in higher measured n than actual, and differences in recovery magnitude would likely result in different n in different devices.

Fig. 11 shows time evolution of SILC during PBTI stress for different $V_{G,STR}$ and T. It is well-known that SILC is due to trap assisted tunneling and increase in SILC clearly indicates TG, although some debate exists regarding the exact location of these generated traps [13], [14]. Once again, a power law time dependence is observed, although with n that is much larger than that for ΔV_T and DCIV measurements. Note, SILC in HKMG stacks shows recovery [10], [14] and would result in higher n than actual when measured in the MSM mode. However, this recovery artifact is unlikely to be responsible for such large differences seen between SILC and PBTI ΔV_T

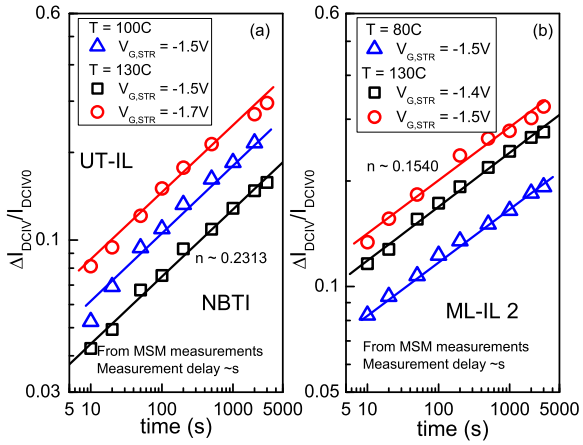

Fig. 9. Time evolution of TG from DCIV for (a) UT-IL and (b) ML-IL 2 stacks under NBTI stress at different $V_{G,STR}$ and T. IL thicknesses are mentioned in Fig.7.

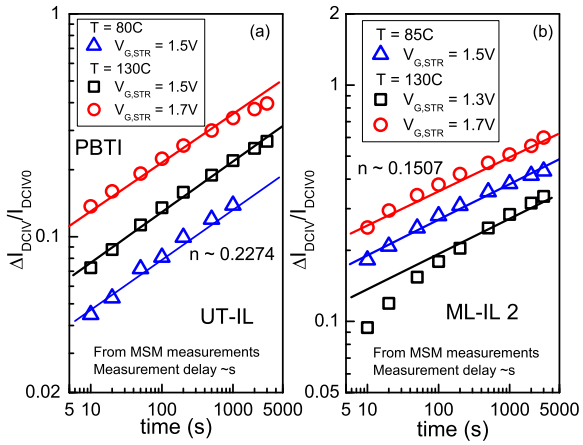

Fig. 10. Time evolution of TG from DCIV for (a) UT-IL and (b) ML-IL 2 stacks under PBTI stress at different $V_{G,STR}$ and T. IL thicknesses are mentioned in Fig.7.

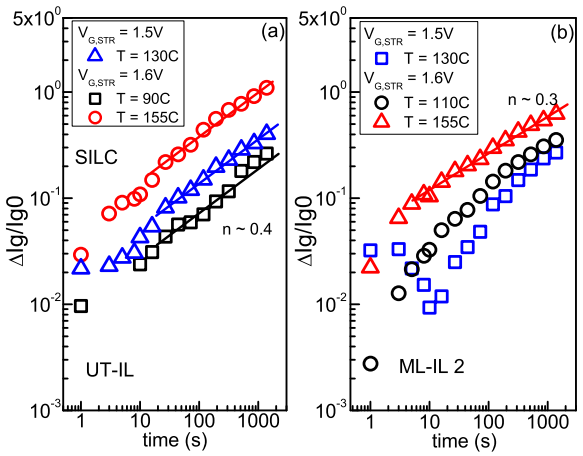

Fig. 11. Time evolution TG from SILC under PBTI Stress for (a) UT-IL and (b) ML-IL 2 stacks at different $V_{G,STR}$ and T. IL thicknesses are mentioned in Fig.7.

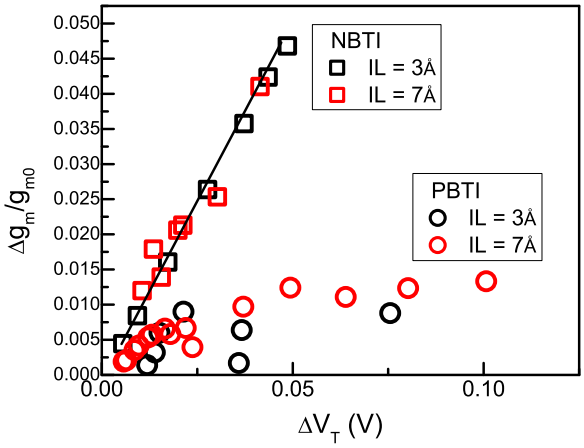

Fig. 12. Correlation of g_m degradation to ΔV_T for gate stacks having different IL thickness under NBTI and PBTI stress.

data, and more work is needed to understand these differences. Similar to that shown in [18], negative SILC is observed at shorter time, although for low $V_{G,STR}$ and T and only in ML-IL stack (Fig. 11(b)) having relatively larger pre-existing bulk trap density that facilitates TP. This is discussed later in this paper.

Fig. 12 shows the correlation of Δg_m to ΔV_T during N and P BTI stress for Chem-Ox and UT-IL stacks. NBTI results in g_m degradation in HKMG stacks (similar to that in SiON devices, which is now well-known), and identical correlation of Δg_m to ΔV_T is observed for thicker and thinner IL gate stacks, which is fully consistent with NBTI being dominated by TG at Si/IL interface when obtained from slow MSM IV data. TG at Si/IL interface is naturally probed by DCIV [12] as shown in Fig. 9. However, PBTI stress shows no appreciable Δg_m for both thick and thin IL gate stacks and indicates negligible IL degradation [10], [19], which is also fully consistent with negligible PBTI in SiON devices. Therefore, we speculate that the location of TG in HKMG stacks as probed by the DCIV method during PBTI stress (see Fig. 10) is at or very near the IL/HK interface (towards HK and further away from the channel), although this assumption needs further assessment.

Fig. 13 shows ΔV_T and $\Delta I_{DCIV}/I_{DCIV0}$ as a function $V_{G,STR}$ and T during NBTI stress for Chem-Ox IL and UT-IL devices. ΔV_T and DCIV show similar $V_{G,STR}$ acceleration (Γ) for both devices, similar T activation (E_A) for UT-IL, while ΔV_T shows slightly lower E_A compared to DCIV for Chem-Ox. Note, it is now well established in SiON stacks that NBTI is due to generation of interface traps (ΔN_{IT}), hole trapping in process related traps (ΔN_{HT}) and bulk trap generation (ΔN_{OT}) [9], [10], and all components are mutually uncorrelated. Along similar lines, NBTI in HKMG is primarily due to ΔN_{IT} (TG at Si/IL interface, independently probed by DCIV) and ΔN_{HT} (TP in IL hole traps, relative magnitude of traps estimated from flicker noise), while ΔN_{OT} is negligible due to low V_G drop across IL (as $V_{G,STR}$ gets divided into drops across HK and IL, and as ΔN_{OT} has strong V_G de-acceleration [9], [10]). Since ΔN_{IT} and ΔN_{HT} has similar Γ [9], [10], ΔV_T ($\sim \Delta N_{IT} + \Delta N_{HT}$) and DCIV ($\sim \Delta N_{IT}$) show similar Γ for both devices. As ΔN_{HT} has lower E_A

than ΔN_{IT} [9], relatively higher ΔN_{HT} in Chem-Ox IL stack (discussed in detail in section IV) results in lower E_A for ΔV_T compared to DCIV. Similar E_A for ΔV_T and DCIV for UT-IL stack suggests low ΔN_{HT} in these stacks (discussed in detail in section IV). Finally as ΔN_{HT} saturates at longer stress time [9], relatively higher ΔN_{HT} contribution would reduce the long time *n* of overall ΔV_T as shown in Fig. 7 and is also discussed in detail in section IV.

To understand and model the gate insulator process impact, NBTI ΔV_T data is decomposed into underlying ΔN_{IT}, ΔN_{HT} and ΔN_{OT} components (ΔN_{OT} has negligible contribution in HKMG stacks) by using a simple, closed form NBTI model [10], [20] as shown in Table-I. The model is physically based (H/H2 RD model for ΔN_{IT} and 2 energy well model for ΔN_{HT} [9]) and uses only 4 device dependent parameters (effectively 3 parameters for HKMG as ΔN_{OT} is negligible) to predict long time ΔV_T time evolution for different T, $V_{G,STR}$, and different gate stacks. The model can explain both SiON and HKMG data with consistent set of model parameters, refer to [10], [20], [21] for more details. Fig. 14 shows measured data and model prediction, together with underlying components, for (a) UT-IL and (b) ML-IL devices, and for different $V_{G,STR}$ and T for (c) UT-IL and (d) ML-IL devices. Similar exercise is done for all gate stacks and used in section IV to explain NBTI process dependence.

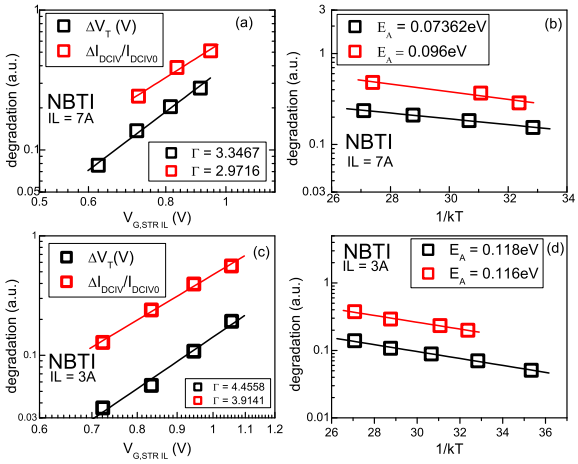

Fig. 13. Measured ΔV_T and TG from DCIV for thick and thin IL gate stacks during NBTI stress as a function of $V_{G,STR}$ (across IL) and T.

TABLE I
SIMPLIFIED NBTI MODEL

For Stress		
$\Delta N_{IT} = A(V_G - V_{T0} - \Delta V_T)^{\Gamma_{IT}} e^{-\frac{E_{AIT}}{kT}} t^{\frac{1}{6}}$		
where $E_{AIT} = (\frac{2}{3}(E_{Akf} - E_{Akr}) + \frac{E_{ADH2}}{6})$		
$\Delta N_{HT} = B(V_G - V_{T0} - \Delta V_T)^{\Gamma_{HT}} e^{-\frac{E_{AHT}}{kT}}$		
$\Delta N_{OT} = C(1 - e^{(-(\frac{t}{n})^{\beta_{OT}})})$		
where: $n = \eta(V_G - V_{T0} - \Delta V_T)^{-\frac{\Gamma_{OT}}{\beta_{OT}}} e^{(\frac{E_{AOT}}{kT\beta_{OT}})}$		
A, B, C & $\Gamma_{IT}(=\Gamma_{HT})$ are variable across devices		
Fixed Parameters (constant across devices)		
E_{Akf} = 0.175eV	E_{Akr} = 0.2eV	E_{ADH2} = 0.6eV
E_{AHT} = 0.03eV	E_{AOT} = 0.15eV	β_{OT}=0.36eV
Γ_{OT} = 9	η = 5x10^{12}	
For details refer [10] & [20]		

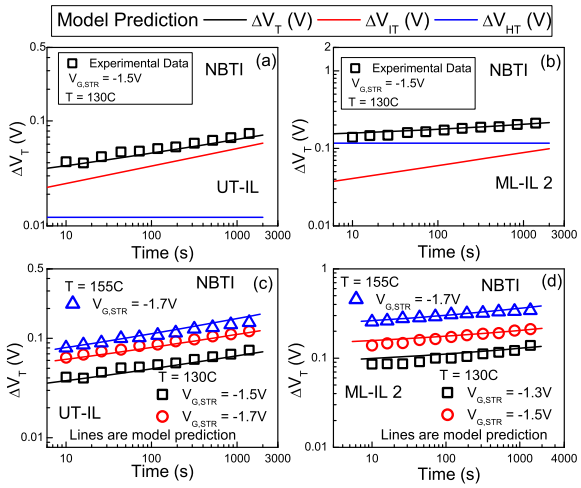

Fig. 14. Measured ΔV_T and model prediction during NBTI stress on UT-IL and ML-IL2 stacks, where (a, b) underlying ΔV_{IT} and ΔV_{HT} components are shown, and (c, d) prediction shown for different $V_{G,STR}$ and T. ΔN_{OT} under these stress conditions is negligible and not shown. NBTI model shown in Table-I has been used. IL thicknesses are mentioned in Fig.7.

Fig. 15 shows ΔV_T, DCIV and SILC data as a function of $V_{G,STR}$ and T during PBTI stress in Chem-Ox and UT-IL devices. SILC shows much larger Γ and E_A compared to ΔV_T and DCIV for both devices. ΔV_T shows slightly higher Γ and slightly smaller E_A compared to DCIV. As PBTI shows no IL degradation, TG probed by DCIV and SILC must come from that in IL/HK interface and/or HK bulk. Very different *n*, E_A and Γ for TG probed by DCIV and SILC suggest two different types of traps. It has been proposed [10] that DCIV probes TG at the IL/HK interface (ΔN_{IT-HK}) and SILC probes TG in the HK bulk (ΔN_{OT-HK}) [14]. As shown in [10], [11], ΔV_T during PBTI consists of TG together with TP due to electron trapping in HK bulk traps (ΔN_{ET}). Assuming similar Γ for ΔN_{IT-HK} and ΔN_{ET}, higher Γ for ΔV_T ($\sim \Delta N_{IT-HK} + \Delta N_{ET} + \Delta N_{OT-HK}$) when compared to DCIV ($\sim N_{IT-HK}$) is attributed to the contribution due to ΔN_{OT-HK} (probed by SILC). Lower E_A for ΔV_T when compared to DCIV can be explained by assuming a much lower E_A for ΔN_{ET} (electron trapping in HK bulk traps).

To understand and model the gate insulator process impact,

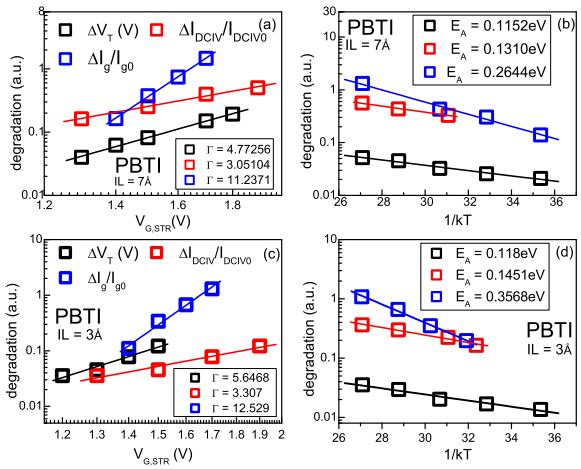

Fig. 15. Measured ΔV_T and TG from both DCIV and SILC for thick and thin IL gate stacks during PBTI stress as a function of $V_{G,STR}$ and T.

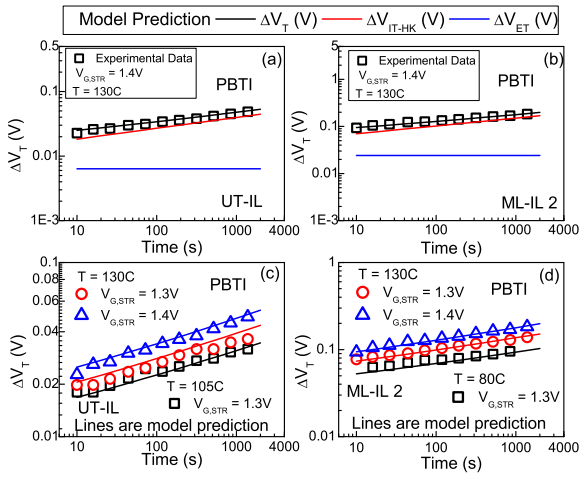

Fig. 16. Measured ΔV_T and model prediction during PBTI stress on UT-IL and ML-IL2 stacks, where (a, b) underlying ΔV_{IT-HK} and ΔV_{ET} components are shown, and (c, d) prediction shown for different $V_{G,STR}$ and T. ΔN_{OT-HK} under these stress conditions is negligible and not shown. PBTI model shown in Table-II has been used. IL thicknesses are mentioned in Fig.7.

PBTI ΔV_T data is decomposed into underlying ΔN_{IT-HK}, ΔN_{ET} and ΔN_{OT-HK} components using a simple, closed form model [10], [11] as shown in Table-II. The model uses only 6 device dependent parameters to predict long time ΔV_T time evolution across different T, $V_{G,STR}$, and different gate stacks. It should be noted that unlike NBTI, more work is needed to understand the physical mechanism responsible for TG and TP in PBTI, which is beyond the scope of the present paper. Fig. 16 shows measured data and model prediction, together with underlying components, for (a) UT-IL and (b) ML-IL devices, and for different $V_{G,STR}$ and T for (c) UT-IL and (d) ML-IL devices. Similar exercise is done for all gate stacks and used in section V to explain PBTI process dependence. The model, although empirical, can predict ΔV_T data obtained for different $V_{G,STR}$ and T and across different gate stacks with consistent set of model parameters (see [10] for further details).

TABLE II
PBTI EMPIRICAL MODEL

For Stress		
$\Delta N_{IT-HK} = A(V_{G-HK})^{\Gamma_{IT-HK}} e^{-\frac{E_{AIT-HK}}{kT}} t^{\frac{1}{6}}$		
$\Delta N_{ET} = B(V_{G-HK})^{\Gamma_{ET}} e^{-\frac{E_{A-ET}}{kT}}$		
$\Delta N_{OT-HK} = C(1 - e^{(-(\frac{t}{n})^{\beta_{OT-HK}})})$ where: $n = \eta(V_{G-HK})^{-\frac{\Gamma_{OT-HK}}{\beta_{OT-HK}}} e^{(\frac{E_{AOT-HK}}{kT\beta_{OT-HK}})}$		
A, B, C, Γ_{IT-HK}, Γ_{ET} and E_{AIT-HK} are variable across devices		
Fixed Parameters (constant across devices)		
E_{A-ET} = 0.03eV	E_{AOT-HK} = 0.52eV	β_{OT}=0.36eV
Γ_{OT-HK} = 15	η = 5x10^{12}	
For details refer [10]		

IV. Gate Insulator Process Impact on NBTI

Fig. 17 shows gate oxide field (E_{OX}) dependence of (a) ΔV_T and (b) TG from DCIV ($\Delta I_{DCIV}/I_{DCIV0}$) during NBTI for Chem-Ox and UT-IL stacks without and with PHKN. UT-IL shows 2X lower ΔV_T and similar (slightly lower) TG w.r.t Chem-Ox IL. PHKN of both stacks increases ΔV_T; UT-IL+PHKN still has lower ΔV_T w.r.t Chem-Ox IL+PHKN. PHKN results in reduction in TG for UT-IL but increase in TG for Chem-Ox IL. Fig. 17(c) shows correlation of ΔV_T to TG for these stacks, indicating higher TP contribution for Chem-Ox IL compared to UT-IL, and also higher TP contribution for stacks subjected to PHKN. Relative magnitude of TP is fully consistent with IL trap density estimated using flicker noise, shown in Fig. 17(d). Note, higher hole trap density for Chem-Ox IL is due to larger Hf-O intermixing and larger N penetration from TiN gate as Chem-Ox IL is porous in nature. Higher hole trap density for Chem-Ox IL and for gate stacks subjected to PHKN is fully consistent with SiON results [9], [10], [20]–[23]. The physical mechanism responsible for higher hole traps due to presence of Hf and N in SiO_2 IL needs further study and is beyond the scope of the present paper.

Fig. 18(a) shows experimental parameters for stacks used in Fig. 17. Of particular interest is n and E_A, which are found to be lower for Chem-Ox IL w.r.t UT-IL, and lower values are seen for PHKN stacks. Fig. 18(b) shows ΔV_T and extracted ΔV_{IT} ($= q\Delta N_{IT}/CET$) and ΔV_{HT} ($= q\Delta N_{HT}/CET$), obtained using the model described in Table-I. Relatively higher contribution from ΔV_{HT} (which saturates at long time and has lower E_A) is seen for Chem-Ox IL compared to UT-IL and also for PHKN stacks, and can explain lower n and E_A values for these stacks. Chem-Ox IL has lower Γ compared to UT-IL, and can be due to higher N penetration owing to its porous nature. Note, it is well known from SiON data that

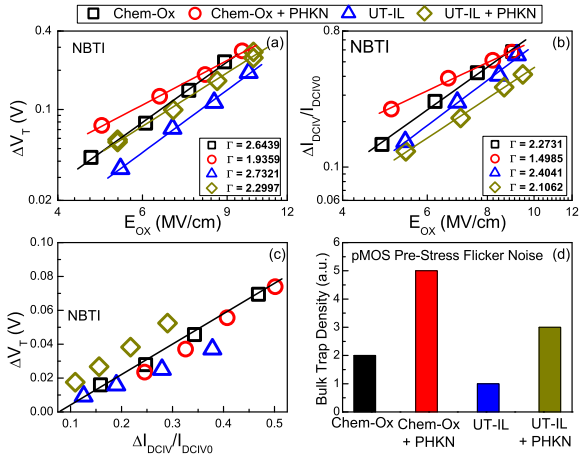

Fig. 17. Impact of IL processes (Chem-Ox IL , UT-IL) and PHKN on NBTI: E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV; (c) correlation of TG and ΔV_T; (d) pre-stress IL hole trap density from flicker noise. UT-IL thicknesses is $3\mathring{A}$.

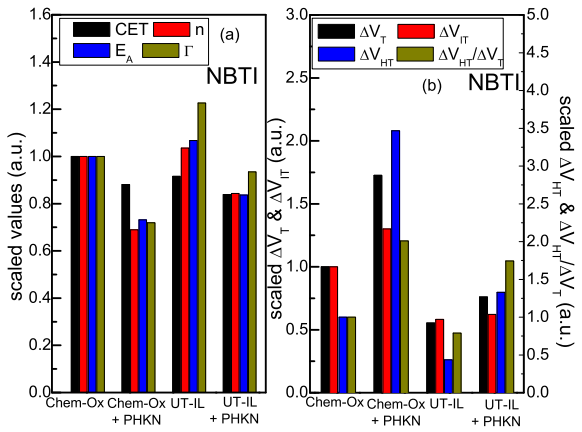

Fig. 18. Impact of IL processes (Chem-Ox IL , UT-IL) and PHKN on NBTI: (a) CET and measured NBTI parameters n, E_A, Γ; (b) measured ΔV_T and extracted TG (ΔV_{IT}) and TP (ΔV_{HT}) components at E_{OX} = 7MV/cm, T = 130^0C and t-stress = 1000s. Components are extracted using the NBTI model shown in Table-I. UT-IL thickness is $3\mathring{A}$.

higher N close to the Si/SiO_2 interface results in reduction in Γ [22], [23]. PHKN causes reduction in Γ as shown, which is also consistent with SiON results, see [22] , [23] for details.

Fig. 19 shows E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during NBTI for UT-IL stacks having different IL and HK thicknesses. Identical ΔV_T (when normalized to CET) and TG are observed across all stacks, which clearly indicates very low TP in UT-IL. Low process induced hole traps in UT-IL is attributed to lower Hf-O intermixing resulting in clear IL/HK transition, and also denser quality of thermal IL that prevents N penetration from TiN gate, as discussed in section II, and is consistent with higher Γ observed for these stacks.

Fig. 20 shows E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during NBTI for UT-IL and ML-IL stacks (ML-IL2 has $1\mathring{A}$ lower CET compared to ML-IL 1 stack). ML-IL stacks are fabricated using N surface passivation and show higher ΔV_T but lower TG compared to UT-IL, and the trend is similar to the comparison between UT-IL and UT-IL+PHKN

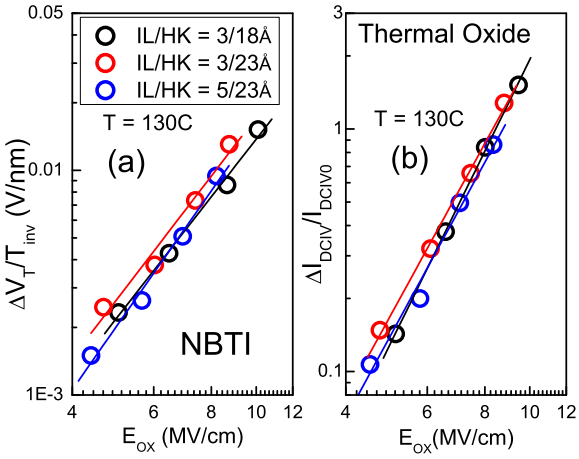

Fig. 19. E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during NBTI in UT-IL stacks having different IL and HK thickness.

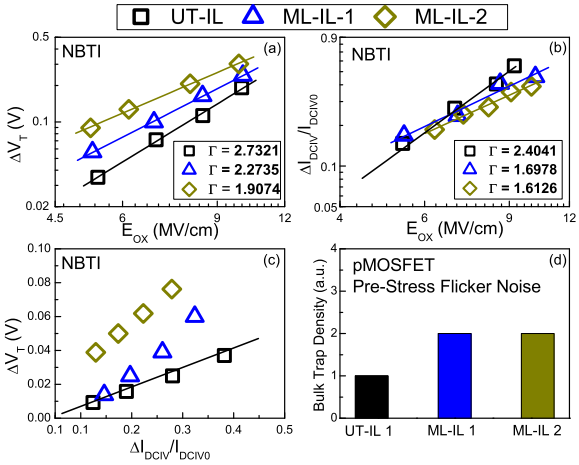

Fig. 20. Impact of N based IL scaling on NBTI: E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV; (c) correlation of TG and ΔV_T; (d) pre-stress IL hole trap density from flicker noise. IL thicknesses are mentioned in Fig.7.

stacks as shown in Fig. 17. Fig. 20(c) shows correlation of ΔV_T to TG for these stacks, indicating higher TP contribution for N based ML-IL, which is consistent with IL hole trap density extracted from flicker noise as shown in Fig. 20(d), and also with SiON results [22], [23].

Fig. 21(a) shows experimental parameters for stacks used in Fig. 20, and ΔV_T along with extracted NBTI components (ΔV_{IT} and ΔV_{HT}) are shown in Fig. 21(b). N containing ML-IL stacks show lower n, E_A and Γ, which is consistent with PHKN results shown in Fig. 18 and also consistent with SiON results [23]. Higher relative ΔV_{HT} contribution extracted for ML-IL stacks (see Fig. 21(b)) is fully consistent with reduced n and E_A observed in these stacks.

V. Gate Insulator Process Impact on PBTI

Fig. 22 shows E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during PBTI for Chem-Ox and UT-IL stacks. HK bulk trap density as obtained from pre-stress flicker noise is shown in the inset of Fig. 22(b). Similar ΔV_T, TG and electron

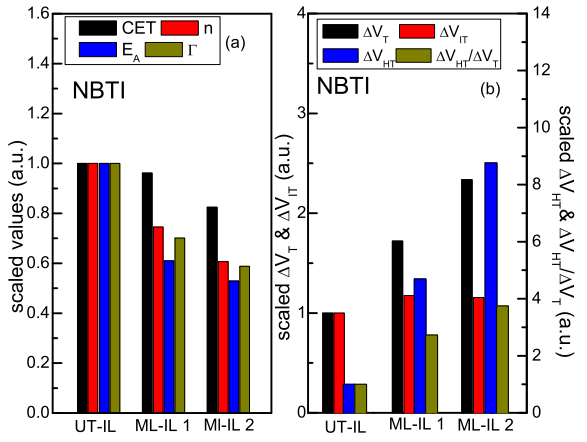

Fig. 21. Impact of N based IL scaling on NBTI: (a) CET and measured NBTI parameters n, E_A, Γ; (b) measured ΔV_T and extracted TG (ΔV_{IT}) and TP (ΔV_{HT}) components at E_{OX} = 7MV/cm, T = 130^0C and t-stress = 1000s. Components are extracted using the NBTI model shown in Table-I. IL thicknesses are mentioned in Fig.7.

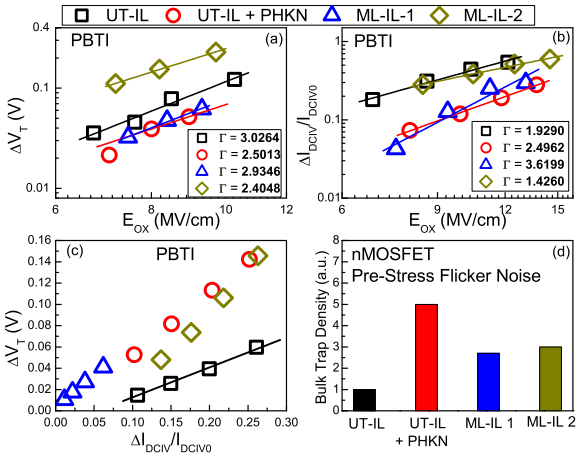

Fig. 23. Impact of PHKN and N based IL scaling on PBTI: E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV; (c) correlation of TG and ΔV_T; (d) pre-stress HK electron trap density from flicker noise. IL thicknesses are mentioned in Fig.7.

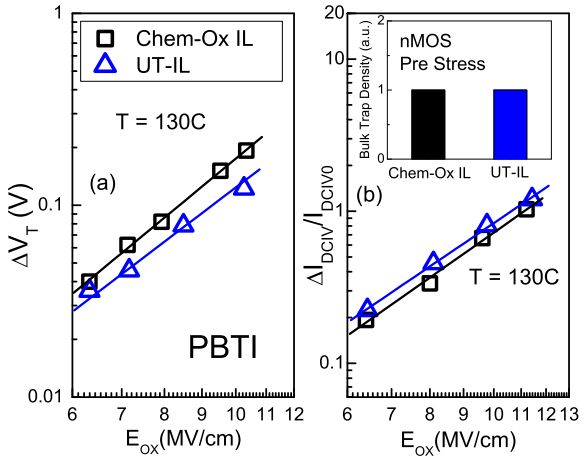

Fig. 22. E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during PBTI in Chem-Ox IL and UT-IL stacks. Inset shows pre-stress HK electron trap density from flicker noise. UT-IL thicknesses is $3\mathring{A}$.

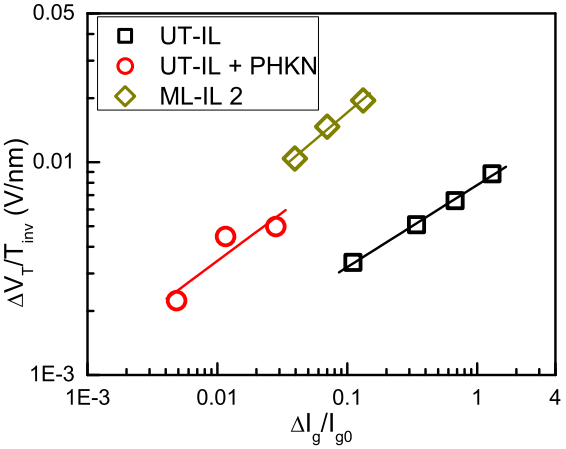

Fig. 24. Impact of PHKN and N based IL scaling on PBTI: Correlation of ΔV_T to TG from SILC. IL thicknesses are mentioned in Fig.7.

trap density in HK bulk are observed for both stacks [5], which suggests similar HK quality between both stacks and clearly demonstrates the effectiveness of the in-situ hydration process

Fig. 23 shows E_{OX} dependence of (a) ΔV_T and (b) TG from DCIV during PBTI for UT-IL, UT-IL+PHKN and ML-IL gate stacks. Presence of N results in reduction in ΔV_T (compared to UT-IL) as can be seen from PHKN and ML-IL 1 stacks, only extremely scaled ML-IL 2 stack shows increase in ΔV_T. Similar trends are observed for TG, with reduction (compared to UT-IL) seen for PHKN and ML-IL1 stacks and increase for ML-IL2 stack (see Fig. 23(b)). Correlation of TG to ΔV_T, as shown in Fig. 23(c), suggests higher TP for PHKN and ML-IL stacks, which is consistent with extracted HK trap density by using flicker noise as shown in Fig. 23(d).

Fig. 24 shows correlation of ΔV_T during PBTI with TG from SILC measurements for UT-IL, UT-IL+PHKN and ML-IL stacks. Similar to that seen in Fig. 23(c) for TG obtained by using DCIV, higher ΔV_T is seen for a given TG, now obtained using SILC, and suggests higher TP in stacks containing N. It is noted that N causes reduction in SILC, and stacks having higher TP show negative SILC (see Fig. 11). The fundamental physical mechanism responsible for higher HK electron traps due to the presence of N needs further study and is beyond the scope of the present paper.

Fig. 25(a) shows experimental parameters for stacks used in Fig. 23. ΔV_T together with extracted PBTI components ΔV_{IT-HK} ($= q\Delta N_{IT-HK}/CET$) and ΔV_{ET} ($= q\Delta N_{ET}/CET$) for these stacks are shown in Fig. 25(b). The model shown in Table-II has been used for extraction of ΔV_{IT-HK} and ΔV_{ET}. ΔN_{OT-HK} as probed by SILC is presumed to have 2nd order effect and is neglected, as ΔV_T shows n, E_A and Γ that are similar to ΔN_{IT-HK} probed by DCIV and very different from ΔN_{OT-HK} probed by SILC (see Fig.8, Fig.10, Fig.11 and Fig.15). Once again, of particular interest is n and E_A, which reduces (when compared to UT-IL) for UT-IL+PHKN and ML-IL stacks. This is fully consistent with higher ΔV_{ET} (presumably saturates at longer

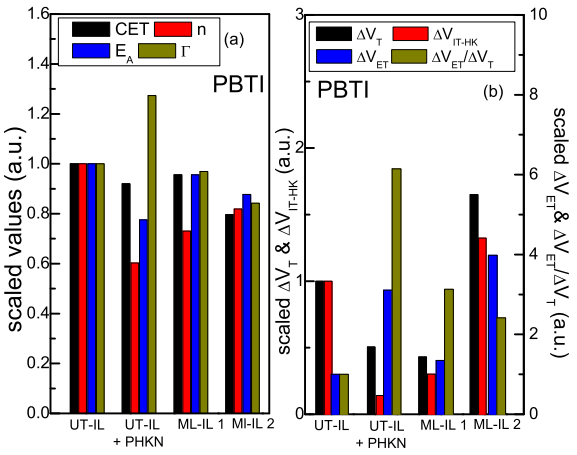

Fig. 25. Impact of PHKN and N based IL scaling on PBTI: (a) CET and measured PBTI parameters n, E_A, Γ; (b) measured ΔV_T and extracted TG (ΔV_{IT-HK}) and TP (ΔV_{ET}) components at E_{OX} = 7MV/cm, T = 130^0C and t-stress = 1000s. Components are extracted using the PBTI model shown in Table-II. IL thicknesses are mentioned in Fig.7.

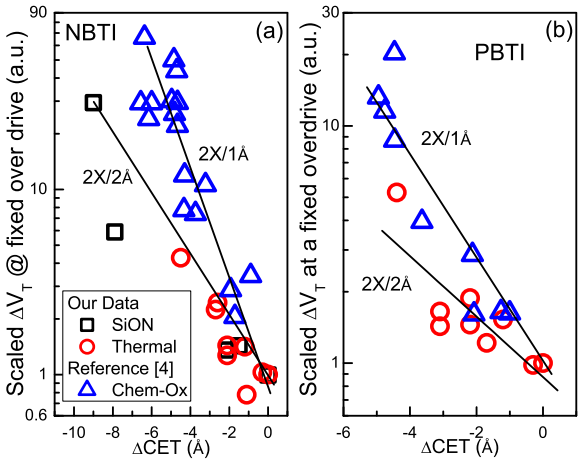

Fig. 26. Impact of IL scaling: ΔV_T (at fixed overdrive bias of 1V) as a function of CET during (a) NBTI and (b)PBTI stress. Thermal IL data are measured in this work. Chem-Ox IL data taken from [4] are shown as reference. For NBTI, SiON data from [23] are shown as an additional reference.

time and has lower E_A) observed in these stacks, and is also consistent with HK trap density from flicker noise shown in Fig. 23(d). Unlike NBTI, no particular trend is observed for N impact on Γ for PBTI stress, as shown in Fig. 25(a).

VI. Impact of IL Scaling on N, P BTI

Fig. 26 shows increase in ΔV_T for (a) NBTI and (b) PBTI at fixed gate overdrive bias as CET of gate stack is reduced by IL scaling. The Chem-Ox reference data obtained from [4] shows 2X increase in ΔV_T with every $1\mathring{A}$ reduction in CET for both N and P BTI. Thermal IL stacks show a much lower rate, with 2X increase in ΔV_T with every $2\mathring{A}$ reduction in CET, once again for both N and P BTI. For NBTI, SiON data are also shown for reference [23], which demonstrate similar trend as thermal IL. Note, a fixed gate overdrive would cause increase in E_{OX} as CET is scaled, which would increase TG and TP components of BTI. Since ΔV_{IT} and ΔV_{HT} for NBTI (ΔV_{IT-HK} and ΔV_{ET} for PBTI) have similar Γ, in the absence of any additional effects, both TG and TP are expected to increase by the same rate due to increase in E_{OX} at scaled CET.

Fig. 27 shows extracted (a) TG (ΔV_{IT}) and (b) TP (ΔV_{HT}) for NBTI and (c) TG (ΔV_{IT-HK}) and (d) TP (ΔV_{ET}) for PBTI as a function of CET obtained by IL scaling. Models shown in Tables I and II have been used for the calculations. For thermal IL, TG and TP were extracted from measured data. For Chem-Ox IL, TG and TP were extracted to maintain 2X increase in ΔV_T for every $1\mathring{A}$ reduction in CET, by keeping measured data as a reference. Although both TG and TP increases with scaling as expected (due to increase in E_{OX}), TP shows relatively larger increase than TG for both N and P BTI, and the increase in TP is much larger for N than P BTI. Relatively larger increase in TP with IL scaling is consistent with lower time exponent n for ML-IL compared to UT-IL stacks, see Figs. 7, 8. Moreover for both N and P BTI, Chem-Ox IL shows larger relative increase in TG and TP compared

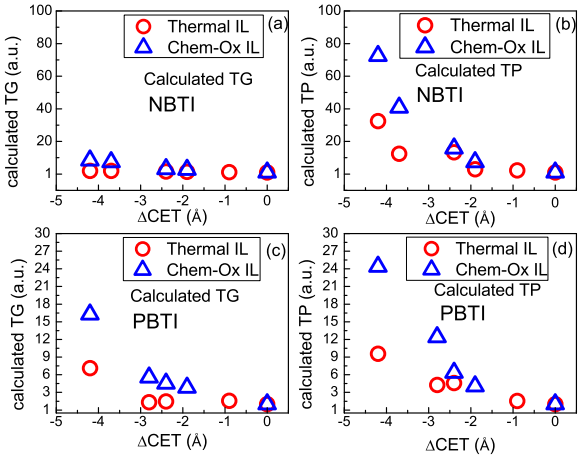

Fig. 27. Impact of IL scaling on underlying BTI components: Calculated values of (a, c) TG and (b, d) TP as a function of CET for UT-IL & Chem-Ox IL stacks. See text for details.

to thermal IL stacks.

Thermal IL scaling is done by using N (either UT-IL+PHKN or N containing ML-IL), hence IL scaled stacks show relatively larger TP during NBTI, as N increases hole traps [22], although some relief is obtained due to lower trapping volume. Chem-Ox IL stacks suffer from higher Hf-O intermixing and higher N penetration from TiN gate. Both these effects result in high IL hole traps, and the situation becomes worse with IL scaling as IL/HK interface comes closer to the Si/IL interface. Therefore, Chem-Ox IL stacks show much larger relative increase in TP during NBTI as IL is scaled.

For PBTI, Chem-Ox IL shows larger increase in TP with IL scaling compared to thermal IL stacks. We speculate this is due to poorer ALD HfOx quality when deposited using ALD on Chem-Ox scavenged stacks. PBTI improvement for thermal IL stacks can also be attributed to presence of N in UT-IL+PHKN and ML-IL stacks. Although N results in somewhat higher HK

electron traps and hence higher TP, more importantly, it causes a significant reduction in TG at the IL/HK interface as probed by DCIV (also in HK bulk as probed by SILC), which helps in lowering the overall ΔV_T. In principle, Chem-Ox IL stacks can also be nitrided to reduce PBTI, but due to its porous nature, N would likely diffuse inside IL and would result in very large increase in NBTI which may not be acceptable.

VII. Conclusion

Scaled HKMG stacks are fabricated using a novel cluster tool system that integrates low T RTP for IL and ALD for HK without vacuum break. For the same EOT, thermal IL stack shows 2X lower NBTI w.r.t Chem-Ox IL stack with no PBTI penalty. EOT scaling down to $6\mathring{A}$ by thermal IL scaling shows a reduced rate of increase in N and P BTI ($2X/2\mathring{A}$) compared to Chem-Ox IL scavenged stacks ($2X/1\mathring{A}$). PBTI improvement is caused by reduction in HfOx trap generation due to presence of N. NBTI improvement is due to superior thermal IL quality with less Hf/O intermixing and lower N penetration that leads to lower IL hole traps. Proposed solution enables EOT scaling by overcoming the BTI limitations observed in Chem-Ox IL based HKMG stacks.

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References

[1] "International Technology Roadmap for Semiconductors(ITRS), 2011." [Online]. Available: http://www.itrs.net/Links/2011ITRS/2011Tables/ORTC_2011Tables.xlsm

[2] W. Tsai, L.A. Ragnarsson, L. Pantisano, P.J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax, S. De Gendt and M. Heyns, "Performance comparison of sub 1 nm sputtered TiN/HfO2 nMOS and pMOSFETs," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, dec. 2003, pp. 13.2.1 – 13.2.4.

[3] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, P. Jamison, M. Wang, E. Cartier, S. Zafar, J. Bruley, A. Kerber, B. Linder, A. Callegari, Q. Yang, S. Brown, J. Stathis, J. Iacoponi, V. Paruchuri and V. Narayanan, "Extremely scaled gate-first high-k/metal gate stack with EOT of 0.55 nm using novel interfacial layer scavenging techniques for 22nm technology node and beyond," in *VLSI Technology, 2009 Symposium on*, June 2009, pp. 138 –139.

[4] E. Cartier, A. Kerber, T. Ando, M.M. Frank, K. Choi, S. Krishnan, B. Linder, K. Zhao, F. Monsieur, J. Stathis and V. Narayanan, "Fundamental aspects of HfO2-based high-k metal gate stack reliability and implications on tinv-scaling," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, Dec. 2011, pp. 18.4.1 –18.4.4.

[5] K. Joshi, S. Hung, S. Mukhopadhyay, T. Sato, M. Bevan, B. Rajamohanan, A. Wei, A. Noori, B. McDougall, C. Ni, C. Lazik, G. Saheli, P. Liu, D. Chu, L. Date, S. Datta, A. Brand, J. Swenberg and S. Mahapatra, "Scaled Gate Stacks for Sub-20-nm CMOS Logic Applications Through Integration of Thermal IL and ALD HfOx," *Electron Device Letters, IEEE*, vol. 34, no. 1, pp. 3 –5, Jan. 2013.

[6] M.J. Bevan, R. Curtis, T. Guarini, W. Liu, S.C.H. Hung and H. Graoui, "Ultrathin SiO2 interface layer growth," in *Advanced Thermal Processing of Semiconductors (RTP), 2010 18th International Conference on*, 28 2010-oct. 1 2010, pp. 154 –156.

[7] C. Oslen, Patent US Patent 017 596 1A1, Sep'04.

[8] S. Deora, P. Narayanasetti, M. Thakkar, and S. Mahapatra, "Development of a Novel Ultrafast Direct Threshold Voltage Technique to Study NBTI Stress and Recovery," *Electron Devices, IEEE Transactions on*, vol. 58, no. 10, pp. 3506 –3513, Oct. 2011.

[9] S. Mahapatra, N. Goel, S. Desai, S. Gupta, B. Jose, S. Mukhopadhyay, K. Joshi, A. Jain, A.E. Islam and M.A. Alam, "A Comparative Study of Different Physics-Based NBTI Models," *Electron Devices, IEEE Transactions on*, vol. PP, no. 99, pp. 1 –16, 2013.

[10] K. Joshi, S. Mukhopadhyay, N. Goel, S. Mahapatra, "A consistent physical framework for N and P BTI in HKMG MOSFETs," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*, April 2012, pp. 5A.3.1 –5A.3.10.

[11] J. Yang, M. Masuduzzaman, K. Joshi, S. Mukhopadhyay, J. Kang, S. Mahapatra, M.A. Alam, "Intrinsic correlation between PBTI and TDDB degradations in nMOS HK/MG dielectrics," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*, April 2012, pp. 5D.4.1 – 5D.4.7.

[12] A. Neugroschel, G. Bersuker, and R. Choi, "Applications of DCIV method to NBTI characterization," *Microelectronics Reliability*, vol. 47, no. 9 -11, pp. 1366 – 1372, 2007.

[13] M. Masuduzzaman, A. Islam, and M. Alam, "A multi-probe correlated bulk defect characterization scheme for ultra-thin high-K; dielectric," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, May 2010, pp. 1069 –1072.

[14] E. Cartier and A. Kerber, "Stress-induced leakage current and defect generation in nFETs with HfO_2/TiN gate stacks during positive-bias temperature stress," in *Reliability Physics Symposium, 2009 IEEE International*, April 2009, pp. 486 –492.

[15] W. Mizubayashi, N. Yasuda, K. Okada, H. Ota, H. Hisamatsu, K. Iwamoto, K. Tominaga, K. Yamamoto, T. Horikawa, T. Nabatame, H. Satake, A. Toriumi, "Carrier separation analysis for clarifying carrier conduction and degradation mechanisms in high-k stack gate dielectrics," *Microelectronics Reliability*, vol. 45, no. 7-8, pp. 1041 – 1050, 2005. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271404005232

[16] K.K. Hung, P.K. Ko, C. Hu and Y.C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 37, no. 3, pp. 654 –665, Mar 1990.

[17] T. Morshed, S.P. Devireddy, M.S. Rahman, Z. Celik-Butler, Tseng Hsing-Huang, A. Zlotnicka, A. Shanware, K. Green, J.J. Chambers, M.R. Visokay, M.A. Quevedo-Lopez and L. Colombo, "A new model for 1/f noise in high-k MOSFETs," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, dec. 2007, pp. 561 –564.

[18] J.Q. Yang, M. Masuduzzman, J.F. Kang and M.A. Alam, "SILC-based reassignment of trapping and trap generation regimes of positive bias temperature instability," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, April 2011, pp. 3A.3.1 –3A.3.6.

[19] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer, "BTI reliability of 45 nm high-K + metal-gate process technology," in *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, May 2008, pp. 352 –357.

[20] T. Naphade, N. Goel, P. R. Nair and S. Mahapatra, "Investigation of Stochastic Implementation of Reaction Diffusion (RD) Model for NBTI Related Interface Traps," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013.

[21] S. Desai, S. Mukhopadhyay, N. Goel, N. Nanaware, B. Jose, K. Joshi and S. Mahapatra, "A Comprehensive AC/DC NBTI Model: Stress, Recovery, Frequency, Duty Cycle and Process Dependence," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013.

[22] G. Kapila, N. Goyal, V.D. Maheta, C. Olsen, K. Ahmed and S. Mahapatra, "A comprehensive study of flicker noise in plasma nitrided SiON p-MOSFETs: process dependence of pre-existing and NBTI stress generated trap distribution profiles," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, Dec. 2008, pp. 1 –4.

[23] V. Maheta, C. Olsen, K. Ahmed, and S. Mahapatra, "The Impact of Nitrogen Engineering in Silicon Oxynitride Gate Dielectric on Negative-Bias Temperature Instability of p-MOSFETs: A Study by Ultrafast On-The-Fly Technique," *Electron Devices, IEEE Transactions on*, vol. 55, no. 7, pp. 1630 –1638, July 2008.