Tunnel FET-based Ultra-Low Power, High-Sensitivity UHF RFID Rectifier

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Abstract

Hetero-junction Tunnel FET (HTFET) for ultra-low power RF circuit design has been explored at the device and circuit level. In this paper, benchmarking and design insights for optimizing the performance of the TFET based differential drive rectifier is presented. Our evaluation of the HTFET based rectifier demonstrates its promise compared to the state-of-art passive RFIDs. With the 10-stage optimized TFET rectifier at 915 MHz, PCE of 98% with 0.5 nW power consumption, sensitivity of -24dBm for 9 µW P_{DC} and sensitivity of -33dBm for 0.4µW P_{DC} were achieved.

Keywords

Tunnel FETs, RF Circuits, Rectifiers, Energy Scavenging

1. Introduction

RF energy scavenging to power wireless sensor networks, RFIDs, implantable biomedical ICs etc, is widely used. In RFID applications, power is transmitted by a "reader" to one or many "tags" [1]. The tags can be completely passive, i.e., with no onboard batteries, or active, with a backup battery. Passive RFID tags limit the communication range (to less than 3 m). In this battery less systems, the RF signal will be converted to DC by the rectifier circuits. The rectifiers in these systems must extract enough DC power from incident radiation to power the circuitry on the tag. Rectification is difficult when the incident power levels are very low. Therefore, most rectifiers have an unresponsive dead zone at low voltage amplitudes [1]. Small turn-on voltage of devices is one of the most important factors in rectifier design. This makes steep slope devices such as tunnel FETS (TFETs) [7] attractive device options for this application. Alternately, several compensation techniques have also been proposed recently to reduce the effective threshold voltage (V_{th}) [2]. However, they still need to deal with several issues such as sensitivity to leakage current. Some of the recent rectifier studies focus on maximizing Power Conversion Efficiency (PCE) and output power, but not much on rectifier sensitivity [3]-[5]. And few such as [6] target more on optimizing rectifier sensitivity with little emphasis on PCE and DC output power levels. PCE of a rectifier circuit is also affected by several parameters such as circuit topology, diode-device parameters, input RF signal frequency, amplitude, and output loading conditions [4]. Therefore, designing a rectifier with high PCE, high sensitivity for long-range communication are important design challenges of any passive RFID rectifier.

There are few rectifier topologies proposed so far which can perform efficiently at microwatts (1-100 µW) of available RF power with higher sensitivity and providing long range RF communication. This work explores the design and analysis, performance benchmarking and optimization of a TFET based UHF RFID rectifier topology to achieve high PCE and high rectifier sensitivity values for increased RF communication range. Our work complements recent efforts in using TFET for low-V_{CC} for digital circuit application [8]-[9] and towards design of energy harvesting and network sensor systems [10]. The remainder of the paper is organized as follows. Section 2 presents the TFET device structure, favourable device characteristics as well as TFET Verilog-A model. Session 3 develops the theoretical justification for TFET rectifier improved performance. Design criterion, performance benchmarking and optimization of TFET based passive RFID rectifier topology is described in Section 4. Finally, conclusions are offered in Section 5.

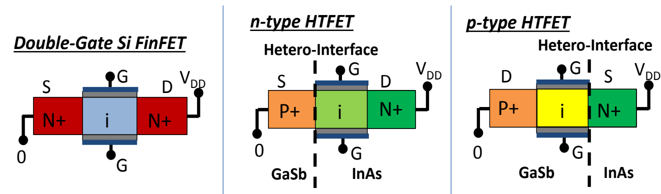

Figure 1: Si FinFET, n-type and p-type HTFET schematics

2. The TFET Device and Simulation Models

2.1 TFET Device Architecture

As shown in Figure 1, TFET is essentially a reverse-biased, gated p-i-n tunnel diode with asymmetrical source/drain doping. The reverse biased diode leakage determines the I_{off} of TFET. The on-state is enabled by the gate-controlled band-to-band tunneling at the source-channel junction, and a sub-60mV/decade steep-slope can be achieved in TFET with desired I_{on}/I_{off} over a low-V_{CC} range. Moreover, with the introduction of the III-V material and heterojunction, III-V HTFET exhibits improved energy efficiency for below 0.5V V_{CC} compared to the state-of-art CMOS technology [8].

2.2 TFET Verilog-A Model for Circuit Simulation

Due to the lack of the mature compact SPICE models for III-V TFET so far, a Verilog-A model has been developed from TCAD Sentaurus [13] device simulation and utilized in the circuit implementations of HTFETs. We have calibrated our GaSb-InAs Heterojunction n-type TFET models with the Atomistic simulation, which is consistent with [14]. Si FinFET based circuits have been employed for baseline comparison, which has been calibrated with experiment data. As shown in Figure 2 for LOP operation, 20nm gate-length HTFET shows 7x on-current improvement at V_{CC} = 0.3V with

an average SS of 30mV/decade over 2 decades of the current change. I_{off} for both devices is 5nA/μm. Since the p-type TFET solution is still in development, symmetrical p-type device performance with the same drive strength is assumed for both Si FinFET and HTFET. The device parameters are shown in Table I. Then the look-up table based Verilog-A models are generated and applied to Spectre [15] for our following circuit evaluation.

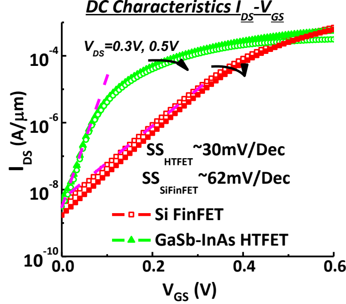

Figure 2: I_{ds}-V_{gs} comparison for Si FinFET and GaSb-InAs HTFET.

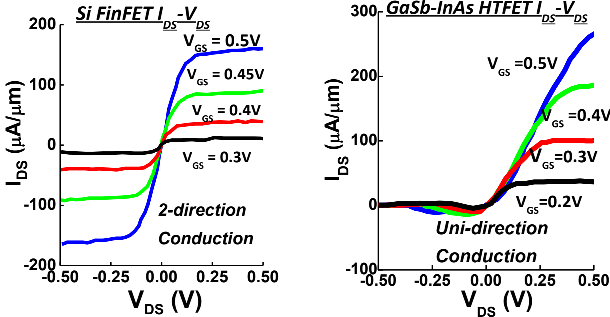

Figure 3: I_{ds}-V_{ds} comparison for Si FinFET and GaSb-InAs HTFET

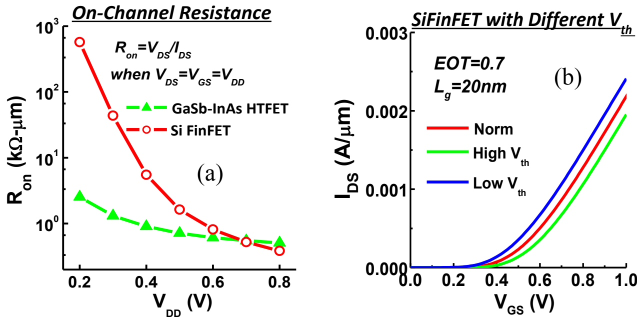

Figure 4: (a) On-channel resistance vs. supply voltage comparing Si FinFET and GaSb-InAs HTFET. (b) Si FinFET models with different V_{th}.

2.3 TFET Device Metrics in Low Power Rectifier Design

Power conversion efficiency (PCE) is the ratio of the average output power at the load to the average real input power to the rectifier. Prior study on power-efficient rectifier design [16] has shown that the transistors' on-resistance (R_{on}) and reverse conduction will induce voltage drop (V_{drop}) as well as the power loss across the rectifier, reducing the output voltage range and the power delivered to the load.

HTFET exhibits uni-directional conduction characteristics (Figure 3) due to the p-i-n device structure, which will be shown later to reduce reverse conduction induced power loss. Figure 4(a) shows that HTFET has lower R_{on} comparing to Si FinFET due to the steep slope switching (high current drive at low V_{cc}), which can improve the PCE for a fixed load.

Another benefit from the steep slope switching is the reduced "turn-on" voltage (since V_{th} definition for TFET varies due to the tunneling mechanism, the term, turn-on voltage is used here), which can lead to the improved output voltage $V_{DC,out}$. The low turn-on voltage and leakage power trade-off of TFET design is compared with multiple Si FinFET models with different V_{th}. As shown in Figure 4(b), high-V_{th} and low-V_{th} represent +0.05V and -0.05V V_{th} shift respectively comparing to the nominal Si FinFET case.

TABLE I: Device Simulation Parameters

Parameter	Value
Channel Length (L_g)	20 nm
EOT (HfO_2)	0.7
HTFET Device Body Thickness (t_{Body})	7 nm
Si FinFET Fin Width (W_{Fin})	10nm
n-type HTFET Source (GaSb) Doping	4×10^{19} cm^{-3}
n-type HTFET Drain (InAs) Doping	2×10^{17} cm^{-3}
Si FinFET Source/Drain Doping	1×10^{20} cm^{-3}
HTFET Material Bandgap (E_g) and Hetero-Interface Band Alignment (ΔE_c): $E_{g,GaSb}$=0.804eV, $E_{g,InAs}$=0.44eV, ΔE_c=0.796eV	

3. TFET Low Power Rectifier Operatoin Principle

3.1 TFET Low Power RF Rectifier Topology

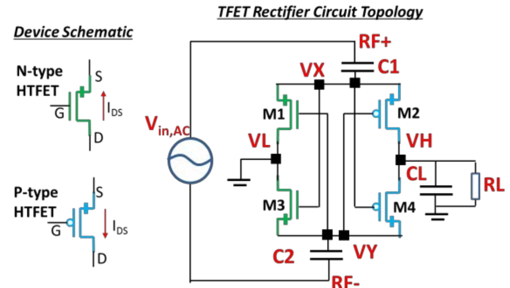

Figure 5: TFET 4-Transistor differential drive RF rectifier topology. TFET connection direction is shown on the left due to uni-directional conduction. (Note: Si FinFET rectifier allows source and drain connection to alter.)

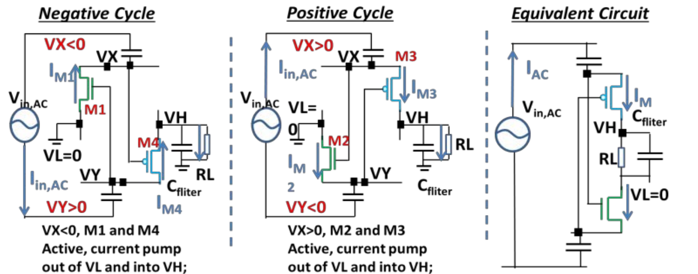

Figure 6: TFET differential drive rectifier operation during half-cycle and equivalent circuit.

Figure 5 shows the design of the TFET based 4-transistor differential drive rectifier topology, which is employed from the CMOS based design in [4] with appropriate consideration to account for the uni-directional conduction of TFETs. A differential input signal $V_{in,AC}$ is applied across nodes RF+ and RF- and a DC output voltage $V_{out,DC}$ = V_H develops across the load impedance. During the positive half of input cycle, when RF+ - RF- increases beyond the device threshold, M2 and M3 will switch on, allowing current to flow into the load while M1 and M4 will remain off (Figure 6). Continuing through the cycle as RF+ - RF- drops below the device threshold, M2 and M3 will turn off until RF+ -

RF- becomes more negative than -V_{th}, at which point M1 and M4 turn on rectifying the negative half of the incoming RF signal. Since V_L is ground in 1-stage rectifier, an effective ground [16] is introduced to get the equivalent circuit.

3.2 Theoretical Analysis of TFET Based Rectifier

The full-wave range utilization is enabled as discussed above, which essentially works as a charge pump to the load. The net charge Q transfer to the load determines $V_{DC,out}$ [4]

$$Q_{VRF_+<0} = Q_{M1,Frd} - Q_{M1,Rev} = Q_{M4,Frd} - Q_{M4,Rev} \quad (1)$$

$$Q_{VRF_+>0} = Q_{M2,Frd} - Q_{M2,Rev} = Q_{M3,Frd} - Q_{M3,Rev} \quad (2)$$

$$Q_{VRF_+<0} + Q_{VRF_+>0} = \frac{V_{DC,out}}{R_L} T \quad (3)$$

where $Q_{VRF_+<0}$ and $Q_{VRF_+>0}$ are the net charge transferred to the load at the negative cycle and positive cycle of $V_{in,AC}$, respectively. $Q_{M1,Frd}$ and $Q_{M1,Rev}$ are the forward ($V_{GS} > 0$) and reverse operations ($V_{GS} < 0$) induced charge transfer due to M1, respectively (similar terms applied to M2, M3 and M4). T is the period of the input RF signal.

To analyze $V_{DC,out}$ and PCE of the TFET rectifier, we take M1's operation during [0, T] (1 signal cycle) as an example comparing with the operation of M1 in Si FinFET rectifier. The terminal voltages ($V_{GS,M1}$ and $V_{DS,M1}$) can be expressed for both Si FinFET and TFET rectifiers as

$$V_{GS,M1} = V_Y - V_X = -V_{in,AC} \quad (4)$$

$$V_{DS,M1} = -V_X = -\frac{1}{2}V_{in,AC} = \frac{1}{2}V_{GS,M1} \quad (5)$$

Note that the device operates at linear region due to (5) at the on-state. Since pFET with the same drive strength is assumed, the matched V_{th} of pFET and nFET eliminates the operation region differences of M1, M4 pair as well as M2, M3 pair. Taking Si FinFET rectifier as baseline, M1 operation in [0, T] can be divided into: subthreshold [0, t_1], linear region [t_1, t_2], subthreshold [t_2, T/2], off-state [T/2, T].

3.2.1 Device Operation in 1 cycle [0,T]

Subthreshold Operation in [0, t_1]and [t_2,T/2]: For -$V_{in,AC}$ < $V_{th,\ SiFinFET}$

$$I_{M1,FinFET} = I_{sub,Vth} \approx I_0 * 10^{\frac{V_{GS,M1}}{n*2.3*V_t}} = I_0 * 10^{\frac{-V_{in,AC}}{SS_{FinFET}}} \quad (6)$$

$$I_{M1,TFET} \approx I_1 * 10^{\frac{-V_{in,AC}}{SS_{TFET}}} \quad (7)$$

where $V_t \approx$ 26mV thermal voltage, n is the body factor, I_0 and are the zero-bias leakage for Si FinFET and TFET respectively, and I_{sub_vth} is the subthreshold current. Since SS_{FinFET}>60mV/decade and the average of SS_{TFET}~ 30mV/decade, $|I_{M1,TFET}|$ > $|I_{M1,SiFinFET}|$ when -$V_{in,AC}$ < $V_{th,SiFinFET}$, Similar analysis can be applied to [t_2, T/2].

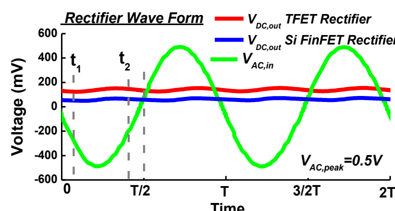

Figure 7: Rectifier input signal $V_{AC,in}$, $V_{DC,out}$ during [0, T] for Si FinFET and TFET. t1, t2 are illustrated at $V_{AC,in}$= $V_{th,Si\ FinFET}$

Linear Operation in [t_1, t_2]: Since $V_{GS,M1} = 2V_{DS,M1}$, when -$V_{in,AC}$ > $V_{th,\ SiFinFET}$, from Session II, we have

$$I_{M1,Si\ FinFET} = I_{Linear} < I_{M1,TFET}\ when\ |V_{in,AC}| < 0.5V \quad (8)$$

$$I_{M1,Si\ FinFET} = I_{Linear} > I_{M1,TFET}\ when\ |V_{in,AC}| > 0.5V \quad (9)$$

I_{Linear} is the device current at the linear region (triode mode).

Reverse Conduction in [T/2,T]: In [T/2, T], $V_X > 0$, ideally M1 is off initially with only leakage power loss caused by I_{off}. As the $V_{DC,out}$ increases untill a state-state ouput formed, a common voltage will be developed for V_X and V_Y, as seen as DC component (Figure 7) . For Si FinFET, $V_{GD,\ M1}$ can be positive, then M1 is turned on when $V_{SD,\ M1}$ > 0 [11]. Since MOSFET is symmetrical, a reverse leakage exists, which is eliminated in TFET.

3.2.2 TFET $V_{DC,out}$ Analysis

To estimate the net charge transfer, we integrate I_{M1} in [0, T/2] first [18]

$$Q_{M1,Frd} = \int_0^{\frac{T}{2}} I_{M1}(t)V_{in}(t)dt$$

$$= \int_0^{t1} I_{Sub,Vth}(t)V_{in}(t)dt + \int_{t1}^{t2} I_{Linear}(t)V_{in}(t)dt + \int_{t2}^{T/2} I_{Sub,Vth}(t)V_{in}(t)dt \quad (10)$$

According to (6)- (7), the steep switching of TFET leads to significant improvement of I_{M1} at low $V_{in,AC}$ compared to subthreshold Si FinFET as well as improvement of both input power utilization and charge transfer in [0, t_1] and [t_2, T/2].

According to (8) and (9), in [t1, t2], M1 is turned on and operating at linear region for Si FinFET. Here TFET shows higher I_{on} compared to Si FinFET at V_{CC} < 0.5V, but losing the energy efficiency at high V_{cc} due to tunneling process limitation. Therefore, at low $V_{in,AC}$, TFET can achieve higher peak I_{M1}, but has lower peak I_{M1} at high $V_{in,AC}$ compared to Si FinFET. Figure 8 shows the comparison I_{M1} of Si FinFET and HTFET for input voltage amplitude of 0.5V and 0.6V, respectively. For both 0.5V and 0.6V operation, HTFET show earlier "turn-on" compared to Si FinFET due to steep-slope with improved utilization of the input signal. At 0.5V input, HTFET shows improved I_{M1}, and reduced peak I_{M1} at 0.6V input. As a result, in the half-cycle input, $Q_{M1,Forward}$ in HTFET will be higher at low $V_{in,AC}$, but will be reduced at high $V_{in,AC}$ due to low I_{on} compared to Si FinFET.

In [T/2, T], M1 is at the off-state, the I_{off} and reverse conduction $I_{Rev}(t)$ induced charge transfer is

$$Q_{M1,Rev} = \int_{T/2}^{T} (I_{Rev}(t) + I_{OFF})V_{in}(t)dt \quad (11)$$

$I_{rev}(t)$ in Si FinFET can be eliminated with the replacement of TFET (uni-directional conduction). With the fixed I_{off} for (Session II), $Q_{M1,Rev}$ is reduced in TFET.

Assuming M1 (M4) and M3 (M2) are identical, using (3),

$$V_{DC,out} = \frac{R_L}{T} * 2 * (Q_{M1,Frd} - Q_{M1,Rev}) = (2V_{RF} - V_{drop}) \quad (12)$$

where V_{RF} is the RMS value of the input signal and V_{drop} is lumped the voltage loss [6]. With the same load and signal frequency, V_{drop} due to the inefficient utilization of the input can be reduced in TFET rectifier, leading to the improved $V_{DC,out}$ at low $V_{in,AC}$ compared to the Si FinFET rectifier.

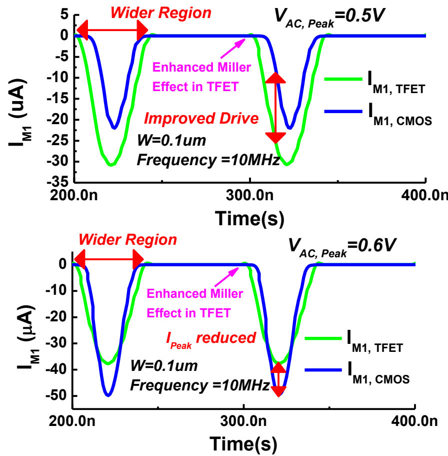

Figure 8: I_{M1} comparison at $V_{AC,peak}$ = 0.5V and 0.6V for TFET based and Si FinFET rectifier

3.2.3 PCE Analysis

According to [11], PCE can be expressed as

$$PCE = \frac{P_{DC,out}}{P_{RF,in}} = \frac{I_{DC,out}V_{DC,out}}{\frac{1}{T}\int_0^T I_{in,AC}(t)V_{in,AC}(t)dt}$$

$$= \frac{\frac{V_{DC,out}^2}{R_L}}{\frac{V_{DC,out}^2}{R_L}+P_{Loss}} \quad (13)$$

$$P_{Loss} = P_{Leakage} + P_{Reverse} + P_{switching} + P_{Ron} \quad (14)$$

$$P_{switching} = 1/T(W_{M1}C_{gg,M1} + W_{M4}C_{gg,M4})\,V_{DC,out}^2 \quad (15)$$

$$P_{Ron} = 2 * (I_{M1}^2 R_{on,M1} + I_{M4}^2 R_{on,M4}) \quad (16)$$

where $P_{DC,out}$, $P_{RF,in}$ and P_{Loss} represent the output DC power, input RF power and the power loss, respectively, $I_{in,AC}$ is the current flowing through the branch. The power loss sources considered in the following analysis are leakage power $P_{Leakage}$, reverse conduction power $P_{Revserse}$, device capacitance switching induced dynamic power $P_{switching}$ and the on-resistance induced thermal power loss P_{Ron}. W_{M1} and W_{M4} represent the device width, $C_{gg,M1}$ and $C_{gg,M4}$ represent the total capacitance of M1 and M4.

Due to the fixed I_{off} for TFET and Si FinFET, $P_{Leakage}$ in [T/2, T] are comparable. However, TFET uni-directional conduction can significantly reduce the reverse conduction induced leakage and power loss $P_{Reverse}$, hence improve the PCE. The improved power ultilization and reduced power loss can improve the $V_{DC,out}$ for TFET rectifier at low $V_{in,AC}$.

TFET also shows an enhanced Miller capacitance effect [17] (higher gate-drain C_{gd} component and suppressed gate-source C_{gs} in total gate capacitance C_{gg}). This effect can cause the transient current "spike" during switching (also shown in Figure 9), which induces an increased $P_{switching}$. In our following evaluation, we will compare PCE with $V_{in,AC}$ to evaluate the rectifier performance.

4. Performance Benchmarking, Design Optimization of TFET Based Passive UHF RFID Rectifier

This Section present the performance benchmarking and design optimization of a TFET based RFID rectifier presented in Section 2.

4.1 TFET Rectifier Performance Comparison with Si FinFET Rectifier

The simulation parameters used for our baseline rectifier design are $C_{1,2} = C_L = 10$pF, $R_L = 10$kΩ, $W_n = 0.1$μm, $W_p = 0.2$ μm, single stage. We analyze the rectifier topology in this study, under the condition that perfect impedance matching is obtained in order to evaluate the intrinsic performance of the rectifier similar to [3]. Figure 9 demonstrates the DC output voltage performance comparison of HTFET rectifier with Si FinFET (Standard-V_{th} (SVT), Low-V_{th} (LVT) and High-V_{th} (HVT)). For the reasons presented in Session II, HTFET rectifier has a larger DC output voltage of ~95x to that of LVT FinFET, 488x to that of SVT FinFET and 1587x to that of HVT FinFET at an RF input voltage of 0.1V (See Figure 9). Irrespective of tuning V_{th} of Si FinFET, the HTFET rectifier has better performance for very weak RF input signals. We observe that HTFET remains the preferred choice till around 0.4V, while Si FinFETs have better performance with increasing RF input levels as tunneling currents are limited.

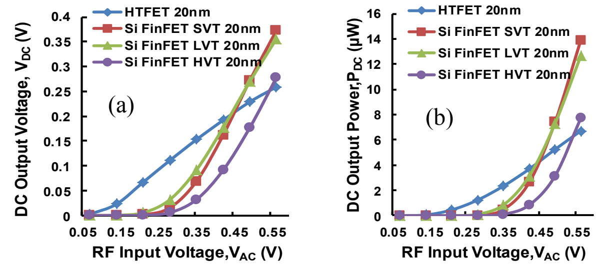

Figure 9: (a) DC output voltage (HTFET vs Si FinFET) and (b) DC output power response of single stage four transistor rectifier topology with varying RF input levels.

Figure 9 also shows the DC output power performance comparison of HTFET rectifier with Si FinFET topology with the 3 different device options. Since the DC output voltage of TFET rectifier is large for a given load, DC output power is higher compared to using Si FINFET for most of the RF amplitude range considered. At approximately, 0.4V RF amplitude, TFET single stage can provide a DC output power of ~3.5μW, whereas LVT FinFET rectifier will provide ~2.2μW, SVT FinFET rectifier will provide ~1.8μW and HVT FinFET rectifier will provide ~0.4μW, respectively.

4.2 Design Optimization for Maximum DC Output Voltage, DC Output Power and Sensitivity

In this section, the performance of the TFET rectifier design for varying circuit parameters is explored to optimize our HTFET rectifier topology.

4.2.1 Dependence on Frequency and Output Loading Conditions

We studied the DC output voltage characteristics of TFET rectifier for different RF input frequencies (For brevity, we only summarize results and do not show the graphs). At 100MHz, TFET rectifier circuit performance is almost similar to that at 10MHz. With the further increase in frequency up to 1GHz, RF rectifier circuit performance slightly degrades due to the increase in $P_{switching}$. Thus, using TFETs one can design UHF RFID rectifiers (for increased communication range) with a slightly reduced performance. Effect of load resistance

on TFET rectifier performance was also evaluated. With an increase in the load resistance (or for reduced load currents), the rectified DC output voltage increases slightly. Since the load current also reduces, the rectified DC output power is almost the same and almost similar PCE values. At an RF input voltage of 0.4V, for R_L=10KΩ, the DC output voltage is ~0.111, at R_L=100KΩ, the DC output voltage is 0.232V and at R_L=1000KΩ, the DC output voltage is 0.264V.

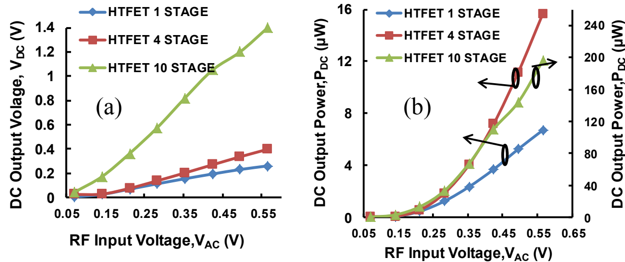

Figure 10: (a) DC Output voltage and (b) DC output power of TFET Rectifier Topology in multi-stage configuration.

4.2.2 Effect of Number of Rectifier Stages and Design Tradeoffs

The multi-stages configuration can achieve large output DC voltage, which serially stacked along the DC path and connected in parallel to the input RF terminals. Figure 10 presents the DC output voltage of TFET rectifier with 1, 4 and 10 stages. Multi-stage topology significantly increases the DC output of TFET rectifier (1.3x output voltage at V_{RF} = 0.35V AC for 4 stage and 5.3x DC output voltage for 10 stage TFET rectifier) and DC output power (1.7x DC output power at V_{RF}=0.35V AC for 4 stage one and 28.6x DC output power for 10 stage TFET rectifier) in comparison to single stage, with a reduction on PCE (from 98% to 93% for 10 stages due to increased losses). Similarly, a significant improvement in the DC output power of 10-stage TFET rectifier is observed in comparison to single and 4-stage TFET rectifier. Similar analysis has been carried out for 15 stages, but the improvement is almost negligible. Thus 10 stages are used in further analysis of the TFET rectifier.

4.2.3 Effect of Transistor Sizing, Coupling Capacitance and Design Tradeoffs

Transistor sizing plays a significant role in the rectifier design optimization. Larger W/L leads to larger device capacitances (larger $P_{switching}$) and smaller R_{on}. By increasing transistor sizing, DC output voltage and power increases, as long as switching losses are small fraction of on-channel conduction losses. However, once the switching losses become comparable to conduction losses, increasing transistor sizing has no improvement on the DC output characteristics. Therefore, we observed that the optimal value for device sizing was 0.75 (detailed results omitted for brevity) for our 10 stage TFET rectifier topology.

Coupling capacitors (C_1 and C_2) strongly affect the rectifier input impedance and thus rectifier output. With the increase of coupling capacitance, the rectifier input impedance reduces, thus more input current flows through the devices (increased conduction losses P_{Ron}), but also increases the DC output voltage and power. $P_{switching}$ also increases with larger coupling capacitors. However, once $P_{switching}$ becomes comparable with P_{Ron}, the DC output characteristics gets worse. Thus an optimal value of $C_{1,2}$=10fF is then obtained in the further analysis of 10 stage TFET rectifier topology.

4.2.4 Performance of Optmized TFET Rectifier

Design optimization has been performed for a 10 stage TFET rectifier at 915MHz with W_p/W_n=1,W_p=W_n=0.75µm, $C_{1,2}$=C_L=10fF, R_L=10KΩ based on design exploration shown above. Figure 11 present the variation of PCE and DC output power of a 10-stage TFET rectifier for varying RF input power levels. For RF input power levels of -72dBm to-36dBm, the DC output power level varies from 73pW to 0.2µW with significant improvement in PCE. From -36 dBm to -13 dBm input levels, there has been a significant increase in output power (from 0.2 µW to 50 µW). This shows one can achieve good communication range of ~10-100m with increased sensitivity values using multi-stage TFET rectifier.

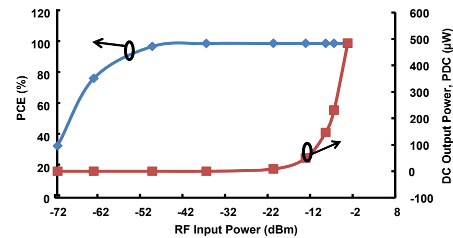

Figure 11: PCE and DC output power variation of a 10 stage TFET Rectifier topology under optimal conditions.

Using the 10-stage rectifier for $V_{in,AC}$ =0.1V, the optimized TFET rectifier has 8.4x larger DC output voltage than the baseline TFET rectifier (Table II). For the same conditions, the optimized TFET rectifier has 69.5x larger DC output power than un-optimized one. Also, the power consumption of the un-optimized one is ~13.4nW and that of the optimized one is ~0.46nW. For the rectifier that can produce a DC output voltage of 0.3V, driving a load of 10KΩ (load current 30µA), minimum DC output power should be 9 µW. The optimized rectifier is able to achieve this with a sensitivity of -24dBm and the non-optimized one has a sensitivity of -20dBm. This means the optimized TFET rectifier can have the similar performance at ~30m RF communication range in comparison to the un-optimized one operating at ~20m communication range. The communication range using TFET rectifier for passive RFIDs can be further increased using more number of rectifier stages and following the optimization procedure. Table III summarizes the performance and benchmarking of optimized TFET rectifier with the published data. Friis equation [1], [3] is used to estimate communication range. With the 10-stage optimized TFET rectifier, 98% of PCE with 0.5nw of power consumption, sensitivity of -24dBm for 9 µW P_{DC} (free-space communication range of ~30m) and sensitivity of -33dBm for 0.4µW P_{DC} (free-space communication range of ~90m) and was achieved.

TABLE II: TFET RECTIFIER DESIGN OPTIMIZATION

Case	V_{DC} (V) (V_{in}=0.1V)	P_{DC} (µW)	PCE (%)	0.3V_{DC} Sensitivity (dBm)	RF Range (m)

Non-Optimized	0.042	0.18	93	-20	20
Optimized	0.354	12.5	98	-24	30

5. Conclusion

In this work, performance benchmarking and design insights for TFET based differential drive rectifier have been presented for the first time. Irrespective of tuning V_{th} of Si FinFET, the HTFET rectifier performance is superior for rectifying weak RF input signals. HTFET Rectifier has been shown to have 25-50% larger DC rectified output power in comparison to Si FinFET topology due to the steep switching, improved I_{on} at low V_{CC} and uni-directional conduction. A design parameter optimization specific to TFET rectifier was also explored. The optimized TFET rectifier has 8.4x larger DC output voltage, 69.5x larger DC output power with larger PCE values in comparison to non-optimized case. With the 10-stage optimized TFET rectifier at 915 MHz, PCE of 98% with 0.5 nW power consumption, sensitivity of -24dBm for 9 µW P_{DC} (with free-space communication range of ~30m) and sensitivity of -33dBm for 0.4µw P_{DC} (with free-space communication range of ~90m) is achieved.

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TABLE III: HTFET RECTIFIER BENCHMARKING

	K. Kotani [4]	M. Ghovanloo [12]	P.Asbeck [11]	R. Sarpeshkar [1]	D. Wentzloff [6]	This work
Technology	0.18 µm CMOS	0.5 µm CMOS	0.25 µm CMOS	0.18 µm CMOS	0.13 µm CMOS	20nm HTFETs
Device V_{th} (V)	0.437 /- 0.450	0.75/-0.9	0.4/-0.4	0.1/-0.29	LVT,ZVT,ZVTDG	~0.110
Year	2009	2013	2010	2007	2012	2013
Rectifier Topology	4-T Differential drive	Active voltage doubler	4-T Modified differential-drive	4-T Modified differential-drive	2-T Dickson multiplier	4-T Differential drive
RF input power (µw)	114	7300	~91	10-200	0.1-2.5	73pW-500 µW
V_{RF} (V)	---	1.46	0-1.8V	--	---	0.010-0.5V
DC output voltage (V)	0.8	2.4	(0-2.6V) 1.4 V	0.5	0.2-2.6	0.5mV-2.2V
DC output power (µw)	64	5800	~65	5	~100	25pW-484 µW
RF Frequency (MHz)	953	13.56	915	900	915	915
RL (kΩ)	10	1	30	1000	1000	10
C_{in} and C_L	1.13 pF / 1.13 pF	1µF/1µF	Nil/0.5pF	--/1.19pF	1pF/1pF	10fF/10fF
Power consumption(µw)	1 stage (38 µW)	800	~25	---	---	0.5nW
Number of stages	1, 3	---	---	2	30,50,70	10
Peak PCE (%)	67.5	79	71.5	---	---	98
Sensitivity (dBm)	-12.5	~ +8.6	-4	-24.7	-32 with 50 stages	-24 for 9 µW P_{DC} -33 for 0.4 µW P_{DC}
RF range (m) (For 4W EIRP)	8.7	~0.0007	~3	26	66 with 50 stages	30 for 9 µW P_{DC} 90 for 0.4 µW P_{DC}
Charging Time (s)	---	---	---	---	155ms for 50 stages	0.4-0.6µs for 1 stage and few µs for 10 stages