Steep Switching Tunnel FET: A Promise to Extend the Energy Efficient Roadmap for Post-CMOS Digital and Analog/RF Applications

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Abstract

Steep switching Tunnel FETs (TFET) can extend the supply voltage scaling with improved energy efficiency for both digital and analog/RF application. In this paper, recent approaches on III-V Tunnel FET device design, prototype device demonstration, modeling techniques and performance evaluations for digital and analog/RF application are discussed and compared to CMOS technology. The impact of steep switching, uni-directional conduction and negative differential resistance characteristics are explored from circuit design perspective. Circuit-level implementation such as III-V TFET based Adder and SRAM design shows significant improvement on energy efficiency and power reduction below 0.3V for digital application. The analog/RF metric evaluation is presented including g_m/I_{ds} metric, temperature sensitivity, parasitic impact and noise performance. TFETs exhibit promising performance for high frequency, high sensitivity and ultra-low power RF rectifier application.

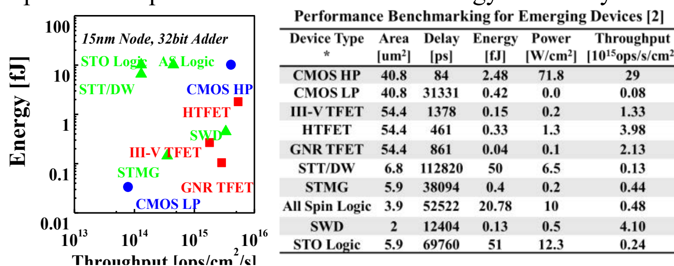
Keywords

Steep switching, Tunnel FETs, TFET SRAMs, energy efficiency, supply voltage scaling, ultra-low power digital, low power analog/RF

1. Introduction

With continued transistor scaling, the static power has become a dominant component in total power consumption due to the threshold voltage (V_{th}) scaling and off-state leakage (I_{off}) trade-off. While V_{th} reduction is critical to lower supply voltage, I_{off} increases exponentially as the threshold voltage is reduced. The ability to control this increase is fundamentally limited by the 60mV/dec sub-threshold slope (SS) in CMOS technology. Thus, the supply voltage (V_{CC}) scaling has slowed due to the leakage power budget and required minimum on-state drive current (I_{on}), which has fundamentally restrained the power consumption reduction for high-performance, low-power digital application. The reduction of device intrinsic gain (g_m/g_{ds}) with technology scaling as well as the effective gain (g_m/I_{ds}) limit and design trade-offs in CMOS technology impose further challenges for ultra-low power analog/RF application.

Various innovations in devices have been investigated to improve the energy efficiency per computation for post-CMOS circuit and architecture application. Steep switching Tunnel FETs (TFETs), an alternative device architecture, can enable further scaling of V_{CC} for ultra-low power applications [1]. Benchmarking on beyond CMOS logic devices including electronic and spintronic devices have shown that TFET can achieve > 10^{15} Integer Ops/s/cm^2 with power < 1W/cm^2 (Figure 1) [2]. Recent approaches in TFET based digital and analog/RF designs have shown significant performance improvement and power reduction [3-6]. Due to the device characteristics of TFETs (e.g. asymmetrical source/drain, vertical device architecture, steep switching, uni-direction conducting, etc), co-design from device metrics to circuit implementation needs to be applied to TFET technology to optimize the performance benefits and energy efficiency.



Performance Benchmarking for Emerging Devices [2]

Device Type *	Area [um²]	Delay [ps]	Energy [fJ]	Power [W/cm²]	Throughput [10^{15}ops/s/cm²]
CMOS HP	40.8	84	2.48	71.8	29
CMOS LP	40.8	31331	0.42	0.0	0.08
III-V TFET	54.4	1378	0.15	0.2	1.33
HTFET	54.4	461	0.33	1.3	3.98
GNR TFET	54.4	861	0.04	0.1	2.13
STT/DW	6.8	112820	50	6.5	0.13
STMG	5.9	38094	0.4	0.2	0.44
All Spin Logic	3.9	52522	20.78	10	0.48
SWD	2	12404	0.13	0.5	4.10
STO Logic	5.9	69760	51	12.3	0.24

*Si MOSFET high performance (CMOS HP) and low power (CMOS LP), III-V and Heterojunciton TFET (HTFET), Graphene Nanoribbon (GNR) TFET, Spin Torque based Domain Wall (STT/DW), Majority Gate (STMG) and Oscillator (STO) Logic, Spin Wave Device (SWD).

Figure 1 Energy vs throughput and area, delay, power comparison for emerging electronic and spintronic/magnetic devices [2].

In this paper, the device metrics for digital and analog/RF application and circuit implementation have been discussed from III-V TFET from device-circuit interaction perspective. This paper is divided into five sections. In Section 2, the device operation and performance benchmarking of steep switching TFET are discussed. Section 3 shows modeling and design considerations for implementing TFETs as energy efficient digital circuits. Section 4 shows the TFET metrics for ultra-low power analog/RF applications. The challenges of III-V p-type TFET and layout considerations are discussed in Section 5, followed by conclusions.

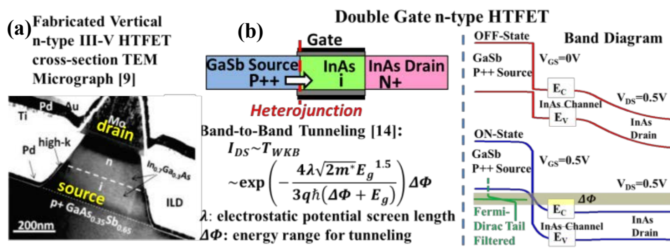
2. Steep Switching Interband Tunnel FET

Tunnel FET is essentially a reverse-biased, gated p-i-n tunnel diode with asymmetrical source/drain doping (Figure 2(a-b)). In MOSFETs, the carrier injection is controlled by the thermal electrostatic potential barrier, where only carriers with energy exceeding the barrier can contribute to the on-state current (I_{on}). These high energy carriers following Fermi-Dirac distribution injected through thermionic emission at the source/channel p-n junction have an energy slope of kT, which induces SS > 60mV/dec (~2.3kT/q) in MOSFET at the room temperature (300K). In TFETs, the on-off switching is enabled by the gate-voltage induced band-to-band tunneling (BTBT) at the source-channel junction, which opens the tunneling window in the energy bands. Since the high energy tail of Fermi-Dirac distribution is filtered by the tunneling window, a sub-60mV/dec SS can be achieved in TFET.

The design of TFET involves the considerations of material systems, tunnel junction, gate electrostatics, supply voltages, geometries and factors that degrade SS. Figure 2(b) shows the tunneling current dependence, which illustrates the

paths to improve TFET performance [14]. Low-bandgap (E_g) materials (e.g. Ge, III-Vs, etc) with low effective mass (m*) as well as hetero- band-alignment can significantly improve the tunneling probability (T_{WKB}) at low V_{CC}. Tunnel junctions with steep profiles and low defects as well as improved gate-control from planar towards the gate-all-around structures (e.g. nanowires) can further improve the electrostatics (reduce λ) for steep SS and high I_{on}. In [7-9], III-V heterojunction nTFETs (HTFET) have been demonstrated with MOSFET-like I_{on} achieved due to the significant tunneling transmission probability improvement. The most recent work on fabricated n-type III-V TFETs and device performance is summarized in Figure 2(c). The main obstacle of non-steep SS in fabricated TFET is due to the trap assisted tunneling (TAT) of the source/channel interface states [1, 7], which can be sovled with further improvement on material interface.

In order to realize the complementary TFET logic, p-type TFET demonstration is crucial. Si, SiGe, Ge-based pTFET have been investigated [13, 15, 16]. The demonstrated GeSn p-TFET in [15] shows I_{on} of 4.34 μA/μm at 1V. [16] reported the first fabricated strained-Si nanowire TFET inverter with I_{on}>10 μA/μm at 0.5V for n- and p-TFETs, a minimum SS of 30mV/dec for nTFET and high static gain at 0.2V achieved. The simulated n- and p- TFET characteristics with various material systems are compared in Figure 2(d) [3, 13].



(c) Performance Comparison for Fabricated III-V TFET [7]

Reference	Source-Channel Material	EOT [nm]	I_{ON} [uA/um]	V_{DS} [V]	V_{ON}-V_{OFF} [V]	I_{ON}/I_{OFF}	S_{MIN} [mV/dec]	S_{EFF} [mV/dec]
Zhou [7]	GaSb-InAs	1.3	180	0.5	1.5	6000	200	400
Zhou [8]	InP-InGaAs	1.3	20	0.5	1.75	450000	93	310
Mohata [9]	GaAsSb-InGaAs	1.75	135	0.5	1.5	17000	230	350
Zhao [10]	$In_{0.7}Ga_{0.3}As$	1.2	40	0.5	2	200000	84	380
Li [11]	AlGaSb-InAs	1.6	78	0.5	1.5	1600	125	470
Dewey [12]	$In_{0.53}Ga_{0.47}As$	1.1	5	0.3	0.9	70000	58	190

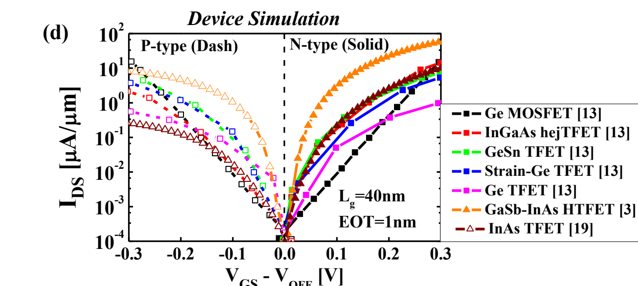


Figure 2 (a) Fabricated III-V HTFET TEM micrograph [9] (b) Double-gate HTFET device schematic, band diagram at on/off state, tunneling current dependence (c) Summary of the reported III-V TFET performance comparison [7]. (d) Simulated double-gate n- and p- TFET with various material systems [3, 13, 19]. GaSb-InAs HTFET shows improved I_{on} for 0.3V.

3. Tunnel FET for Energy Efficient Digital Application

3.1 Tunnel FET Modeling for Circuit Simulation

Compact model for Si TFET has been reported in [17], showing good agreement with TCAD simulation. However, due to the material system difference, compact models for III-V TFETs have yet to be developed. In order to perform the III-V TFET based circuit design, we have developed look-up table based Verilog-A models [3, 19] from TCAD Sentaurus simulation [18], which can capture both DC and transient characteristics of III-V TFETs. The TCAD simulation models of III-V TFET have been calibrated with fabricated III-V TFET data and applied to the projected technology nodes to compare with the state-of-art CMOS technology. At the gate length (L_g) of 20nm, our calibrated GaSb-InAs HTFET model shows seven times improvement of I_{on} at 0.3V V_{CC} over L_g=20nm Si FinFETs for LOP application with off-state leakage of 5nA/ μm (Figure 3), which is also comparable with the Atomistic NEGF simulation projection in [20] at L_g=16nm. An average SS of 30mV/dec over 2 decades of current change can be achieved in the modeled GaSb-InAs TFET.

TFET Verilog-A models are based on two dimensional look-up tables with $I_{ds}(V_{gs}, V_{ds})$, $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ obtained from fine-granularity simulation across a range of V_{ds} and V_{gs}. A Si FinFET based Verilog-A model has also been developed with experiment data calibration as a baseline corresponding to the LOP device target (Figure 3) for the following performance comparison. Verilog-A modeling technique provides an accurate way for emerging device based circuit design and performance analysis, which is suitable for small transistor count digital and analog/RF circuit simulation.

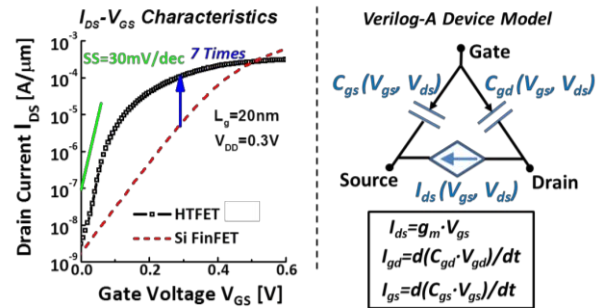


Figure 3. I_{ds}-V_{gs} HTFET characteristics comparing with Si FinFET at L_g=20nm and Verilog-A modeling [3, 19].

3.1. TFET Characteristics and Impact on Circuit Design

Unidirectional Conduction: Due to the asymmetrical p-i-n structure, TFET exhibits uni-directional conduction characteristics (before forward biasing p-i-n the diode), opposed to the symmetrical source/drain in MOSFETs (Figure 4 (a-b)). In TFET based circuit design, the device source/drain orientation needs to be addressed while additional transistors are required to solve the internal circuit nodes charging/discharging issues (e.g. pass transistor logic) [3]. In certain circuit designs (e.g. TFET RF rectifier), however, this uni-directional conduction can simultaneously reduce the reverse conduction leakage as well as the power loss [5].

Gated Negative Differential Resistance (NDR): In TFET normal operation, the built-in p-i-n tunnel diode is reverse-biased (V_{ds} > 0V for nTFET). As forward biasing the p-i-n diode (V_{ds} < 0V for nTFET) at the device on-state (V_{gs} > 0V for nTFET), TFET exhibits negative differential resistance (gated NDR) characteristics. Compared to the NDR effect in resonant tunnel diodes (RTD), the current level of TFET and stand-by power consumption is significantly lower for power reduction. Figure 4 (c) shows the NDR in fabricated InGaAs TFET [21], with a peak-valley ratio (PVCR) of 2 within 0.2V

window, which can be further improved by material system and dielectric interface engineering. The NDR characteristics in TFET can provide both positive and negative transconductance, which is promising for the NDR based cellular neural networks (CNN) cell realization [22].

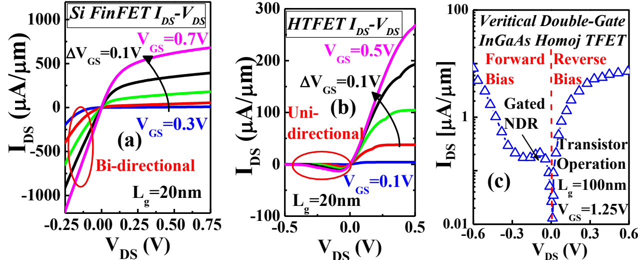


Figure 4 Output characteristics (I_{ds}-V_{ds}) for (a) Si FinFET and (b) HTFET. HTFET shows unidirectional conduction. (c) Measured gated NDR in homojunction InGaAs TFET in forward biasing operation [21].

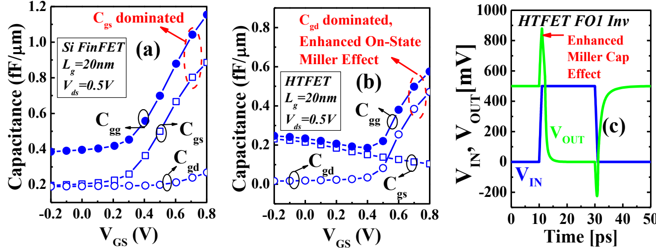


Figure 5 Capacitance characteristics for (a) Si FinFET and (b) HTFET and (c) HTFET FO1 Inverter switching performance [3].

Enhanced On-State Miller Capacitance Effect: TFETs exhibit different capacitance performance compared to MOSFETs, known as enhanced on-state Miller capacitance effect [23]. In MOSFETs, the gate-source capacitance C_{gs} dominates the total gate capacitance C_{gg} at on-state. In TFETs, due to the unequal charge sharing between source and drain, the gate-drain capacitance C_{gd} dominates the total capacitance C_{gg} at on-state (Figure 5). The large portion of C_{gd} in C_{gg} induces a voltage "spike" during switching as an enhanced Miller capacitance due to the strong coupling between the gate and drain, which has recently been validated by the fabricated Si TFET inverter characterization [16]. This effect increases the circuit stabilizing time during switching and results in increased delay and dynamic power consumption in certain circuit design [4] with increased number of switching nodes. In SRAM design, however, this effect can improve the storage nodes coupling and assist the node recovery due to radiation, improving the SRAM soft error resilience [24].

Soft Error Performance: Soft error is the key challenge in low power CMOS circuits with V_{CC} scaling induced circuit node charge reduction. Given the material ionization energy is proportional to bandgap, low bandgap materials as channel replacement for performance improvement may cause further increase of soft error rate (SER). In fully depleted channel devices (e.g. FDSOI, FinFETs), the transient current duration due to radiation is dominated by the bipolar gain effect rising from the deposited hole storage in the channel. In TFETs, because of the built-in p-i-n junction, the generated electrons and holes due to radiation can be effectively collected by the drain and source nodes, respectively, leading to significant reduction in the transient current duration and total charge collection (Figure 6(a)). Significant SER reduction (5 times reduction at 0.3V) can be achieved in HTFET based SRAM due to the charge collection reduction and enhanced node capacitance coupling (enhanced on-state Miller effect) comparing to Si FinFET based SRAM (Figure 6(b)). In HTFET logic, high I_{on} at low V_{CC} can further improve the latching window masking effect and reduce the error latching portability due to both the reduced latching window duration (at the same clock frequency) and reduced transient current duration (Figure 6(c)). Thus, HTFET based circuits can achieve superior radiation resilience at low V_{CC} in comparison of the Si FinFET based circuits, which is highly desired for radiation resilient ultra-low power application [24].

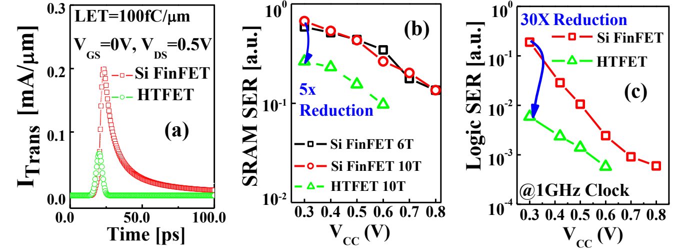


Figure 6 (a) Transient current profile due to radiation (b) SRAM SER and (c) logic SER vs V_{CC} comparing Si FinFETs and HTFETs based circuits [24].

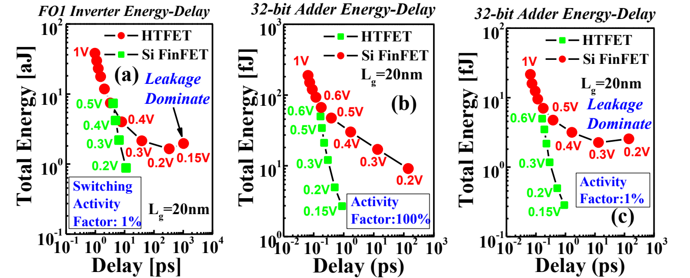


Figure 7 (a) FO1 inverter and 32-bit Hans-Carlson Adder energy-delay evaluation for L_g=20nm HTFET and Si FiFET at activity factor of (b) 100% and (c) 1% respectively[19].

3.4 Tunnel FET Logic Performance Benchmarking

Figure 7 shows the energy-delay comparison of FO1 (fanout of 1) inverter and the 32-bit prefix-tree Hans-Carlson Adder using HTFETs and Si FinFETs [19]. A cross-over at V_{CC}=0.5V in the energy-delay characteristics is observed for HTFET based FO1 inverter and 32-bit Adder for both high (100%) and low activity (1%) levels, which outperforms the Si FinFET-based circuits with a favorable energy-delay tradeoff. As the leakage energy starts to dominate the total energy consumption at low-activity level (1%), Si FinFET-based 32-bit Adder reaches the energy minima at V_{CC}=0.3V and shows increased energy consumption when continuously reducing V_{CC}. The HTFET-based 32-bit Adder, in contrast, shows continued energy reduction with V_{CC} scaling down to 0.15V and desired delay performance due to its steep switching slope.

3.5 Tunnel FET SRAM Design

TFET as an energy efficient device alternative for below 0.3V V_{CC} operation can enable further power reduction in CMOS SRAM in addition to the current power saving approaches. Due to the unidirectional conduction characteristics of TFETs described in Session 2, the traditional 6T CMOS SRAM cell needs to be modified for TFET SRAM to achieve read/write operation and desired noise margin with a higher transistor count. Figure 8 shows TFET based 8T and 10T SRAM cell designs including 8T TFET Transmission-Gate (TG) SRAM cell, 8T/10T dual-port (DP) SRAM cell,

TFET Schmitt-Trigger (ST) SRAM cells. Device sizing has to be adjusted for iso-area regarding to 6T CMOS SRAM cell and noise margin optimization. Significant delay reduction below 0.4V V_{CC} and dynamic power consumption reduction below 0.3V V_{CC} can be achieved in HTFET SRAM arrays (256x256) due to the I_{on} enhancement and steep switching at low V_{CC} compared to subthreshold Si FinFET operation (low I_{on} and off-leakage dominates in dynamic power) [3].

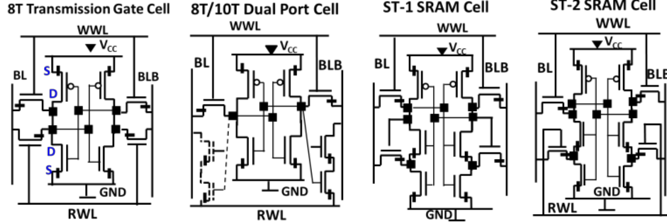


Figure 8. SRAM design examples using HTFETs: 8T Transmission Gate (TG) cell, 8T/10T dual port (DP) cell, ST-1 and ST-2 with Schmitt-feedback. TFET orientation is illustrated in each design [3].

4. Tunnel FET Analog/RF Application Metrics

While the digital application drives the transistor scaling as projected by Moore's law, analog/RF design typically employ the older technologies due to the tradeoffs in matching, linearity, gain, noise, bandwidth and frequency for different applications. With growing markets for portable, battery-less energy harvesting systems, ultra-low power analog/RF circuits using sub-threshould (sub-V_{th}) CMOS have been investigated for optimal energy efficiency. Due to the performance variation increase at low current, sub-V_{th} CMOS design is still limited by the tradeoffs among signal-to-noise ratio (SNR), speed, precision and robustness within certain area constraint. In this section, we will focus on TFET analog/RF metrics to further improve the performance and energy efficiency for ultra-low power analog/RF application.

4.1 High Effective Gain g_m/I_{DS} due to Steep Switching

g_m/I_{ds} metric as the effective gain per energy step is the key factor for low power analog circuit design. In MOSFETs, the peak g_m/I_{ds} is achieved at the device sub-V_{th} region:

$$g_m = \frac{I_{D0}}{nV_t}\exp\left(\frac{V_{GS}-V_T}{nV_t}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_t}\right)\right)$$

$$\frac{g_m}{I_{DS}} \sim \frac{1}{nV_t} < \frac{1}{26mV} = 40V^{-1}$$

Since MOSFET sub-V_{th} current follows kT/q slope, g_m/I_{DS} has an upper limit of 40 V^{-1} at 300K. In steep switching devices, g_m/I_{DS} can overcome the 40 V^{-1} limit:

$$\frac{g_m}{I_{DS}} = \frac{\partial I_{DS}}{\partial V_{GS}}\frac{1}{I_{DS}} = \frac{\partial ln I_{DS}}{\partial V_{GS}} = \frac{ln10\,\partial\log I_{DS}}{\partial V_{GS}} = \frac{ln10}{\mathrm{SS}}$$

Figure 9(a) shows the g_m/I_{DS} vs. I_{DS} comparison for HTFETs, III-V and Si FinFETs, where HTFETs show improved g_m/I_{DS} at low I_{DS}. This allows the exploration on more energy efficiency for low-power analog application using HTFETs. For example, in Analog-to-Digital Converter (ADC) design, the power dissipation per sampling frequency is bounded by the SNR, g_m/I_{DS} and V_{CC}. Designing ADC at low V_{CC} is increasingly difficult due to the SNR requirement, which also limits the system energy efficiency [25]:

$$\frac{Power}{Sampling\ frequency} \sim \frac{kT\cdot SNR}{V_{CC}}\left(\frac{g_m}{I_{DS}}\right)^{-1}$$

Given high g_m/I_{DS} in TFET, V_{CC} scaling can be realized while maintaining the SNR ratio, leading to further reduction of energy per conversion step in low-power ADC design.

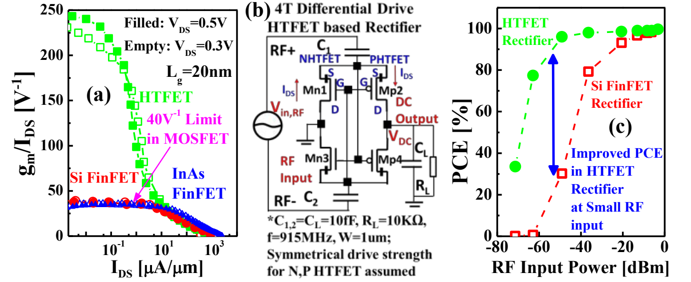


Figure 9 (a) g_m/I_{DS} vs I_{DS} comparing HTFET, Si and III-V FinFET at 0.3V and 0.5V $V_{DS.}$ (b) HTFET based RF rectifier schematic (orientation illustrated) and (c) power conversion efficiency comparison vs RF input Power for 10-stage HTFET and Si FinFET based rectifier [5].

4.2 High Sensitivity and Efficiency due to Steep Switching

In RF rectifier and wake-up receiver design, a transistor with low V_{th} is preferred to improve the circuit sensitivity to small amplitude RF input signal. Due to the leakage power constrain, the tradeoff between I_{off} and V_{th} is essential in high sensitivity, ultra-low power RF rectifier and receiver design using CMOS technology. With the steep switching, TFET exhibits a reduced effective turn-on voltage at the same leakage compared to CMOS, which can be applied to the analog/RF circuits to improve the sensitivity. Also, the unidirectional conduction characteristics can prevent the reverse leakage paths rising from the sinusoidal input to further improve the efficiency. Figure 9(b) shows the recently demonstrated 4T differential drive TFET RF rectifier design for ultra-low power RFID application [5]. Comparing with the Si FinFET based RF rectifier, the power conversion efficiency (PCE) of 95% can be achieved at -50 dBm RF input power in the optimized 10-stage TFET rectifier, while PCE of Si FinFET based design drops to 30%. This sensitivity boosting comes from the improved utilization of input signal, reserve leakage induced power loss reduction as well as the reduced on-state resistance due to the improved I_{on} at low V_{CC}.

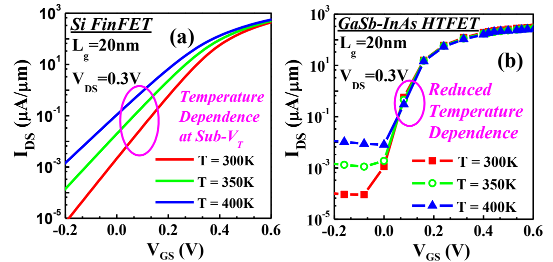


Figure 10 Temperature dependent I_{ds}-V_{gs} for (a) Si FinFET and (b) HTFET.

4.3 Temperature Sensitivity

Temperature drift is another design concern in CMOS circuits. Due to the thermal limited SS, MOSFET exhibits temperature dependent switching performance with V_T shift and leakage increase. In TFET, I_{off} (p-i-n diode reverse leakage) is dominated by Shockley-Read-Hall generation-recombination with temperature dependence. The BTBT induced steep switching of TFET, however, exhibits reduced temperature sensitivity, which is mainly due to the weak temperature dependent E_g. Figure 10 shows the simulated temperature dependent I_{DS}-V_{GS} comparing Si FinFET and

HTFET at varied temperatures, where reduced temperature dependence has been observed in HTFET. Experimental characterization on III-V TFET in [26] has confirmed the temperature independence of gated tunneling, however, the reduction of TAT is still required to improve the temperature insensitivity. Thus, TFET can be a suitable candidate to mitigate the temperature induced performance variations.

4.3 Variation and Mismatch

Process variation induced device characteristic fluctuation has become increasingly important with scaling. Due to the exponential dependence of I_{on} on the tunneling-barrier, variation sources that can alter the tunneling-barrier width will cause significant I_{on} fluctuation in TFET. The variation sources for a double-gate ultra-thin-body (UTB) HTFET have been investigated in [3] considering fluctuations in source doping, oxide thickness (T_{ox}), gate-contact work function (WF), gate-source/gate-drain overlap, body thickness (T_b). Figure 11(a-b) shows the percentage of each variation source contribution in HTFET and Si FinFET using Monte-Carlo simulation. Gate-source overlap fluctuation is dominated above 0.5V due to the depletion induced tunnel-barrier width change. T_b variation is another major source for both HTFET and Si FinFET due to the quantum confinement effect induced E_g variation. The percentage of I_{on} change shows HTFET is more prone to variations (Figure 11(c)). The variation impact on HTFET and sub-V_{th} CMOS is comparable below 0.3V. Thus, the variation induced mismatch can strongly impact both HTFET and CMOS based circuit-designs at low V_{CC}.

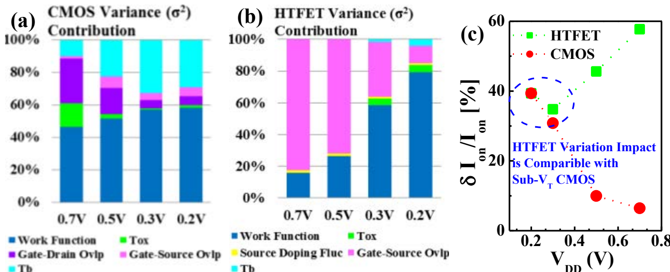


Figure 11 Variance contributions at different V_{cc} from various variation sources for (a) CMOS and (b) HTFET. (c) On-current fluctuation comparing HTFET and CMOS with supply voltage scaling [3].

4.4 Parasitic Analysis of Vertical TFET

Transistor cut-off frequency f_T is strongly impacted by the device parasitic capacitances and series resistances. While the continuous L_g scaling at each technology node keeps boosting f_T in CMOS technology, the growing impact from the un-scaled parasitics may prevent the projected f_T improvement in future technology nodes. The vertical device architecture of TFET with vertically oriented channel allows the independent scaling of contacted gate-pitch and channel-length to prevent the short channel effect in highly scaled technology nodes. But more parasitic elements need to be considered. Figure 12(a) shows parasitic components in a vertical HTFET [27]. The performance comparison shows the parasitic capacitance reduction in vertical HTFET (with 37nm gate pitch and 16nm L_g) due to the asymmetrical source/drain design induced overlap capacitance reduction. HTFET also shows improved f_T at reduced DC power compared to Si NMOS (Figure 12(b)) using vertical device architecture, which is promising for ultra-low power, high frequency applications.

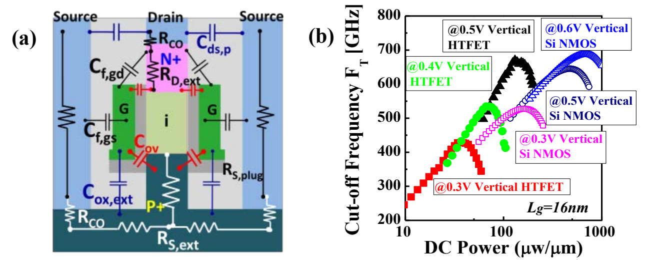


Figure 12 (a) parasitic capacitances and resistances illustration in vertical HTFET (b) cut-off frequency vs DC power comparing vertical THFET and Si NMOS with the presence of parasitics [27].

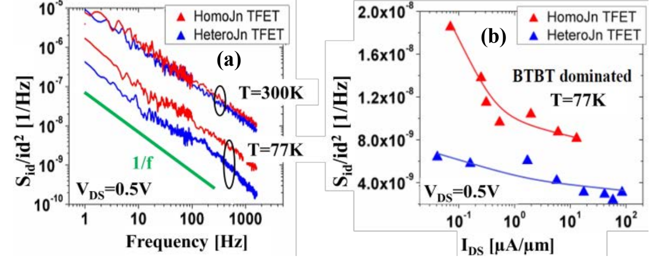


Figure 13 (a) normalized drain current noise spectrum comparing homoj- and heteroj TFET follows 1/f trend. (b) heteroj TFET exhibits lower noise at a given drain current at 77K [29].

4.5 Noise Performance

Noise performance is the key figure-of-merit for low-power analog/RF applications at low V_{cc} and scaled technology nodes. The flicker noise, as the dominant low frequency noise arising from trapping/de-trapping of carriers in multiple trap states in the gate oxide, has been characterized and modeled for III-V homojunction (homoj-) TFET and heterojunction (heteroj-) TFET [29]. As shown in Figure 13, heteroj-TFET exhibits lower flicker noise levels due to the reduced tunneling barrier height and larger effective channel length (the spread of the band-to-band generated carriers) at a given on-current compared to homoj-TFET. Further electrical noise modeling and circuit-level implementation is still required to evaluate the noise performance of TFET based circuits.

5. TFET Challenges

III-V nTFETs have been demonstrated with superior energy efficiency at reduced V_{CC}, but the design of III-V pTFETs with performance comparable as nTFETs remains challenging. To boost I_{on} in TFET, the source material requires heavily doped to achieve a higher junction electric field for tunneling. In the source design of III-V pTFETs, the Fermi level moves deeply into the conduction band with increased source doping due to the low density of states in the conduction band. The source carriers hence having a large temperature dependent portion also participate in tunneling. It leads to a kT/q limited SS in III-V pTFET [28]. The tradeoff between achieving high I_{on} and steep SS remains as a barrier in III-V pTFET design.

Given the vertical device architecture and asymmetrical source/drain, TFET layout design is different compared to Si FinFETs. Due to the usage of the side-gating contacted outside the active region, possible density gain over the lateral devices can be achieved. The cascaded inverter and 2-input NAND layouts using Si Fin-FETs and vertical TFETs are shown in Figure 14 (a-b). For cascaded inverter, the vertical TFETs are parallel connected, having source terminals shared at the bottom with metal plugs connected to the surface [27]. For

TFET based 2-input NAND design, the series connected devices require device isolation with increased area. Further area evaluation and layout optimization are required in TFET based circuit design.

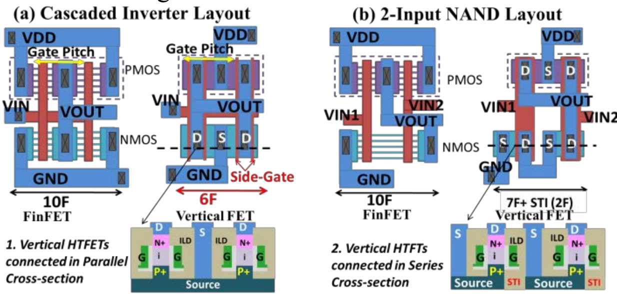


Figure 14 (a) Cascaded inverter and (b) 2-input NAND gate layout using vertical TFET comparing with Si FinFET [27].

6. Conclusions

In this paper, we have reviewed the device performance and metrics of the steep switching TFET and the device-circuit co-design techniques using TFET for energy efficient digital and analog/RF circuit applications. TFET presents improved energy efficiency at low supply voltages compared to state-of-art CMOS, which can enable further V_{DD} scaling and power reduction for digital domain application. For analog/RF application, the steep switching of TFET overcomes the $40V^{-1}$ g_m/I_{DS} limit to enable further energy savings beyond the CMOS. With reduced turn-on voltage and improved I_{on}/I_{off} at reduced voltage window due to the steep switching, TFET is also desired to improve the circuit sensitivity for low RF input signal hence improve the signal utilization and efficiency. TFET also shows superior soft-error resilience, temperature insensitivity and desired high frequency operation. Due to the uni-directional conduction, enhanced on-state Miller capacitance effect, vertical device architecture and asymmetrical source/drain design, TFET based circuit design requires modification and optimization to achieve the optimal performance comparing to the traditional CMOS circuits. Variations and parasitics impact on the TFET circuit performance need to be addressed in future work.

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