Exploration of Vertical MOSFET and Tunnel FET Device Architecture for Sub 10nm Node Applications

H. Liu, D. K. Mohata, A. Nidhi, V. Saripalli, V. Narayanan and S. Datta
The Pennsylvania State University, PA 16802, E-mail: hxl249@psu.edu, Phone: (814) 753 0026, Fax: (814) 865 7065

Introduction: With growing challenges in maintaining physical gate-length (L_g) scaling and device performance tradeoff, extending the technology roadmap with lateral devices to sub-10 nm technology node with 37nm contacted gate-pitch (L_{pitch}) is becoming increasingly difficult.[1] At or beyond this point, vertical device architecture can bring in new perspectives with regards to increasing device density and improving performance[2], simultaneously. Because vertical devices use side-gates which can be contacted outside the active region (Fig. 1), the contacted gate area can be reduced, resulting in ~40% density gain over lateral devices. However, vertical configuration brings additional gate-dielectric overlap for the gate, requires bottom source (or drain) extensions and metal plugs for the contacts, all of which increase the device parasitic elements. In this abstract, a double-gate vertical device architecture has been evaluated using TCAD simulations. Besides showing the area advantage, parasitics included energy efficiency and switching performance of vertical n-channel MOSFET and n-type Hetero-junction Tunnel FET (N-HTFET) are systematically compared for low operating power (LOP) logic applications. L_{pitch} of 37nm is used to target sub-10nm technology node, while L_g of 16nm is used to maintain short channel effects.

Vertical FET Physical Layout: The cascaded inverter layouts using planar CMOS, FinFETs and vertical FETs are shown in Fig. 1. The vertical FETs have source terminals connected at the bottom and eventually to the surface with metal plugs. The source region is recessed down to reduce the gate-to-source capacitance. FinFET inverters exhibit similar area as planar CMOS (10F×W), while the vertical FETs show ~40% area reduction (Table I).

Vertical FET Parasitics: For the evaluation of the parasitic components, the base structure of shared bottom-source is used as shown in Fig. 2(a). The device spacing (L_{pitch}) is 37nm. The total gate fringe capacitance $C_{g,fringe}$ comprises of side-gate to plug, side-gate to drain extension and side-gate to source extension capacitance due to fringe field through the low-k dielectric spacer. The total overlap capacitance, C_{ov} includes gate to source/drain overlap of 1 nm. The lateral gate-oxide extension ($L_{ox,ext}$) induced $C_{ox,ext}$ becomes part of $C_{g,fringe}$ because of the recess and low-k filling. Vertical HTFET and Si NMOS I_{DS}-V_{GS} characteristics are compared in Fig. 2(b). Minimum sub-threshold slope of 30mV is achieved in HTFET. With off-state current I_{OFF} <5nA/μm (LOP target) at V_{GS}=0V, on-state current I_{ON} of 403μA/μm and 397μA/um at V_{DD}=0.5V are obtained in vertical Si NMOS and III-V HTFET, respectively. Fig. 3 provides the parasitic extraction methods with small-signal simulation using vertical Si NMOS as an example. $C_{g,fringe}$ of 0.15fF/μm is extracted from ϵ_{ILD} variation. C_{ov} of 0.213fF/μm is obtained from $C_{g,total}$-$C_{g,fringe}$ extrapolation at $L_{g,eff}$=0nm. $C_{ox,ext}$ of 0.047fF/μm is extracted from $L_{ox,ext}$ variation on the 1st order estimation. The extension series resistance ($R_{SD,ext}$) of 35Ω-μm is extracted from Z parameter analysis.[3] $R_{S,plug}$ is below 0.5Ω-μm for plug height of 28nm with tungsten. Similar evaluations are performed for both Si NMOS and III-V HTFET at V_{DD}=0.3V and 0.5V.

Vertical FET Energy-Performance: As shown in Fig. 4, $C_{g,total}$ of III-V HTFET is dominated by C_{gd} at high V_{GS}, mainly due to the enhanced Miller capacitance.[4] When V_{GS} increases from 0 to V_{DD}, HTFETs offers smaller $C_{g,total}$ compared to Si NMOS (Fig. 5) due to (i) the lower density of states electron mass of III-V and (ii) the required lower drain doping to prevent ambipolar conduction, which also results in C_{ov} reduction, however with a penalty of increased $R_{D,ext}$. Fig. 6 shows the parasitic capacitance components comparison between HTFET and Si NMOS at different V_{DD}. $C_{g,fringe}$ is similar for both Si NMOS and III-V HTFET. Despite lower I_{ON}, the low $C_{g,total}$ in HTFET offers advantage in energy and delay reduction. Table III shows the device performance comparison. At V_{DD}=0.5V, intrinsic delay ($\tau_{intrinsic}$= $C_{g,total}$ × V_{DD}/I_{ON}) of 0.438ps for III-V HTFET and 0.714ps for Si NMOS can be obtained. Energy-delay figure of merit is then evaluated for FO1 (fan-out=1) inverter assuming symmetric PMOS performance with Miller effect considered (Fig.7). Si NMOS can achieve 1ps delay at V_{DD} >0.6V, while HTFET has superior energy efficiency below 0.6V. Fig. 8 shows the cut-off frequency (F_T) versus DC power relationship, considering the parasitics. III-V HTFET presents further advantages for low-power analog applications. Since the contact resistance (R_{co}) dominates the series resistance beyond 32nm technology node [1], the analysis of R_{co} effect is important (Fig. 9). Considering R_{co} of 100Ω (resistivity of 10^{-8} Ω-cm^2) for 1×0.01μm^2 contact, HTFET and Si NMOS show ~26% and ~40% I_{ON} degradation at V_{DD}=0.5V, respectively. R_{co} requires further improvement to maintain the performance.

Conclusions: A vertical device architecture having ~40% density improvement over planar for sub-10nm technology node has been evaluated for Si NMOS and III-V HTFET with L_g=16nm. For LOP applications including the effect of parasitic elements, the HTFET presents superior energy efficiency and desired low-power analog performance for V_{DD}<0.6V, while MOSFET is superior for V_{DD}>0.6V. To further improve MOSFET performance, I_{ON} needs to be improved with higher injection velocity materials (e.g. III-V). For delay reduction, the parasitic capacitances (C_{ov} and $C_{g,fringe}$) and contact resistance need to be further engineered for both MOSFETs and TFETs.

[1] L. Wei et al., *IEEE Trans. Elec. Dev., vol. 56, no. 2,* 2009.
[2] D. K. Mohata et al., *IEEE IEDM Tech. Dig.*, 2011.
[3] R. Torres-Torres et al., *IEEE Electronics Lett., vol. 39, no. 20, 2003.*
[4] S. Mookerjea et al., *IEEE Trans. Elec. Dev., vol. 56, no. 9,* 2009.

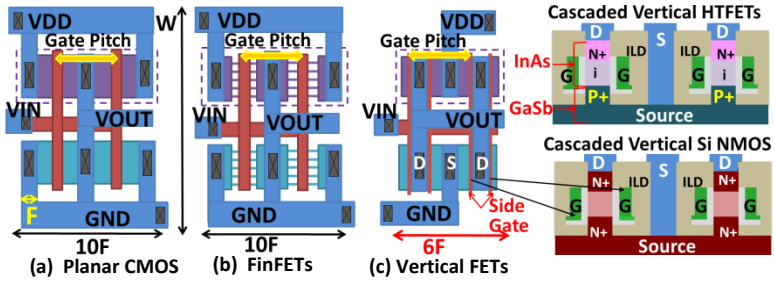

Fig. 1 Planar CMOS (a), FinFET (b) and vertical-FET (c) cascaded inverter layout example with illustrated gate-pitch and cascaded vertical NMOS and HTFETs cross-session. F is the minimum feature. The vertical FETs have reduced layout area.

Table I Normalized Area of Laterial/Vertical FETs

	Planar CMOS	FinFET	Vertical FET
Cascaded Inverter	100%	100%	~ 60%

Table II Parameters in Simulation Setup

L_{pitch}	37nm	L_{N+}	5nm
L_g	16nm	t_B	7nm
$L_{ox,ext}$	7nm	EOT	0.7
L_{ov}	1nm	t_G	5nm
L_{res}	5nm	$\varepsilon_{ILD}/\varepsilon_0$	2.3
$L_{s,ext}$	11nm	ρ_{gate}	5.64 Ω/□
L_{plug}	28nm	t_{plug}	8nm
Si NMOS S/D Doping		1e20 cm^{-3}	
N-HTFET Source Doping (GaSb)		2e17 cm^{-3}	
N-HTFET Drain Doping (InAs)		5e19 cm^{-3}	
For N-HTFET: $E_{g,GaSb}$=0.804eV, $E_{g,InAs}$=0.44eV, ΔEc=0.796eV			

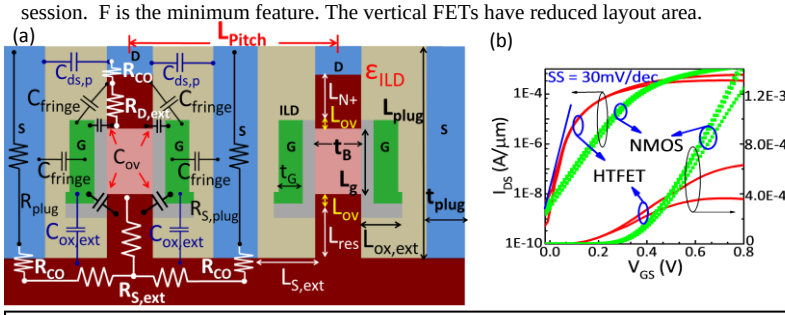

Fig. 2 (a) Simulated structure showing parasitic components. Lpitch=37nm for 10nm technology. (b) I_{DS}-V_{GS} at different V_{DS} of vertical Si NMOS and HTFET. I_{ON}=23 μA/μm, 403 μA/μm, 743 μA/μm for Si NMOS at V_{DD}=0.3V, 0.5V, 0.61V. I_{ON}=130 μA/μm, 398 μA/μm for HTFET at V_{DD}=0.3V, 0.5V.

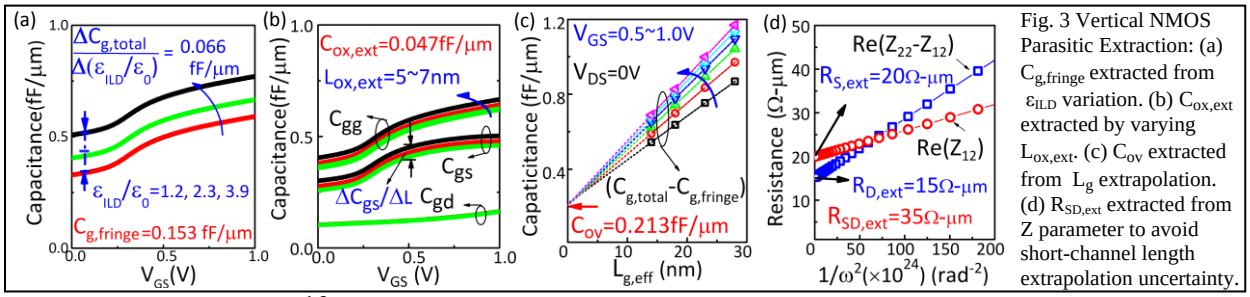

Fig. 3 Vertical NMOS Parasitic Extraction: (a) $C_{g,fringe}$ extracted from ε_{ILD} variation. (b) $C_{ox,ext}$ extracted by varying $L_{ox,ext}$. (c) C_{ov} extracted from L_g extrapolation. (d) $R_{SD,ext}$ extracted from Z parameter to avoid short-channel length extrapolation uncertainty.

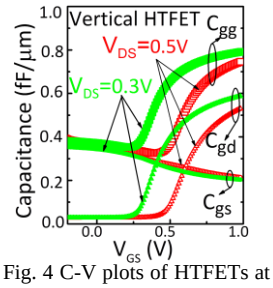

Fig. 4 C-V plots of HTFETs at V_{DS} = 0.3V, 0.5V. At low V_{GS}, C_{gg} is dominant by C_{gs}. As V_{GS} increases, C_{gd} dominates as on-state enhanced C_{miller}.

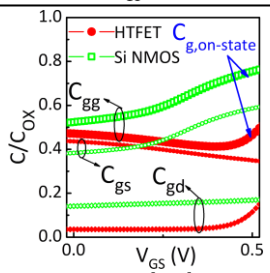

Fig. 5 Normalized capacitance comparison of vertical NMOS and HTFET at V_{DD}=0.5V. Lower C_g in HTFET comes from lower drain doping.

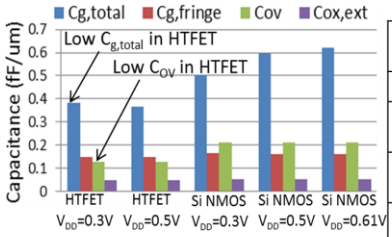

Fig. 6 $C_{g,total}$ and parasitic capacitance comparison of vertical HTFET and Si NMOS. HTFET presents lower $C_{g,total}$ and reduced C_{ov} compared to Si NMOS.

Table III Performance Comparison

	Vertical HTFET	Vertical NMOS
V_{DD} (V)	0.5	0.5
$C_{g,total}$ (fF/μm)	0.367	0.595
$C_{g,fringe}$ (fF/μm)	0.148	0.153
I_{OFF} (nA/μm)	5	5
I_{ON} (μA/μm)	398	403
$R_{SD,ext}$ (Ω-μm)	52	35
τ intrinsic (ps)	0.438	0.714

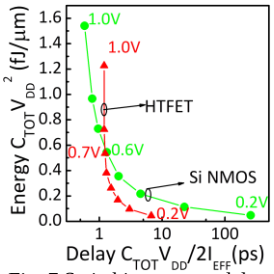

Fig. 7 Switching energy-delay for FO1 inverter using effective current (I_{EFF}) evaluation. Cross-over happens at V_{DD}=0.6V for NMOS. HTFET shows lower power advantage below 0.6V.

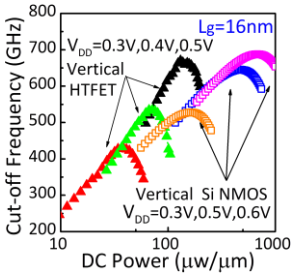

Fig. 8 F_T-DC power of vertical HTFET and Si NMOS of L_g=16nm. HTFET shows superior high frequency performance at low DC power.

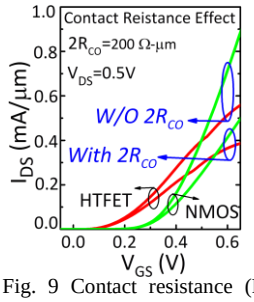

Fig. 9 Contact resistance (R_{co}) effect on vertical HTFET and Si NMOS. HTFET shows lower current degradation (26%) with large R_{co} than NMOS (40%) due to high tunneling resistance.

$$I_{EFF} = (I_H + I_L)/2$$

$$I_H = I_{DS}|(V_{GS} = V_{DD}, V_{DS} = 0.5V_{DD})$$

$$I_L = I_{DS}|(V_{DS} = V_{DD}, V_{GS} = 0.5V_{DD})$$

$$C_{TOT} = 2(C_{g,total} + C_{Miller})$$

$$C_{ox,ext} \approx \frac{\partial C_{gs,total}}{\partial L_{ox,ext}} L_{ox,ext}$$

$$C_{g,fringe} = \frac{\partial C_{g,total}}{\partial \epsilon_{ILD}} \epsilon_{ILD}$$

$$C_{ov} = \left(C_{g,total} - C_{g,fringe}\right)|_{L_{g,eff}=0}$$

$$R_{S,ext} = Re(Z_{12})|_{1/\omega^2=0}$$

$$R_{D,ext} = Re(Z_{22} - Z_{12})|_{1/\omega^2=0}$$