Reduction of Charge Transfer Region Using Graphene Nano-ribbon Geometry for Improved Complementary FET Performance at Sub-Micron Channel Length

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In recent years, use of graphene nano-ribbons to improve device performance through the opening of a small transport gap has been of great interest, with demonstrations of high performance RF graphene devices using nano-ribbon, as well as nano-constriction, geometries [1,2]. While [1] utilizes a nano-ribbon geometry and reports an improvement in f_T of 3× to 60GHz by moving from 100 nm to 40 nm wide nano-ribbons, [2] suggests that use of nano-constrictions within the channel instead of a conventional nano-ribbon geometry can improve gate modulation by keeping the ratio of the channel resistance high compared to the contact and access resistances. On the other hand, recent work by Smith *et al* [3] has shown experimental evidence for improved current injection at the graphene edge versus the graphene bulk, leading to 20% improved contact resistance using nanoribbon patterned contacts, suggesting that an *all* nano-ribbon geometry may be suitable for high performance devices. In this work, we investigate the effect of nano-ribbon geometries on graphene device performance and explain its effect on reducing the negative impact of Dirac point shift due to charge transfer into the graphene channel from the metal-graphene contact thereby leading to improved device performance and balanced n, p FET performance at sub-micron channel lengths.

Graphene devices are prepared on quasi-free-standing epitaxial graphene with Hall mobilities ranging from 1500 – 3000 cm^2/V-sec at a carrier density of 8 – 9×10^{12} cm^{-2}. Fifteen sets of top-gated (50 nm HfO_2) transistors with widths 20, 5, 1, and 0.05 μm and with channel lengths ranging from 200 nm to 10 μm are fabricated, where a modest transport gap is expected only for the case of the 50 nm wide nano-ribbon. Figure 1a shows a schematic of several graphene devices with different channel lengths and widths, while Figure 1b shows SEM micrographs for three different width and length devices. Figure 2a and 2b show the typical transfer characteristics for 20 μm wide graphene sheet and 50 nm wide graphene nano-ribbon devices as a function of channel length (V_{ds} = 50 mV), where the presence of a p-type charge transfer region [4-6] near the metal contact leads to a positive shift in V_{Dirac} and quenching of the n-branch as channel length decreases. The charge transfer region, illustrated schematically in Figure 2d and 2e, extends from the metal contact into the graphene channel, limiting modulation of the channel, acting as an additional parasitic resistance, and contributing to asymmetry between the n and p device performance - all of which severely limit performance of complementary graphene FETs, especially at ultra-small channel lengths (Fig. 2a,b).

Although all the devices show the effects of the charge transfer region, the reduced width nano-ribbon devices show significantly smaller V_{Dirac} shift and improved p, n symmetry relative to the 20 μm wide sheet counterpart, where the 50 nm wide nano-ribbon exhibits the least shift in V_{Dirac}. In order to understand this phenomenon, the capacitive gate coupling between the metal gate and the graphene is simulated (Fig. 3a,b), showing a significant increase in gate coupling as ribbon width is decreased (up to 2× increase moving from 20 μm to 50 nm). The simulated capacitance is compared with capacitance values extracted from the experimental data by fitting the V_{Dirac} shift as a function of channel length for the four investigated widths using a fixed potential decay into the channel (equation 2, l_s=100 nm), which is modified by the gate bias according to a gate capacitance (C_{ox}) that is varied with width (Fig. 3b). The experimental fit is roughly 2× the simulated values and within experimental error. At the shortest channel length, V_{Dirac} shift of 5V for the 20 μm wide sheet is reduced to ~1V for the 50 nm wide nano-ribbon, showing that enhanced charge control in graphene nano-ribbon devices is successful in reducing the effective length of the charge transfer region by enhancing gate control.

Besides reducing V_{Dirac} shift, the reduction in charge transfer region leads to enhanced DC device performance. Figure 4a and 4b plot the peak transconductance (g_m) for the p and n-branch, respectively, and show a monotonic increase in g_m of up to 4× at small channel lengths (≤1 μm), which is attributed to both improved charge control and reduced access resistance due to the reduction in charge transfer regions with nano-ribbon geometry. The 50 nm wide device, however, shows degraded long-channel, on-current performance relative to the 20, 5, and 1 μm wide cases, indicating that mobility degradation due to edge scattering may begin to effect device performance at these small widths. Figure 4c shows an increase in symmetry between the n and p-branch of the transfer curve by moving to nano-ribbon geometries, providing additional evidence for the reduction in charge transfer region, which is known to contribute to device asymmetry through the formation of a p-n junction at the metal contact.

[1] Meng *et al*, IEEE Trans. Elec. Dev., 2011
[2] Habibpour *et al*, IEEE Trans. Micro. Tech. 2013
[3] Smith *et al*, ACS Nano, 2013
[4] Mueller *et al*, Phys. Rev. B, 2009
[5] Nouchi *et al*, Appl. Phys. Express 4, 2011
[6] Khomyakov *et al*, Phys. Rev. B 82, 2010

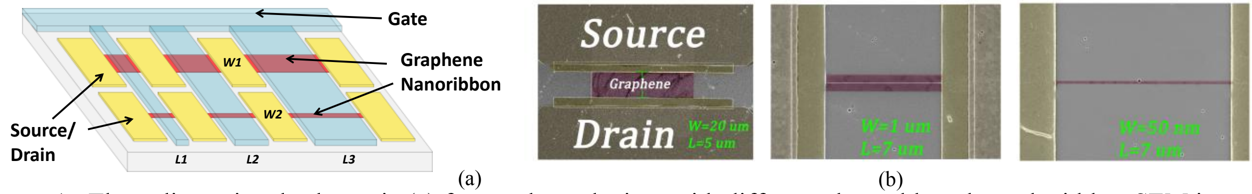


Figure 1. Three dimensional schematic (a) for graphene devices with different channel lengths and widths. SEM image of un-gated graphene transistor (b) showing channel widths ranging from 20 um to 50 nm.

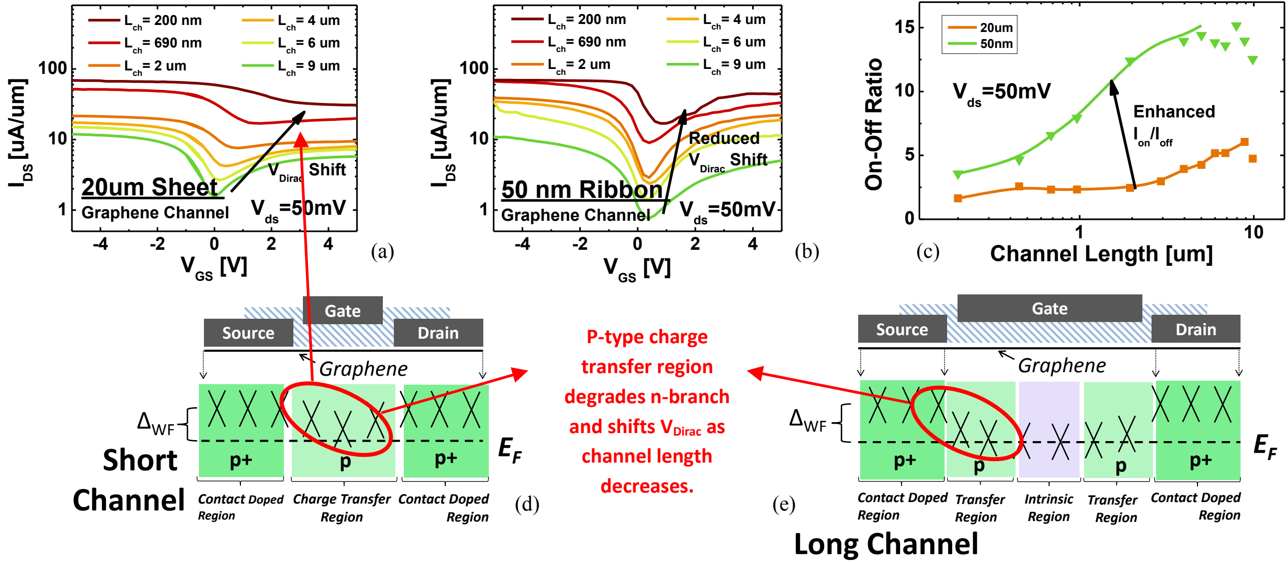


Figure 2. Collection of transfer curves as a function of channel length for 20 um wide (a) and 50 nm wide (b) transistors showing improved symmetry and reduced Dirac shift for the 50 nm devices as well as enhanced I_{on}/I_{off} (c). Schematic representation of the charge transfer phenomenon responsible for V_{Dirac} shift in short (d) and long (e) channel devices.

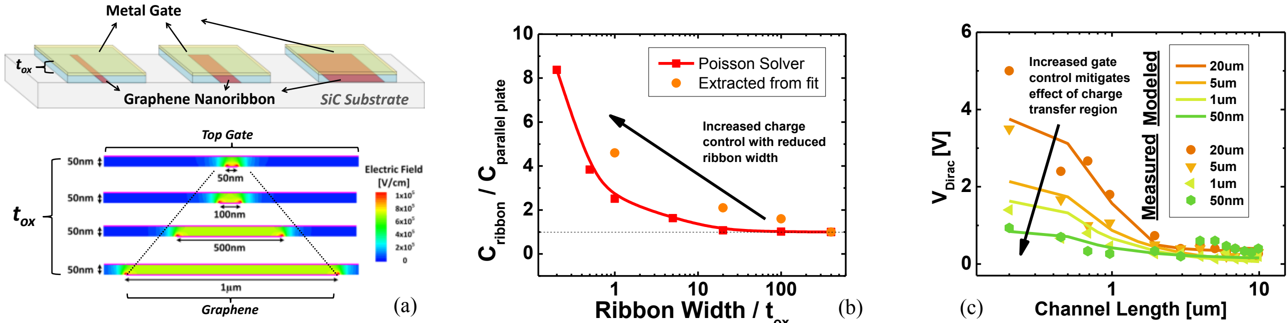
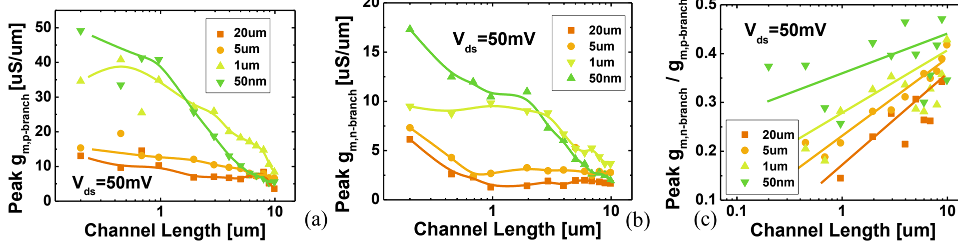


Figure 3. Modeled electric field for gated graphene nano-ribbons (a) showing field enhancement for small ribbon widths. Plot of simulated C_{ribbon} / $C_{parallel\ plate}$ for various ribbon widths compared to the extracted capacitance from the experimental fit of V_{Dirac} shift versus channel length (b). Plot of V_{Dirac} shift versus channel length (c) showing the modeled and experimental data where an exponential decay of the charge transfer into the channel (equation 2) is assumed and fit to the data by scaling the capacitive gate coupling (equation 4).



Equations

(1) $\sigma(x) = \frac{-qD_0\mu(x)|\mu(x)|}{2A}$

(2) $V(x) = \frac{V_B}{\left(\sqrt{x/l_s + \beta_2^2} + \beta_1 - \beta_2\right)^{1/2} (x/l_s + \beta_1^{-2})^{1/4}}$

(3) $Q_{Total} = 2\int_0^{l_s} \sigma(x)dx$

(4) $\Delta V_{Dirac} = \frac{Q_{Total}}{Cox}$ Ref [6]

Figure 4. Peak g_m as a function of channel length for the p-branch (a) and n-branch (b), showing the effect of nano-ribbon geometry on improving short channel device performance, where reduced n-branch performance is attributed to the formation of a p-n junction at the metal contact. Ribbon geometry is found to improve n, p symmetry over sheet geometries (c).

ΔV_{Dirac} (4) was computed assuming a potential profile decay (2) of characteristic length l_s=100nm.