Soft-Error Performance Evaluation on Emerging Low Power Devices

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***Abstract*—Radiation-induced single-event upset (SEU) has become a key challenge for cloud computing. The proposed introduction of low bandgap materials (Ge, III-Vs) as channel replacement and steep switching devices for low-voltage applications may induce radiation reliability issues due to their low ionization energy and device architecture. In this paper, the soft-error generation and propagation in Si FinFET, III-V FinFET, and III-V Hetero-junction tunnel FET (HTFET) are investigated using device and circuit simulation. III-V FinFET shows enhanced charge collection compared with Si FinFET, whereas HTFET shows significant reduction of the bipolar gain effect and charge collection. Soft-error rate (SER) evaluation methodology has been proposed for these emerging devices based on the critical LET extraction. SRAM bit flip, electrical masking effect, and latching window masking effect have been analyzed with supply voltage scaling. The SER evaluation of SRAM and logic shows that HTFET-based circuits are promising for radiation resilient ultra-low power applications. III-V FinFET shows increased SER for SRAM for V_{DD} range of 0.3–0.8 Vand reduced logic SER below 0.5 V compared with Si FinFET.**

***Index Terms*—Heterojunction tunnel FET (HTFET), III-V FinFET, Bipolar gain effect, soft-error rate (SER), SRAM bit-flip, electrical masking, latching window masking.**

I. Introduction

With growing numbers of processors in data centers and constrained power budgets for high-end computation, radiation-induced single-event upset (SEU) has become a key challenge for cloud computing these days. According to the reported experiment results [1], the soft-error rate (SER) per logic state bit increases 8% for each technology generation. With the number of state bits per chip doubling at each generation, the expected SER per chip will have 100 times increase from 180nm to 16nm technology node [2], which can result in a faster-increasing trend of total data center SER (Fig. 1). Another key limit for today's system design is the power consumption budget in silicon CMOS technology. For low power applications these days, the near threshold computing as well as the subthreshold circuit design has been widely studied to achieve the optimal energy efficiency with the tradeoff between overall throughput and performance at reduced supply voltages [3]. However, the reduction of the circuit node charge, which is proportional to the supply voltage, will induce significant increase of SER [4] as shown in Fig. 2, which may further prevent the projected voltage scaling [5] due to the reliability requirements.

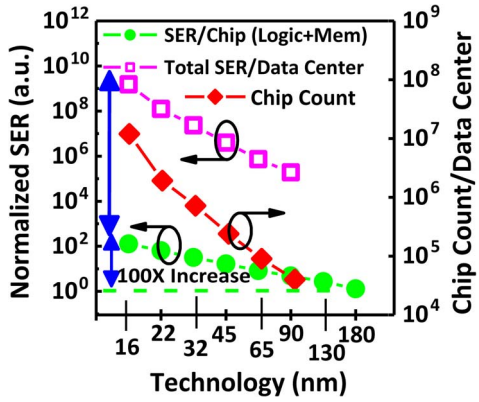

Fig. 1. SER per chip and total SER trend per data center with technology scaling and chip count increase [1], [2].

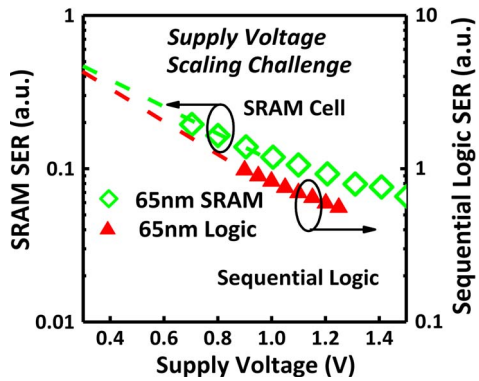

Fig. 2. Soft error rate (SER) with voltage scaling for 65 nm technology [4].

To extend the improvement of energy efficiency along the technology roadmap, low bandgap materials (e.g., germanium, III-Vs) have been proposed as channel replacement for mobility enhancement [6]. The steep switching devices (e.g., III-V Tunnel TFET [7]–[9]) have also been demonstrated to overcome the non-scalable threshold voltage limit (tradeoff between off-state leakage and on-state drive strength) in CMOS technology. These emerging devices have offered new perspectives with improved performance and energy efficiency, especially

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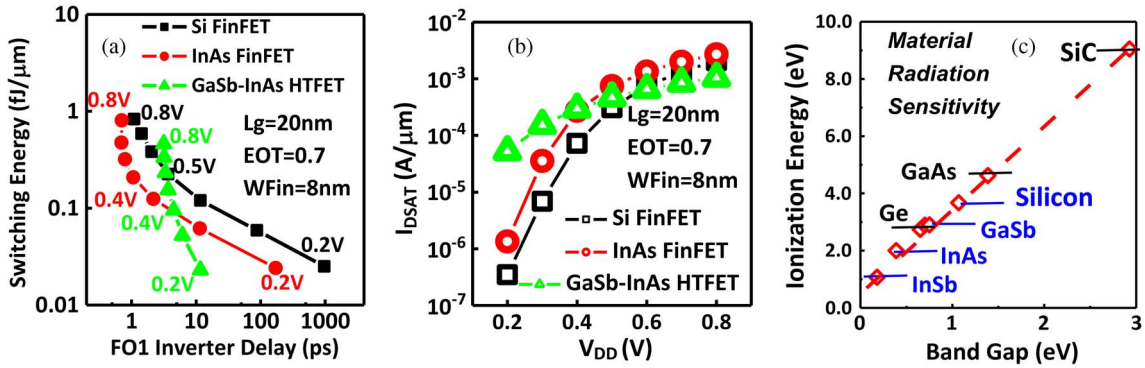

Fig. 3. (a) Switching energy vs. delay performance and (b) drive current I_{DSAT} vs. supply voltage V_{DD} for Si FinFET, III-V FinFET and HTFET. HTFET shows superior energy efficiency below 0.4 V. (c) Radiation ionization energy with band gap for various semiconductor materials [12].

at reduced supply voltages [10], [11] as shown in Fig. 3(a) and (b). From the soft-error point of view, however, the narrow bandgap materials generally have low ionization energies [12], [13], which are more sensitive to neutron radiation compared to Si (Fig. 3(c)). Experimental and simulation studies on radiation-induced transient current generation in III-V HEMTs and HBTs have been performed in [14], [15], showing transient current generation difference due to material and device architecture change. However, the neutron induced charge generation analysis as well as the circuit-level SER has not been systematically investigated for low power emerging devices such as III-V FinFETs and TFETs.

In this paper, the soft-error generation and propagation in Si FinFET, III-V FinFET and III-V Hetero-junction Tunnel FET (HTFET) are investigated for technology assessment from a soft-error perspective. Due to the material and device architecture differences and lack of SPICE models for circuit analysis, we has studied the transient error generation using the device simulation and Verilog-A modeling technique [10] of these emerging devices. To evaluate the SER performance, we have developed the methodology based on the device simulation and critical LET extraction for SRAM and logic, and compared the SRAM bit-flip, electrical and latching window masking effects with supply voltage scaling.

The current paper is organized as follows. Section II discusses the charge collection and device-level transient current generation in Si FinFET, III-V FinFET and HTFET. Section III describes the SER evaluation methodology using device to circuit simulation. The critical LET extraction for SRAM and combinational logic as well as the SRAM bit-flip, electrical masking and latching window masking effects are presented in Section IV. Section V compares the SRAM SER and logic SER with voltage scaling for these three types of emerging devices, respectively. The conclusion is given in Section VI.

II. Transient Error Generation in Emerging Devices

A. Device Simulation and Baseline Setup

In order to perform the radiation analysis using our highly-scaled and calibrated TCAD device models, we adopt the TCAD Sentaurus heavy ion model [17] to perform the radiation-induced transient current evaluation with the energy dependent impact ionization and hydrodynamic transport models. In our model, the generated electron/hole (e/h) pairs along the ion track are assumed to follow the Gaussian distribution with a spatial radius of 10 nm, a characteristic time of 2 ps and time distribution centered on 20 ps [18]. Linear energy transfer (LET) describes the charge deposition per length along the ion track, which is modeled as a fixed value along the track for fully depleted fin structure [19]. The ion strike is centered to the fin at normal incidence. The generated charge results in a transient current at the device off-state ($V_{GS} = 0$ V, $V_{DS} = V_{DD}$).

Radiation-induced ion profiles have been studied through Monte Carlo simulation showing radial expansion of e/h pairs in micrometer range for 45nm and beyond SOI technology with good agreement with the experimental data [16]. An underestimation of the radial expansion in long-channel devices may overestimate the soft-error rate due to the charge deposition confinement. In our work, the device models used for soft-error performance analysis in the later discussion are based on ultra-thin body (UTB), double-gate structures with 20 nm channel length. The ion induced charge deposition is assumed in the channel. The UTB structure is due to the electrostatic control requirement in TFET design to outperform Si FinFET at 20 nm and beyond. Here, it can effectively reduce the device terminal junction area and the length of the ion tracks in vertical direction, constraining the charge deposition in the top device layer. For the lateral expansion of the ion profile, because the device integration of these advanced emerging III-V technologies with specific engineering of the material layers and new device architectures (e.g., HTFET) requires additional device isolations, which can reduce the charge deposition effect outside the gate region. Thus, the choice of 10 nm radial charge expansion in our work is corresponding to the worst case scenario. Further study on the device source/drain design, layout and surrounding structure will improve our models for practical applications.

A study of the charge collection with fin width scaling is performed to set-up a baseline structure on three-dimensional Si FinFET with 20 nm gate length (L_g), 25 nm fin height (H_{Fin}) and 0.7 nm EOT (Fig. 4). The charge collection at the drain node at $V_{DD} = 0.5$ V and 0.8 V with LET = 50 fC/μm is shown in Fig. 5. Due to the reduction of the bulk collection [19], the total collected charge (Q_{coll}) at 1 ns after ion strike and the collected charge to the node charge ratio (Q_{coll}/Q_{node})

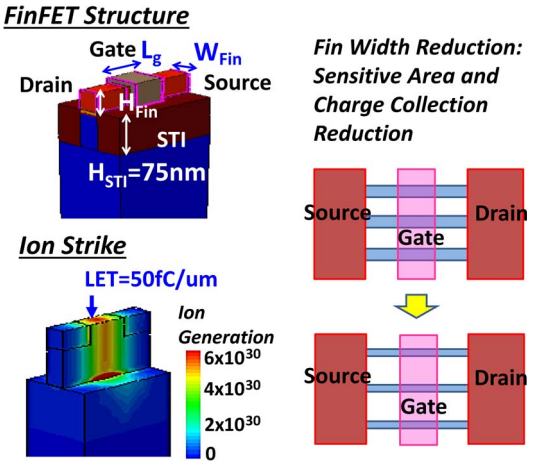

Fig. 4. Sensitive area reduction and charge collection reduction with fin width scaling due to bulk collection reduction.

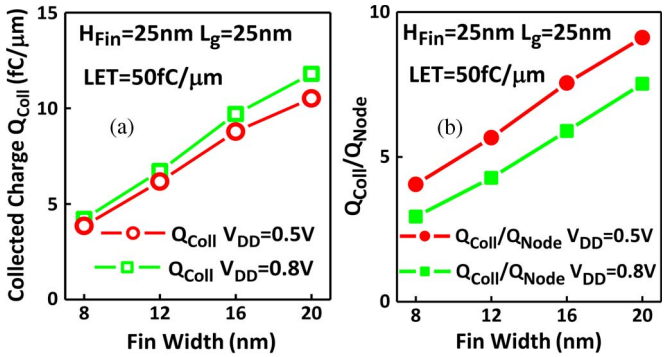

Fig. 5. (a) Charge collection with fin width (b) collected charge to node charge ratio with fin width at $V_{DD} = 0.5$ V and 0.8 V.

TABLE I
DEVICE SIMULATION PARAMETER SETUP

Gate Length (L_g)	20 nm
EOT (HfO_2)	0.7
Fin Width (t_{Body})	8 nm
InAs FinFET Source/Drain Doping	4×10^{19} cm^{-3}
Si FinFET Source/Drain Doping	1×10^{20} cm^{-3}
HTFET Source (GaSb) Doping	4×10^{19} cm^{-3}
HTFET Drain (InAs) Doping	2×10^{17} cm^{-3}

both decrease with the fin width (W_{Fin}) scaling from 20 nm to 8 nm. W_{Fin} reduction can also effectively reduce the radiation sensitive area [20], which further improves the overall radiation resilience.

In the following simulation, a fin width of 8 nm (UTB) is used as baseline in a double-gate structure with 20 nm gate length for Si FinFET, InAs FinFET and GaSb-InAs HTFET. With the quantum confinement effect, GaSb bandgap $E_{g,GaSb} = 0.804$ eV, InAs bandgap $E_{g,InAs} = 0.44$ eV and a conduction band offset $\Delta E_c = 0.796$ eV for hetero-interface are used in HTFET simulation. Table I shows the key parameters in the device simulation. The DC characteristics for Si and III-V FinFETs, which are shown in Fig. 6, have been calibrated with experimental data [21]. The HTFET model has been calibrated in [10] with atomistic non-equilibrium Green's function formalism (NEGF) simulation (a ballistic, full band, two-

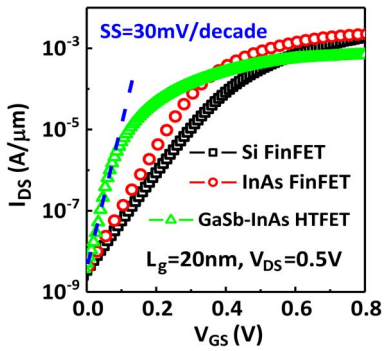

Fig. 6. DC ($I_{ds} - V_{gs}$) characterization and simulation parameters (Table I) of Si FinFET, InAs FinFET and GaSb-InAs HTFET at $V_{DS} = 0.5$ V. Average subthreshold slope (SS) of 30mV/decade over 2 orders of I_{DS} change is achieved in HTFET.

and three-dimensional Schrodinger-Poisson solver to study the quantum transport in various semiconductor devices [22] as a precise simulation approach). At $V_{DS} = 0.5$ V, HTFET shows improved I_{DS} below $V_{GS} = 0.5$ V and $V_{GS} = 0.3$ V compared to Si FinFET and InAs FinFET, respectively. The average subthreshold slope (SS) is 30 mV/dec, which is extracted over 2 decades of current change.

B. Transient Current Generation

In fully-depleted-channel devices (e.g., SOI MOSFETs, FinFETs), the transient current generation and charge collection are significantly affected by the bipolar gain effect [23], [24]. In nMOSFETs, the generated electrons in the channel are collected at the drain node due to the source-drain bias. The generated holes, on the other hand, are stored in the body due to the source-channel barrier, increasing the channel potential. The additional electrons flow into the channel and further increase the drain node charge collection. The ratio of the total collected charge, Q_{coll}, at the drain node to the deposited charge, Q_{dep}, is known as bipolar effect coefficient.

The time evolutions of the hole density in the channel for nMOSFETs and nHTFETs is shown in Fig. 7. The ion strikes the channel center at $t = 20$ ps for each device. The higher initial hole concentration in III-V FinFET at $t = 0$ ps before the ion strike is due to the reduced density of states in InAs compared to Si. For both Si FinFET and III-V FinFET, the hole storage in the channel is clearly observed after the ion strike as discussed, causing the bipolar gain effect and additional charge collection. For nHTFET, however, the hole density in the channel region decreases fast. Similar response is also observed for the electron density in pHTFET as shown in Fig. 8.

The suppression of the hole storage in HTFET can be explained from the HTFET device operation. HTFET is essentially a reverse biased p-i-n diode with asymmetric source/drain doping. The deposited electrons can be collected at drain node (n+ region) similar as in MOSFETs, while the holes can be collected at the source node (p + region) at the same time, rather than being stored in the channel as in MOSFETs. This charge collection through the ambipolar transport leads to significant hole storage reduction in HTFET. Thus, the reduction of the minority carrier storage (e.g., hole storage in n- HTFET) in

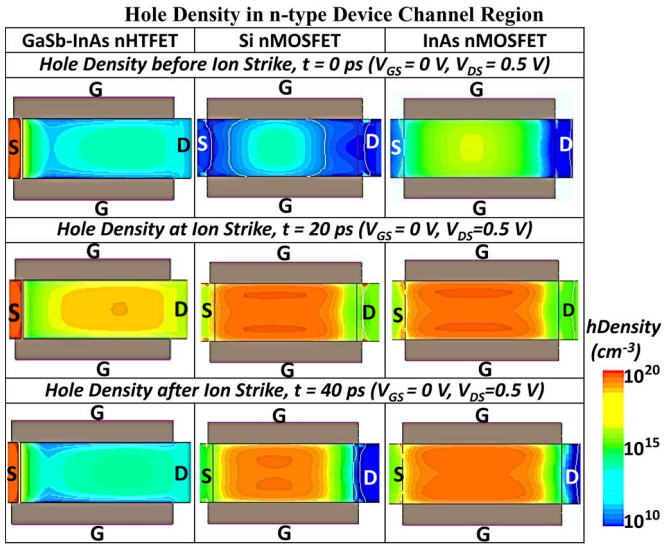

Fig. 7. Time evolution of hole density in n-type device channel region. Hole density decreases quickly in nHTFET due to ambipolar transport. Hole storage due to radiation induced charge deposition is observed in Si and InAs nMOSFETs, which induces the bipolar gain effect.

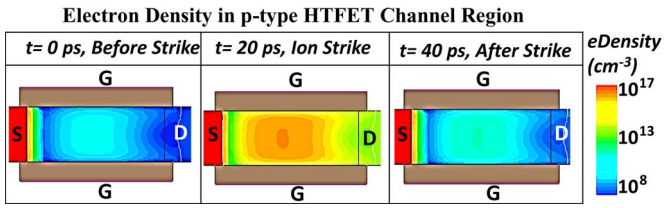

Fig. 8. Time evolution of electron density in p-type HTFET. Electron density decreases quickly in HTFET.

the channel can significantly reduce the bipolar gain effect and additional charge injection (Q_{inj}) in HTFET.

To analyze the contributions of different factors that impact transient current generation and charge collection, we further evaluated the charge collection (Q_{coll}) and charge recombination (Q_{rec}), given the charge conservation $Q_{coll} = Q_{inj} - Q_{rec}$. Fig. 9 shows the band diagram before and after the ion strike for nMOSFETs and nHTFET, which reveals the hole storage induced source barrier lowering effect. In Si FinFET, the hole storage causes 0.119 eV source barrier reduction (10% of Si bandgap, $E_{g,Si}$) at a distance of 2 nm from the source-channel junction toward the channel region, as compared to 0.0044 eV (1% $E_{g,InAs}$) reduction in HTFET. Due to the thermionic emission induced carrier injection in MOSFETs, this significant source barrier reduction results in an exponential increase of current (as device turns on), which further increases Q_{inj} in Si and III-V FinFETs. Moreover, we evaluated the charge recombination in the channel region as shown in Fig. 10(a) and (b) at 1 ns after the ion-strike. HTFET and III-V FinFET show higher Shockley-Read-Hall (SRH) recombination rate due to InAs-channel (reduced bandgap and carrier lifetime) compared to Si FinFET (Fig. 10(a)) [17], while Si and III-V FinFETs exhibit higher Auger recombination due to larger Q_{inj} [17] from the source barrier lowering (Fig. 10(b)). HTFET and III-V FinFET show overall higher Q_{rec} (including both SRH and Auger recombination) than Si FinFET.

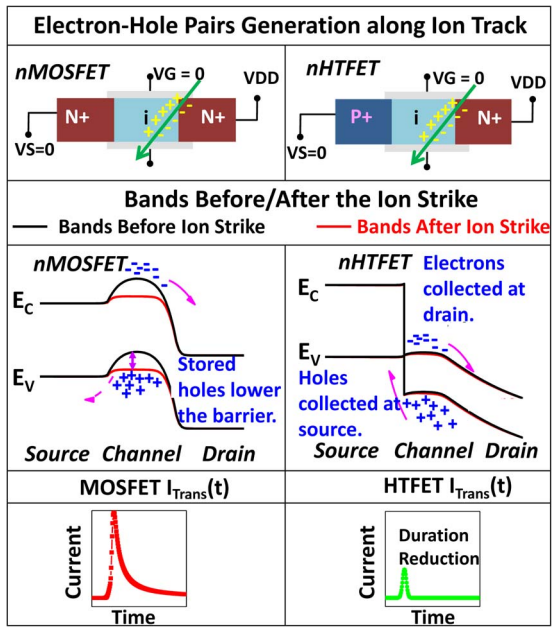

Fig. 9. Band diagrams for nMOSFET and nHTFET before/after ion strike. Hole storage induces barrier lowering and additional charge collection (bipolar gain) in nMOSFET. For nHTFET, holes can be collected at source, which reduces the bipolar gain effect.

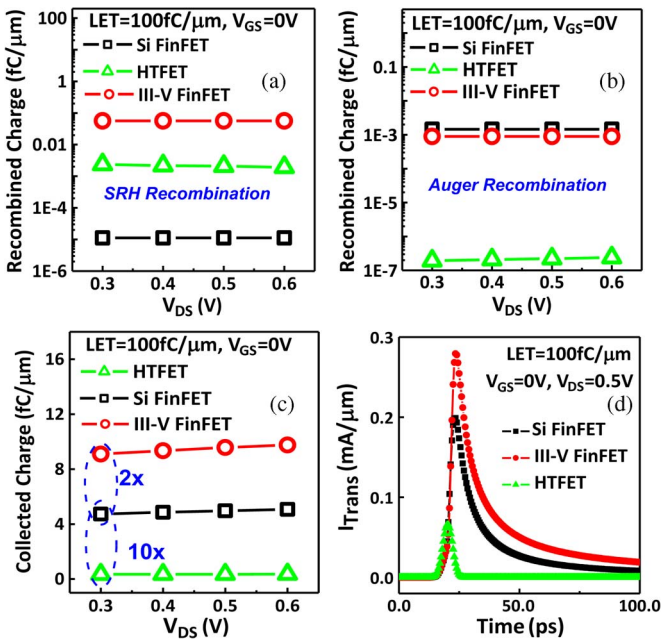

Fig. 10. Radiation induced charge recombination through (a) SRH recombination and (b) Auger recombination, (c) charge collection at 1 ns, and (d) transient current profile for each emerging device (LET $= 0.1$ pC/μm). HTFET shows reduced current magnitude and 10x charge collection reduction compared to Si FinFET. 2x charge collection enhancement is observed in III-V FinFET compared to Si FinFET due to high carrier mobility.

The depletion region volume and the electric field also strongly affect the charge collection process and drift current [28], [30]. Compared to the large reverse bias that exists between the channel and the drain in MOSFETs, HTFET exhibits a very small potential drop between the channel and drain due to its p-i-n structure and the reduced drain doping (to suppress the ambipolar operation) [32], which is also consistent with the

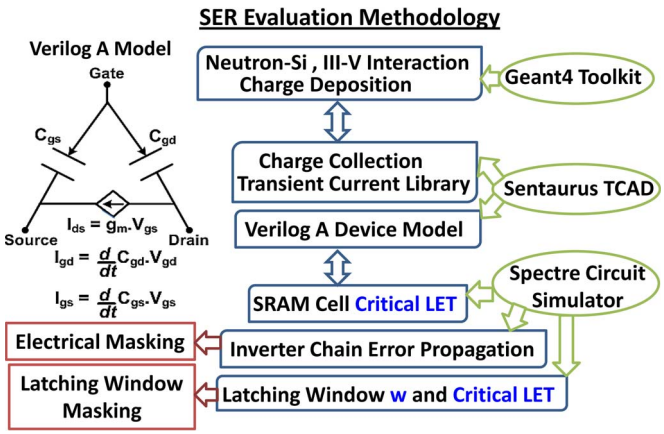

Fig. 11. SER evaluation methodology.

band bending (Fig. 9). 90% of electric field reduction can be achieved in the depleted channel of HTFET as compared to Si FinFET at $V_{ds} = 0.5$ V, which reduces the charge separation and the drift current magnitude.

Fig. 10(c) and (d) show the resulted Q_{coll} at 1ns after the ion strike at LET = 100 fC/um for different V_{DD} and transient current profile at $V_{DD} = 0.5$ V comparing Si FinFET, III-V FinFET and HTFET. Q_{coll} of approximately 6 times and 10 times over the initial deposited charge are observed for Si and InAs FinFETs, respectively, while 60% of the deposited charge is collected in HTFET. Compared to Si FinFET, a vast majority (90%) of the Q_{inj} reduction is due to suppression of the source barrier lowering and the bipolar gain effect. This is the dominant factor for much reduced Q_{coll} in HTFET, considering Q_{rec} is relatively small compared to Q_{coll}. The increased Q_{rec} (1.4x compared to Si FinFET) and the reduction of electric field in HTFET further reduces Q_{coll} and drift current (70% reduction of magnitude). Overall, HTFET exhibits approximately 80% reduction in transient duration compared to Si FinFET, while III-V FinFET shows higher transient current magnitude compared to Si FinFET due to the high channel carrier mobility, which results in enhanced charge collection.

III. Soft-Error Evaluation Methodology

The soft-error rate evaluation methodology used in this paper is shown in Fig. 11, which includes the material-level charge deposition evaluation, device-level charge collection evaluation and transient current profile generation as well as circuit-level critical LET extraction. The sea-level neutron induced charge deposition in materials such as InAs (channel material for III-V FinFET and HTFET) and Si is obtained from Geant4 [25] Monte Carlo simulation using the measured neutron spectrum [26]. The charge deposition in terms of LET is then applied to the TCAD device simulation to obtain the transient current characteristics for each type of nanoscale device at different V_{DD} and radiation strength as discussed in the previous section, which is later on applied as input to the strike node in the circuit analysis. For circuit simulation, a lookup table based Verilog-A models generated from TCAD Sentaurus has been used for each type of device based circuit implementation and

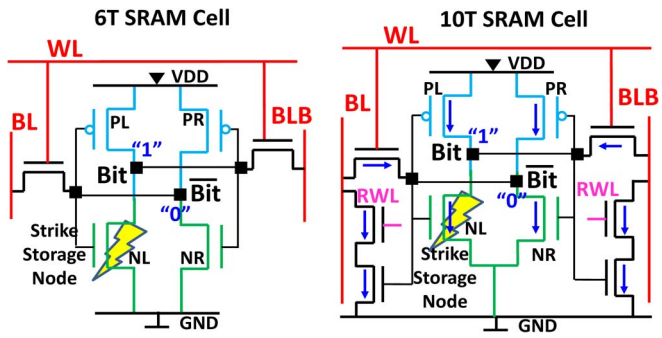

Fig. 12. 6T and 10T SRAM cell schematic. Strike on storage node induced charge exceeding node charge can cause an error. HTFET (unidirectional) current flow direction is illustrated for 10T cell.

soft-error analysis using Spectre [27]. The circuits evaluated in this work include 6T and 10T SRAM cells, FO1 inverter chain and NAND gate based D Flip-flop to study the SRAM bit-flip, combinational logic electrical and latching window masking effects. The critical LETs for SRAM cell and combinational logic are extracted with voltage scaling for SER calculation. Technology adaptable empirical model [28], which is validated on previous CMOS technology nodes, is applied to SER calculation for each emerging device based circuits

$$SER_{SRAM}(LET_{critical}) \sim A \cdot \langle Flux \rangle \cdot \exp\left(-Q_{critical}/\langle Q_s \rangle\right) \sim \exp\left(-LET_{critical}/\langle LET_s \rangle\right). \quad (1)$$

$$SER_{Logic}(LET_{critical}) \sim w/c \cdot \exp\left(-LET_{critical}/\langle LET_s \rangle\right). \quad (2)$$

$$Q_{critical} = t_{body} \cdot LET_{critical}. \quad (3)$$

Here, SER_{SRAM} and SER_{Logic} represent SRAM cell SER and combinational logic SER, respectively. A refers to the radiation sensitive device area, t_{body} is the double-gate structure body thickness, and $\langle Flux \rangle$ is the average neutron flux over the energy spectrum at the sea level. $Q_{critical}$ is the SRAM cell bit-flip critical charge, and $\langle Q_s \rangle$ is the average charge collection coefficient in the exponential function, both of which can be converted to $LET_{critical}$ and $\langle LET_s \rangle$ using (3) [23]. SER_{Logic} is proportional to error latch probability w/c [30], where w is the latching window and c is the clock cycle. Typical $\langle LET_s \rangle$ for Si is 50 fC/μm at sea-level [29], $\langle LET_s \rangle$ for InAs is obtained from Geant4 simulation.

IV. Critical LET Evaluation in Circuits

A. SRAM Critical LET Evaluation

Softs errors occur in SRAM cells when the ion strike induced collected charge exceeds the storage node charge causing the bit-flip. Fig. 12 shows the 6T and 10T SRAM cell schematics with neutron strike at the nMOSFET or nTFET connected to the bit node, which stores "1". 10T SRAM cell here uses iso-area sizing according to the reported TFET SRAM design in [10] to compare with 6T. The SRAM Critical LET is extracted at the threshold LET causing the bit-flip [29]. The 6T and iso-area 10T SRAM cell critical LET extraction is performed for both Si FinFET and III-V FinFET, while only the 10T SRAM critical

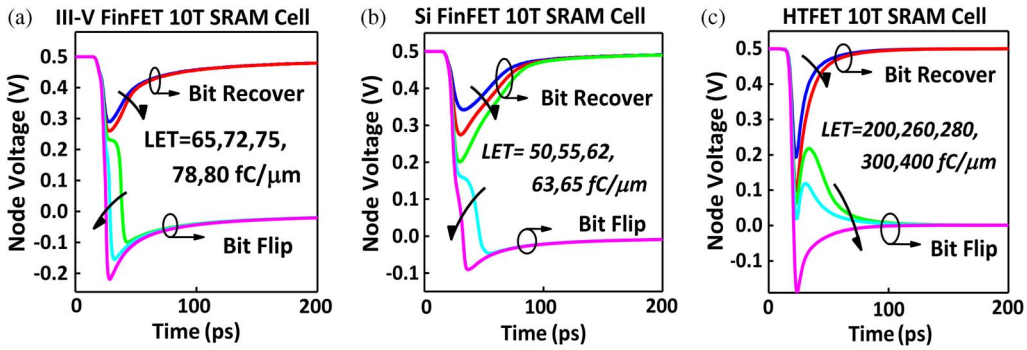

Fig. 13. 10T SRAM cell critical LET extraction and node bit-flip illustration for (a) Si FinFET, (b) III-V FinFET, and (c) HTFET at $V_{DD} = 0.5$ V. HTFET shows high critical LET and short recovery time.

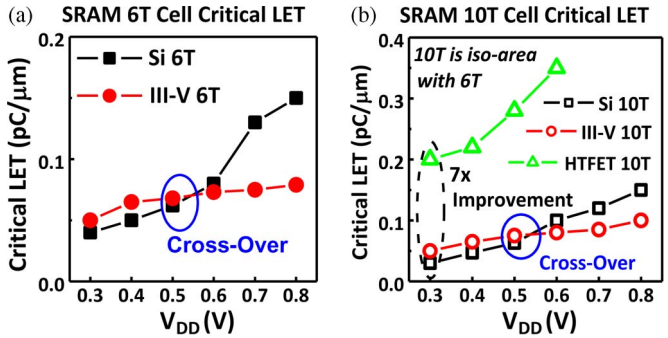

Fig. 14. (a) 6T and (b) 10T iso-area SRAM cell critical LET extraction for Si FinFET, III-V FinFET and 10T HTFET with voltage scaling. HTFET shows 7 times improvement compared to Si FinFET at 0.3 V for 10T case.

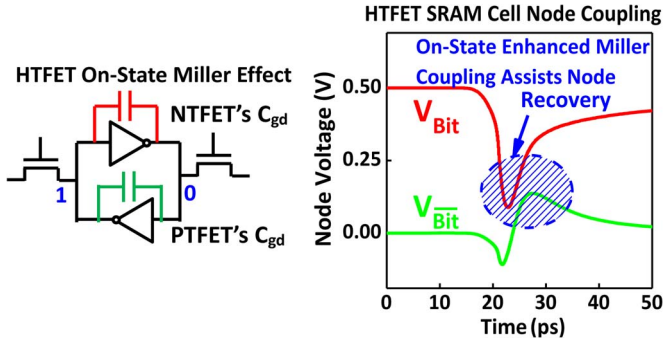

Fig. 15. HTFET on-state enhanced Miller capacitance illustration in SRAM cell and node recovery process with bit and $\overline{bit}$ node coupling.

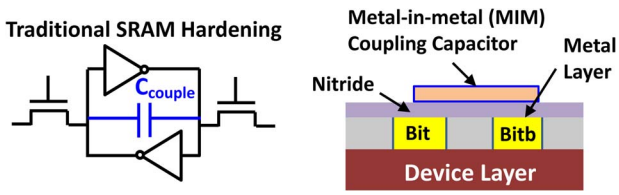

Fig. 16. Metal-in-metal coupling capacitor in SRAM cell and cross-section schematics for traditional CMOS SRAM hardening.

LET extraction is performed for HTFET. This is because of TFET's asymmetrical source/drain and uni-directional current flow characteristic, which requires additional current paths for stable read and write. It has been reported in [10] the 10T HTFET cell can achieve a desired noise margin compared to MOSFET designs.

The bit-flip comparison with LET increase is shown in Fig. 13(a)–(c) for Si, III-V FinFET and HTFET 10T SRAM cell at 0.5 V. HTFET shows improved critical LET and reduced recovery time (transient duration from the strike time to 90% node voltage recovery). The extracted critical LET for 6T (except HTFET) and iso-area10T SRAM cell is plotted with voltage scaling as shown in Fig. 14. For all the evaluated cells, the critical LET decreases with the supply voltage due to the reduced charge of the storage node. Above 0.5 V, Si FinFET cell shows higher critical LET compared to III-V FinFET, which is due to the reduced charge collection. Below 0.5 V, however, the critical LET for Si FinFET cell decreases significantly due to the low drive current near threshold operation, where III-V FinFET with improved drive current shows the cross-over. Compared to Si FinFET, HTFET shows 4.5 times improvement at $V_{DD} = 0.5$ V and 7 times improvement at $V_{DD} = 0.3$ V of the critical LET, and 50% recovery time reduction. This is due to the short transient current duration and the reduced charge collection (discussed in the Section II-B), as well as the enhanced on-state Miller capacitance effect [32].

Due to the asymmetrical p-i-n structure and tunneling mechanism, TFET exhibits different capacitance characteristics compared to MOSFET. In MOSFET, both the gate-to-source capacitance, C_{gs}, mainly contribute to the total gate capacitance, C_{gg} at the device on-state. In HTFET, however, the gate-to-drain capacitance, C_{gd}, is dominant in C_{gg}, while C_{gs} is suppressed at on-state. This enhanced on-state C_{gd} in HTFET can increase the input (gate) to output (drain) coupling during switching, which is known as enhanced on-state Miller capacitance [32]. For soft-error performance, the enhanced on-state Miller capacitance in HTFET assists the node recovery process. As shown in Fig. 15, the feedback from the HTFET $\overline{bit}$ node to bit node can improve the critical LET, which is similar to the metal-insulator-metal (MIM) coupling capacitance (Fig. 16) employed for traditional backend SRAM radiation hardening [33]. For the evaluated voltage range of 0.3 V to 0.6 V, HTFET presents superior soft-error resilience compared to Si FinFET and III-V FinFET.

B. Combinational Logic Critical LET Evaluation

In the combinational logic, the generated transient current induces a voltage pulse at circuit node, which is propagated through the circuit path. Due to the delay of the logic gates [34],

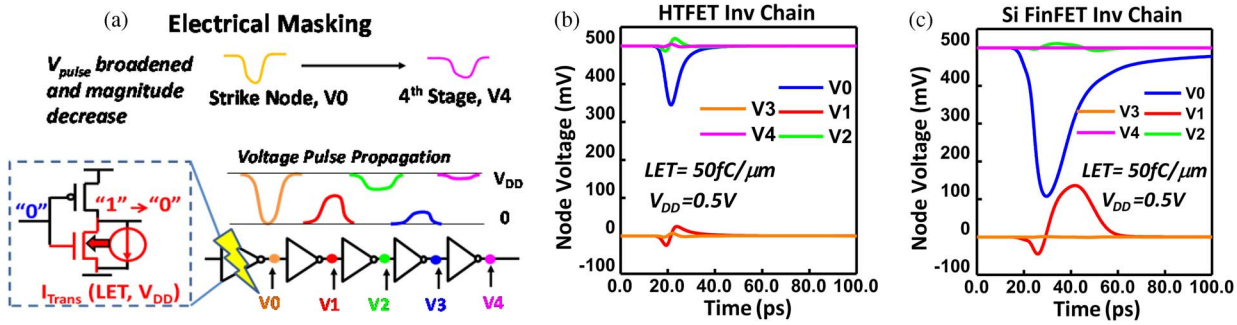

Fig. 17. (a) Electrical masking effect illustration using FO1 inverter chain. The strike is induced at the 1st stage nFET, where the transient current causing a voltage pulse at node V0. (b) Transient voltage propagation at each node from V_0 to V_4 for HTFET and (c) Si FinFET FO1 inverter chain at LET $= 50$ fC/μm strike.

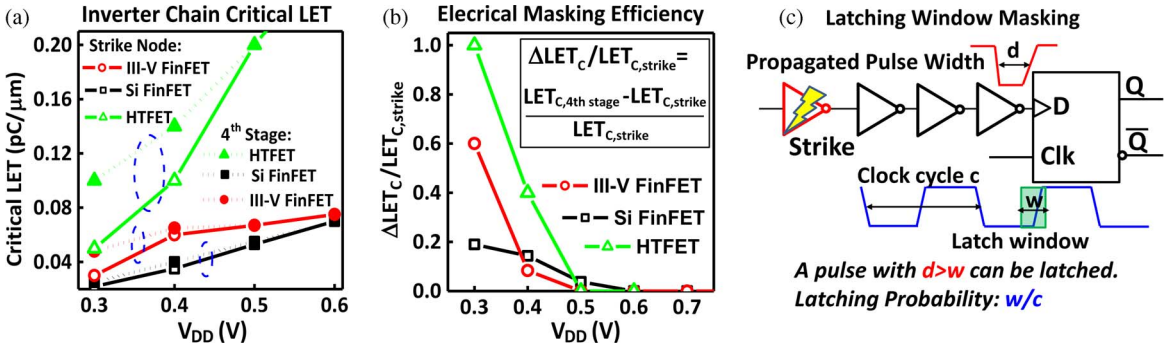

Fig. 18. (a) Inverter chain critical LET (causing $V_{pulse} > 0.5\ V_{DD}$) at the strike node and the 4th inverter stage and (b) normalized critical LET difference between strike node and 4th stage with voltage scaling. (c) DFF latch window masking schematic. Propagated transient voltage pulse width d exceeding the latch window w can be latched with the probability of w/c.

the voltage pulse (V_{pulse}) can be masked with certain number of stages during propagation, which is known as the electrical masking effect. Fig. 17(a) illustrates the error propagation evaluation using FO1 inverter chain, showing the electrical masking effect. The strike induced transient current causes a voltage pulse at the strike node, which decreases during propagation. Fig. 17(b) and (c) compares the transient voltage propagation in HTFET and Si FinFET based FO1 inverter chains at $V_{DD} = 0.5$ V. HTFET shows faster voltage degradation and reduced transient voltage duration, which is consistent with transient current characteristics (Section II). The critical LET is extracted as the threshold LET which causes the propagated V_{pulse} magnitude exceeding 0.5V V_{DD}.

Fig. 18(a) shows the critical LET with voltage scaling at the strike node and 4th stage, respectively. The increase of the critical LET between the strike node and the 4th stage in the inverter chain represents the masking effect. As shown in Fig. 18(b), the difference of critical LET between the strike and the 4th node is normalized to the critical LET of the strike node, showing the electrical masking efficiency. For all the evaluated devices, the inverter chain critical LET decreases with voltage scaling, while the electrical masking effect increases due to the increase of circuit delay with reduced V_{DD}. At low V_{DD}, the masking strength as well as the circuit radiation resilience is dominated by the drive current. As a result, below 0.4 V, III-V FinFET shows improved electrical masking effect compared to Si FinFET due to the mobility enhancement. HTFET presents superior masking effect below 0.5 V due to the abrupt switching and improved current performance. Additionally, because of the reduced transient duration (reduce bipolar gain effect) and enhanced Miller capacitance, the critical LET for HTFET of all the evaluated voltage range is greatly improved compared to Si and III-V FinFET.

Error occurs in the state element requires: (1) the transient V_{pulse} width d exceeds latch window w, which determines the latching window critical LET; (2) the transient error propagates to the state element during latching process. The error latched probability is then proportional to the latch window w to the clock cycle c ratio, w/c. The evaluation schematic of the latching window masking effect is shown in Fig. 18(c) using the NAND gate based D flip-flop (DFF). Fig. 19(a) shows the extracted w of Si FinFET, III-V FinFET and HTFET DFFs with voltage scaling. Due to the steep switching, HTFET DFF shows reduced w (improved circuit speed) at low V_{DD}, which can outperform Si and III-V FinFET DFF below 0.6 V and 0.4 V, respectively. The propagated voltage pulse d is then extracted with 4 stages of electrical masking. Fig. 19(b) shows the extracted d at $V_{DD} = 0.5$ V with the lower LET electrically masked. The latching window critical LET is then extracted at $w = d$ at different V_{DD}. As shown in Fig. 19(c), HTFET shows overall improved latching window masking effect with improved critical LET compared to Si and III-V FinFET, and 8 times improvement of critical LET over Si FinFET is observed at $V_{DD} = 0.3$ V. Above 0.5 V, III-V FinFET shows lower critical LET compared to Si FinFET due to the reduced w and enhanced charge collection. III-V FinFET outperforms Si FinFET due to the improved current drive below $0.5V_{DD}$.

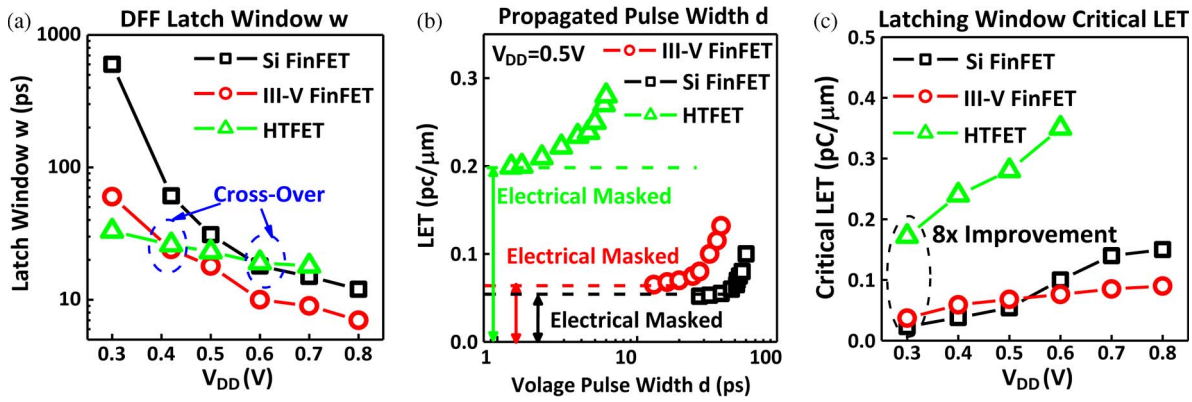

Fig. 19. (a) Latch window w and (b) voltage pulse width d characterization at 0.5 V for each device. HTFET shows reduced pulse width at the same radiation strength (LET) and higher threshold LET which can be electrical masked. (c) Latching window critical LET is extracted at $w = d$. HTFET shows 8 times critical LET improvement compared to Si FinFET at 0.3 V. III-V FinFET shows cross-over at 0.5 V due to reduced w/c.

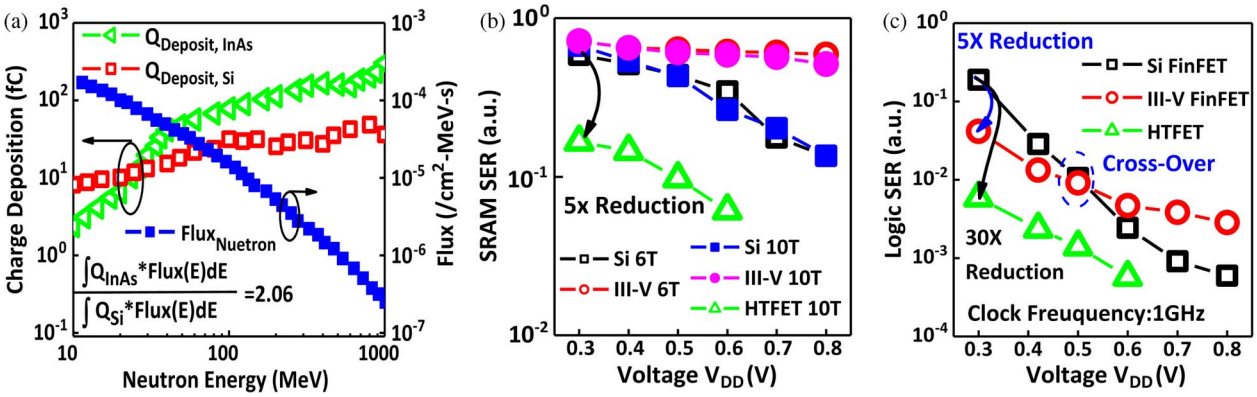

Fig. 20. (a) Monte Carlo simulation for neutron induced charge deposition on Si and InAs. InAs shows twice the charge deposition over the neutron spectrum [26] integration. (b) SRAM SER and (c) logic SER comparison with voltage scaling for Si, III-V FinFETs and HTFET. HTFET shows superior soft error resilience for both SRAM and logic. III-V FinFET logic shows lower SER below 0.5 V over Si FinFET logic.

V. SER Evaluation

A. Neutron Induced Charge Deposition

The neutron induced charge deposition is shown in Fig. 20(a) for InAs and Si. The evaluated sea-level neutron energy range is from 10MeV to 1000MeV (soft-error sensitive range) [35]. For each neutron energy step, 10000 strike events are simulated to obtain the average energy deposition and charge ionization. Based on the neutron spectrum integration, 2.06 times enhancement of charge deposition is observed for InAs compared to Si, which is applied to the following SER evaluation.

B. SRAM and Combinational Logic SER

Based on the critical LET and charge deposition analysis, the SRAM cell SER and logic SER are calculated based on (1) and (2) discussed in the Section III, respectively. Fig. 20(b) and (c) shows the relative SRAM SER and logic SER for Si FinFET, III-V FinFET and HTFET with the voltage scaling, respectively. HTFET shows superior soft-error resilience for voltage range from 0.3 V to 0.6 V for both SRAM and logic. 5 times reduction of SRAM cell SER and 30 times reduction of logic SER are obtained at 0.3V for HTFET compared to Si FinFET. This improvement is contributed from both the improved critical LET and latching window masking effect at low voltage because of steep switching. III-V FinFET shows different SER performance for SRAM cell and logic compared to Si FinFET. For SRAM cell, III-V FinFET SRAM shows overall high SER due to both the charge deposition and collection enhancement, but with a shallower slope with the voltage scaling than Si FinFET SRAM due to the drive current improvement at low V_{DD}. As shown in Fig. 20(c), III-V FinFET logic shows lower SER below 0.5 V compared to Si FinFET logic. The combinational logic SER relates to both the critical LET and the latching probability, w/c. At high V_{DD}, the critical LET and charge deposition enhancement dominates the logic SER, where the latching window is comparable for III-V and Si FinFET at high drive current. At low V_{DD}, the latching window increases significantly for Si FinFET at near-threshold operation, which increases the error latched probability as well as the logic SER.

VI. Conclusion

Sea-level radiation-induced soft error has been evaluated for Si FinFET, III-V (InAs) FinFET and III-V (GaSb as source/InAs as channel and drain) HTFET using device to circuit simulation. The device simulation shows that the asymmetrical source/drain doping induced ambipolar transport in HTFET greatly reduces the minority carrier storage in the channel,

which significantly reduces the bipolar gain effect and the charge collection as well as the transient duration. The III-V FinFET shows enhanced charge collection due to the mobility enhancement compared to Si FinFET. Based on the device simulation results, the SER based on critical LET extraction has been evaluated for SRAM cell and combinational logic, respectively, considering the charge deposition enhancement in III-V material with Geant4 simulation. Comparing Si and III-V FinFETs, III-V FinFET shows increased charge deposition due to lower ionization energy, which increases the SER for SRAM cells for all evaluated V_{DD}. The logic SER evaluation shows III-V FinFET has lower SER than Si FinFET below 0.5 V, which results from the reduced latching probability at low voltage due to the improved latching window masking effect. Compared to Si and III-V FinFETs, HTFET shows superior radiation resilience over both Si and III-V FinFET with the voltage range of 0.3 V to 0.6 V for both SRAM and logic. This fundamental advantage stems from the bipolar gain reduction, the on-state enhanced Miller capacitance effect and the improved latching window masking. The significant SER reduction at low supply voltage makes III-V HTFET a promising candidate for radiation resilient ultra-low power applications.

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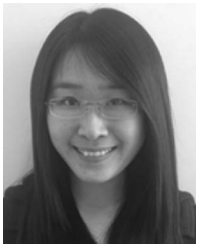

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