Heterojunction Intra-Band Tunnel FETs for Low-Voltage SRAMs

Sumeet Kumar Gupta, *Student Member, IEEE*, Jaydeep P. Kulkarni, *Member, IEEE*, Suman Datta, *Senior Member, IEEE*, and Kaushik Roy, *Fellow, IEEE*

***Abstract*—We propose heterojunction intra-band tunnel (HIBT) FETs based on different semiconductor materials (with matched lattice constants) for the source/drain (S/D) and channel. HIBT FETs have an energy band offset at the interface of the S/D and channel. As a result, carrier transport in the ON state occurs by intra-band tunneling. We analyze the device characteristics of HIBT FETs with Si S/D and GaP channel for different values of band offsets. We show that, due to intra-band tunneling, HIBT FETs exhibit lower ON current at iso-OFF current compared to Si double gate (DG) MOSFETs. However, the energy band offset at the S/D–channel interface leads to 40%–59% lower drain-induced barrier lowering/thinning and significantly reduced variation in OFF current across a range of supply voltages ($V_{\rm DD}$). Moreover, due to the heterovalent nature of S/D and channel materials, there is negligible dopant straggle in HIBT FETs, which further improves their process variation tolerance. We evaluate the impact of low OFF-current variations in HIBT FETs on 6T SRAM stability and leakage. Considering the worst case parameter variations at $V_{\rm DD} = 0.4$ V, HIBT-FET-based 6T SRAMs show 1.56X to 2.85X reduction in cell leakage, 1.28X to 1.58X increase in read static noise margin (SNM), 1.04X to 1.07X higher hold SNM, and 1.7X to 3X increase in write margin compared to Si-DG-MOSFET-based 6T SRAM. The enhancement of cell stability and reduction in cell leakage at low $V_{\rm DD}$ under process variations make HIBT FETs suitable for low-voltage SRAMs.**

***Index Terms*—Dopant straggle, double gate (DG) metal–oxide–semiconductor field-effect transistors (MOSFETs), heterojunction, low-voltage SRAM, process variations.**

I. Introduction

As METAL–OXIDE–SEMICONDUCTOR field-effect transistors (MOSFETs) continue to scale to achieve higher integration density, lower power, and higher performance, the effect of parameter variations on the device characteristics aggravates [1]. With countable dopant atoms in scaled bulk MOSFETs, random dopant fluctuation (RDF) has been shown to be the dominant component of parameter variations [2]. Furthermore, as bulk MOSFETs are scaled, short-channel effects worsen their performance as switches, leading to a large increase in leakage [3]. As an alternate to bulk MOSFETs, multigate FETs with ultrathin body (UTB) have emerged as potential devices for scaled technologies due to the following: 1) superior gate control of the channel and 2) elimination of RDF in the channel as a source of variation due to undoped UTB [4]–[7]. However, body thickness variation can be a problem in these devices [6].

The impact of parameter variations is further aggravated with supply voltage ($V_{\rm DD}$) scaling. It has been shown that the σ/μ (here, σ is the standard deviation, and μ is the mean) of different metrics like circuit delay and leakage increases at reduced $V_{\rm DD}$ [8]. Hence, for systems operated at scaled $V_{\rm DD}$, device and circuit design in scaled technologies becomes extremely challenging.

The adverse effect of parameter variations is particularly critical for circuits like SRAMs, in which mismatch between transistors can lead to cell failures. Conflicting requirements for stable read and write operations in 6T SRAMs further aggravate this issue.

In order to address the issues related to parameter variations in scaled technologies, techniques have been proposed at process [9], device [10], circuit [11], and architecture levels [8]. Since SRAMs show large susceptibility to process variations, the design of robust SRAMs to operate at the minimum possible supply voltage ($V_{\rm MIN}$) is an active area of research [12], [13]. The need for variation-tolerant design techniques assumes more importance for low-power low-throughput applications like implantable devices and sensor nodes, in which low $V_{\rm DD}$ operation and low leakage variations are critical to meet the power budget.

To that effect, we propose a heterojunction intra-band tunnel (HIBT) FET with near-dopant straggle-free characteristics and lower variation in OFF current compared to Si double gate (DG) MOSFETs. In addition, HIBT FETs show significant reduction in drain-induced barrier lowering/thinning (DIBL/T) at the cost of some degradation in the ON current at iso-subthreshold leakage. We analyze the impact of low OFF-current variations in HIBT FETs on the cell stability and leakage of 6T SRAMs and show the suitability of the proposed device for low-voltage SRAMs. The analysis in this paper is based on a simulation framework using non-equilibrium Green's function (NEGF)-based models [14] for devices.

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S. K. Gupta and K. Roy are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA (e-mail: guptask@purdue.edu; kaushik@purdue.edu).

J. P. Kulkarni was with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA. He is now with Intel Corporation, Hillsboro, OR 97124 USA (e-mail: jaydeep.p.kulkarni@intel.com).

S. Datta is with the Department of Electrical Engineering, The Pennsylvania State University, University Park, PA 16802 USA (e-mail: sdatta@engr.psu.edu).

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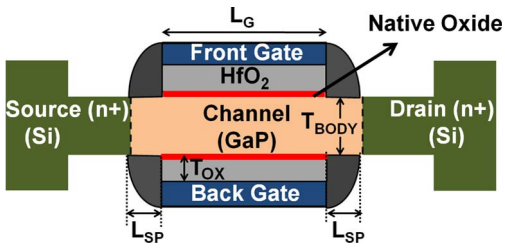

Fig. 1. Device structure of the proposed Si–GaP HIBT FET.

The contributions of this work are summarized as follows.

1) We propose an HIBT FET based on different semiconductor materials (with matched lattice constants) for the source/drain (S/D) and channel.
2) We perform a detailed device analysis and evaluate the benefits and tradeoffs associated with HIBT FETs with Si S/D and GaP channel. The analysis is performed for different values of band offsets introduced at the heterojunction. We show improvement in DIBL/T and output conductance in HIBT FETs compared to those in Si DG MOSFETs. We also describe the near-dopant straggle-free aspect of HIBT FETs.
3) We analyze the sensitivity of ON and OFF currents with respect to variations in different parameters. Our analysis shows lower OFF-current variations in HIBT FETs compared to those in Si DG MOSFETs.
4) We explore the application of HIBT FETs in low-voltage SRAMs. Our simulations show that HIBT-FET-based 6T SRAMs exhibit higher cell stability and lower leakage at low $V_{\rm DD}$ under process variations.

The rest of this paper is organized as follows. Section II introduces the device structure and describes the impact of heterojunction on the current–voltage characteristics. In Section III, we perform the sensitivity analysis of HIBT FETs with respect to different device parameters. Section IV analyzes HIBT-FET-based 6T SRAMs from the point of view of cell stability and leakage across a range of $V_{\rm DD}$ under process variations. Section V concludes this paper.

II. Device Structure and Characteristics

A. Device Structure

Fig. 1 shows the structure of the proposed HIBT FET. Different semiconductor materials are used for the S/D and channel so that a heterojunction is formed. Two requirements for S/D and channel materials are as follows: 1) matched lattice constants and 2) a positive conduction band offset (CBO) from the S/D to channel for an n-type device (Fig. 2). One of the material pairs which meet the requirements for n-type HIBT FETs is Si–GaP, in which the lattice mismatch is less than 0.4% [15], [16]. With a Si S/D and GaP channel, CBO $\sim$ 0.1–0.35 eV is introduced at the interface of the S/D and channel. We perform a subsequent analysis for n-type Si–GaP HIBT FETs for three values of CBO: 0.1, 0.25, and 0.35 eV. The first and the last values are deduced from energy bandgaps of Si and GaP and the valence band offsets (VBOs) observed experimentally in [17] and [18]. The second value has been predicted using theoretical calculations in [19]. In order to

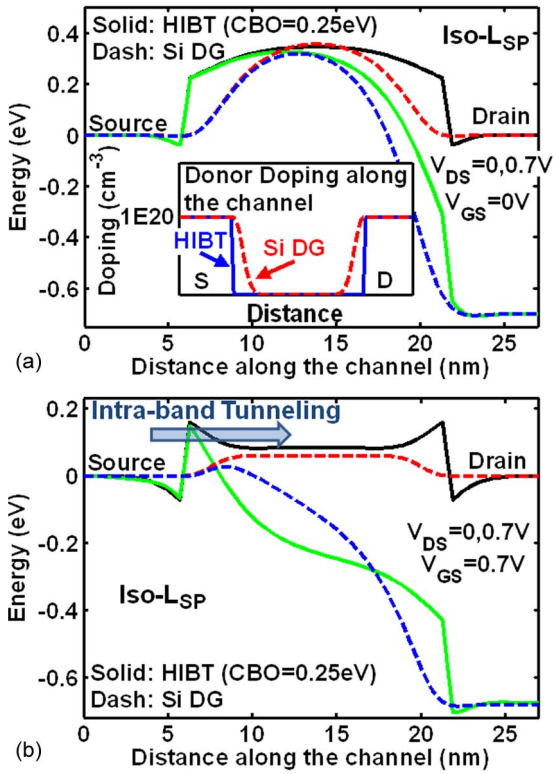

Fig. 2. Conduction band profiles of HIBT FET and Si DG MOSFET at $V_{\rm GS}$ = (a) 0 and (b) 0.7 V showing CBO and intra-band tunneling barrier in HIBT FET. Inset shows abrupt S/D junction in HIBT FET.

fabricate Si–GaP HIBT FETs, vertical growth of Si source, GaP channel, and Si drain is required, similar to [20] and [21].

Another set of lattice-matched materials suitable for n-type HIBT FETs can be Ge–GaAs (CBO = 0.23 eV [22]). Suitable materials with unmatched lattice constants may also be used in HIBT FETs. However, the analysis of such devices would require detailed calculations of strain effects. Hence, to illustrate the device concept, we limit our discussion and analysis to materials with matched lattice constants. We specifically consider the Si–GaP material pair and analyze the benefits and tradeoffs associated with HIBT FETs.

Note that the Si–GaP material pair is not suitable for p-type HIBT FETs because of unacceptably large VBOs [17]–[19]. A material pair that can be potentially useful for p-type HIBT FETs is Si–GaAs (VBO = -0.14 eV [23]). However, since this material pair has a lattice mismatch of $\sim$4% [23], strain effects need to be considered in the evaluation of the p-type Si–GaAs device. As mentioned earlier, this paper focuses on n-type Si–GaP HIBT FETs to explain the proposed device idea and to compare HIBT FETs with Si DG homojunction MOSFETs. The devices are evaluated using NEGF [14]-based simulation framework, which we will briefly discuss next.

B. Simulation Framework and Device Design

HIBT FETs and Si DG MOSFETs are modeled using NEGF-based formalism [14]. Ballistic NEGF equations are solved self-consistently with 2-D Poisson's equation to obtain the device characteristics, taking into account the quantum effects. Devices are designed with gate length = 10.8 nm. HfO_2 +

TABLE I
DEVICE PARAMETERS FOR HIBT FET AND HOMOJUNCTION Si DG MOSFET

Channel Material	HIBT Si DG	GaP Si
Source/Drain Material		Si
Lattice Constant	GaP Si	5.45 A 5.43 A
Band Gap	GaP Si	2.26eV 1.12eV
Gate Dielectric (Dielectric Constant)	HIBT Si DG	HfO_2(26)+Ga_2O_3/$GaPO_4$(7.5) HfO_2(26)+SiO_2(3.9)
Physical Gate Length (L_G)		10.8nm
Body Thickness (T_{BODY})		4.5nm
Physical Oxide Thickness (T_{OX})		2.4nm
Effective Oxide Thickness (EOT)	HIBT Si DG	0.471nm 0.615nm
Spacer Thickness (L_{SP})		2.4nm (Si DG and HIBT) 0.9nm (HIBT iso-L_{CH})
Body Doping		Intrinsic
Source/Drain Doping		$10^{20}cm^{-3}$
Dopant Straggle (σ_{DOP})		1.5nm/decade

native oxide of the channel (SiO_2 for Si DG MOSFETs and $Ga_2O_3/GaPO_4$ [24] for Si–GaP HIBT FETs) is used as the gate dielectric stack with a physical oxide thickness $(T_{\rm OX})$ of 2.4 nm. A higher dielectric constant of $Ga_2O_3/GaPO_4$ compared to SiO_2 [25], [26] leads to a lower effective oxide thickness (EOT) in HIBT FETs (0.471 nm) compared to that in Si DG MOSFETs (0.615 nm). A body thickness $(T_{\rm BODY})$ of 4.5 nm is used. Gaussian profile is assumed for the dopant straggle into the channel with a straggle value of 1.5 nm/decade. The devices are designed with an S/D doping equal to 10^{20} cm^{-3} and intrinsic channel. Gate workfunction (Φ_G) for the devices is chosen to obtain the transistor threshold voltage $(V_{\rm TH}) \sim 0.3$ V.

As we will discuss in the next subsection, HIBT FETs exhibit negligible dopant straggle. This leads to a larger effective channel length $(L_{\rm CH})$ in HIBT FETs compared to that in Si DG MOSFETs. Hence, for comprehensive evaluation of the advantages and disadvantages of HIBT FETs, the comparison of HIBT FETs and Si DG MOSFETs is performed at the following: 1) iso-spacer length $(L_{\rm SP})$, i.e., with identical device footprint, and 2) iso-$L_{\rm CH}$. For the former case, $L_{\rm SP} = 2.4$ nm is used for HIBT FETs and Si DG MOSFETs leading to larger $L_{\rm CH}$ and gate underlap in HIBT FETs. For the latter case, $L_{\rm SP}$ is reduced to 0.9 nm for HIBT FETs to obtain $L_{\rm CH}$ and gate underlap equal to those of Si DG MOSFETs. Table I summarizes the device parameters used in this work.

C. Near-Dopant Straggle-Free Characteristics of Si–GaP HIBT FETs

Heterovalent materials in the S/D and channel (i.e., group IV S/D and III–V channel materials) result in an interesting property of Si–GaP HIBT FETs. Si S/D regions are doped n-type with phosphorous (P) atoms. However, when P atoms diffuse into the channel, they do *not* act as dopants for the GaP channel. As a result, the effective channel length and the device characteristics of HIBT FETs become insensitive to the straggle of P atoms. Note that there is a possibility of cross-doping of GaP with Si [27] which results in n-type doping in GaP [28]. However, the dopant concentration of Si in GaP is small [27]–[29] and therefore has negligible effect on the device characteristics (as shown later). We assume peak cross-doping of 10^{18} cm^{-3} [28], [29] with a Gaussian dopant straggle of 1.5 nm/decade. (We have confirmed, from our simulations, that the device characteristics are fairly insensitive to the dopant straggle because of low peak doping. Hence, other values of dopant straggle will not change the trends that we present later.) Thus, HIBT FETs exhibit near-dopant straggle-free characteristics due to the following: 1) heterovalent S/D and channel materials and 2) low cross-doping. The inset of Fig. 2 compares the doping profile of HIBT FETs and Si DG MOSFETs showing near-abrupt S/D junctions in HIBT FETs.

Other important attributes of HIBT FETs are the following: 1) symmetric device structure with equal bidirectional drain current (unlike band-to-band tunnel (BTBT) FETs [30]) and 2) absence of ambipolar conduction [30], [31] due to the large bandgap of Si S/D (unlike BTBT FETs and Schottky barrier FETs with low-bandgap channel material [31]). Note that, due to the absence of ambipolar conduction in HIBT FETs, suitable material pairs with low-bandgap channel materials and high-bandgap S/D materials can also explored.

With the understanding of the device structure, we now present a quantitative analysis of the device characteristics of HIBT FETs.

D. Device Characteristics

Positive CBO from the S/D to the channel of HIBT FETs results in higher OFF-state energy barrier compared to Si DG MOSFETs and, therefore, lower subthreshold current $(I_{\rm SUB})$. We perform comparison of HIBT FETs and Si DG MOSFETs under iso-$I_{\rm SUB}$ conditions. In order to achieve equal $I_{\rm SUB}$ at $V_{\rm DD} = 0.7$ V, a lower gate workfunction (Φ_G) is used for HIBT FETs so that the devices have a similar OFF-state energy barrier [Fig. 2(a)]. It can be observed from Fig. 2(a) that, at gate voltage $(V_{\rm GS}) = 0$ V, carrier transport in HIBT FETs occurs by thermal injection of the carriers over the source barrier. However, in the ON state, the dominant mechanism of carrier transport is intra-band tunneling [Fig. 2(b)]. As a result, the ON current $(I_{\rm ON})$ degrades in HIBT FETs. Figs. 3 and 4 and Table II show that $I_{\rm ON}$ degradation is higher for larger CBO due to increase in the tunneling barrier. For CBO $= 0.1$ eV, $I_{\rm ON}$ for HIBT FETs is comparable to that of Si DG MOSFETs at iso-$L_{\rm CH}$ in spite of intra-band tunneling. This is due to lower EOT in HIBT FETs (see Section II-B). $I_{\rm ON}$ at iso-$L_{\rm CH}$ is higher than that at iso-$L_{\rm SP}$ due to lower effective channel length and lower gate underlap. (Note that larger gate underlap at iso-$L_{\rm SP}$ leads to weaker modulation of the intra-band tunneling barrier by the gate voltage, which degrades $I_{\rm ON}$).

Abrupt discontinuity in the potential energy due to CBO at the S/D–channel heterojunction results in reduced effect of drain electric fields on the drain current (I_D). Therefore, HIBT FETs exhibit lower DIBL/T compared to Si DG MOSFETs, as can be observed in Figs. 3 and 4 and Table II. The reduced differential of I_D with respect to drain voltage $(V_{\rm DS})$ is also evident in the output characteristics of HIBT FETs showing

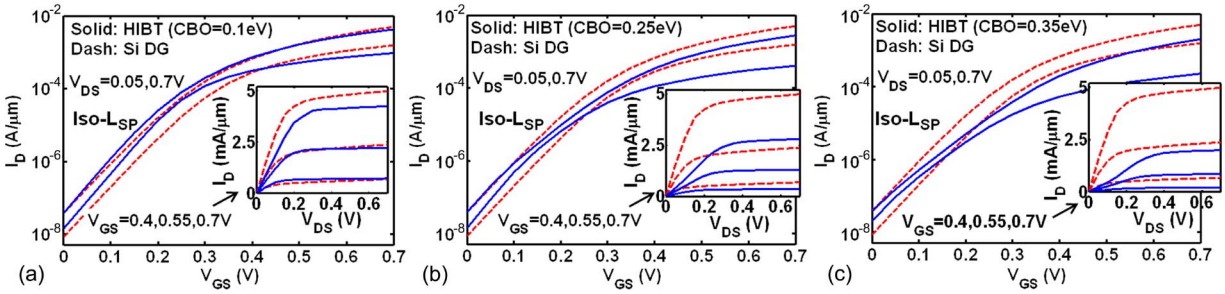

Fig. 3. I_D–$V_{\rm GS}$ and I_D–$V_{\rm DS}$ characteristics of Si DG MOSFET and HIBT FETs with CBO = (a) 0.1, (b) 0.25, and (c) 0.35 eV at iso-$L_{\rm SP}$.

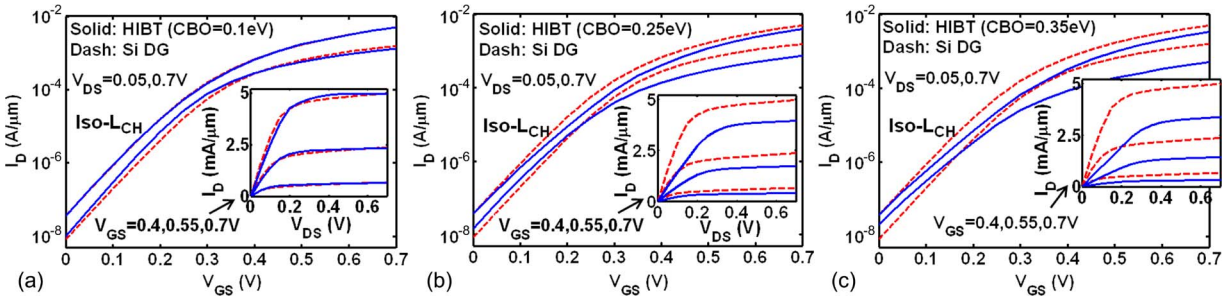

Fig. 4. I_D–$V_{\rm GS}$ and I_D–$V_{\rm DS}$ characteristics of Si DG MOSFET and HIBT FETs with CBO = (a) 0.1, (b) 0.25, and (c) 0.35 eV at iso-$L_{\rm CH}$.

TABLE II
DEVICE METRICS FOR HIBT FETS AT $V_{\rm DD} = 0.7$ V NORMALIZED TO THE RESPECTIVE METRICS FOR Si DG MOSFET

	Iso-L_{SP}			Iso-L_{CH}		
CBO (eV) ➡	0.1	0.25	0.35	0.1	0.25	0.35
I_{ON}	0.85X	0.56X	0.4X	1X	0.8X	0.68X
I_{SUB}	1X	1X	1X	1X	1X	1X
I_{GOFF}	0.55X	1.1X	2.14X	1.29X	2.93X	6.49X
$I_{OFF} = I_{SUB} + I_{GOFF}$	1X	1X	1X	1X	1X	1X
I_{GON}	2.1X	6.5X	18X	1.7X	6.1X	16.7X
I_{LEAK} =0.5*(I_{GON} + I_{SUB})	1.02X	1.07X	1.15X	1X	1.02X	1.14X
DIBL/T	0.6X	0.52X	0.41X	0.76X	0.56X	0.5X
SS	0.91X	1.1X	1.25X	0.99X	1.1X	1.16X
g_m	0.76X	0.58X	0.46X	0.97X	0.86X	0.77X
g_{DS}	0.51X	0.46X	0.38X	0.68X	0.66X	0.72X
R_{ON}	1.35X	2.88X	5.16X	1.06X	1.79X	2.59X
I_{DEFF}	0.92X	0.55X	0.37X	1.03X	0.76X	0.62X

lower output conductance $(g_{\rm DS})$ in the saturation region. However, at the same time, CBO leads to reduced differential of I_D with respect to $V_{\rm GS}$ as well. This results in the following: 1) higher subthreshold swing (SS), 2) lower $I_{\rm ON}-I_{\rm SUB}$ ratio, and 3) lower transconductance (g_m). A higher resistance in the linear region $(R_{\rm ON})$ is also observed in HIBT FETs. This is due to the tunneling barriers at the S/D–channel interfaces.

It can be observed in Table II that $g_{\rm DS}$ (at iso-$L_{\rm SP}$) and DIBL/T decrease with increasing CBO, which explains the role of heterojunction in improving DIBL/T and $g_{\rm DS}$. However, at iso-$L_{\rm CH}$, an increase in $g_{\rm DS}$ is observed as CBO is increased from 0.25 to 0.35 eV. This is explained as follows. While higher CBO on the source side tends to decrease the sensitivity of I_D to $V_{\rm DS}$, higher CBO on the drain side tends to have an opposite effect. This is because the band profile and electric field in the channel are also controlled by the drain CBO and $V_{\rm DS}$ [see Fig. 2(b)]. For higher drain CBO and lower $L_{\rm CH}$ (iso-$L_{\rm CH}$), the effect of $V_{\rm DS}$ on channel electrostatics increases. Hence, an increase in $g_{\rm DS}$ with increasing CBO may occur if the effect of drain CBO is more dominant than that of source CBO. However, in most cases, in Table II, the effect of source CBO dominates. As a result, DIBL/T and $g_{\rm DS}$ decrease with increasing CBO. Note that a lower EOT in HIBT FETs also contributes to lower short-channel effects. However, the role of CBO in improving DIBL/T and $g_{\rm DS}$ is significant, as is evident from the trends for different CBOs in Table II. Table II also show that g_m, SS, and $R_{\rm ON}$ degrade with increasing CBO.

Comparison of the iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$ cases shows improved DIBL/T and $g_{\rm DS}$ for devices with a larger channel length (iso-$L_{\rm SP}$) due to lower short-channel effects. However, at the same time, a lower g_m is observed at iso-$L_{\rm SP}$. This is due to larger gate underlap and weaker modulation of the intra-band tunnel barrier with gate voltage. $R_{\rm ON}$ at iso-$L_{\rm SP}$ is higher than that at iso-$L_{\rm CH}$ due to larger channel length. SS for the device with a larger channel length (iso-$L_{\rm SP}$) is lower compared to that at iso-$L_{\rm CH}$ for CBO = 0.1 eV. This is because of lower short-channel effects at iso-$L_{\rm SP}$. However, for large CBO, SS is higher at iso-$L_{\rm SP}$. This is because, when CBO is large, the current at low $V_{\rm GS}$ (which determines SS) may be due to intra-band tunneling. Hence, due to reduced sensitivity of the tunnel barrier to $V_{\rm GS}$ at iso-$L_{\rm SP}$, SS degrades. (Also, note that SS is not constant for HIBT FETs. This is due to the fact that, as $V_{\rm GS}$ increases, subthreshold current transport changes from thermal injection of the carriers to intra-band tunneling).

We also compare the effective drain current (I_{DEFF}) defined as the average of I_D at $(V_{\rm GS}, V_{\rm DS}) = (V_{\rm DD}, V_{\rm DD}/2)$,

$(V_{\rm GS}, V_{\rm DS}) = (V_{\rm DD}/2, V_{\rm DD})$, and $(V_{\rm GS}, V_{\rm DS}) = (3V_{\rm DD}/4, 3V_{\rm DD}/4)$ [32]. I_{DEFF} is a measure of the circuit delay. It can be observed from Table II that, for low CBO, I_{DEFF} degradation is lower than that of $I_{\rm ON}$ at iso-$L_{\rm SP}$. This is because of the lower $g_{\rm DS}$ and similar saturation voltage (V_{DSAT}) of HIBT FETs compared to those of Si DG MOSFETs. For the same reason, I_{DEFF} at iso-$L_{\rm CH}$ is improved for HIBT FETs for CBO $= 0.1$ eV. However, for high CBO, degradation in I_{DEFF} is larger than that in $I_{\rm ON}$. This is because, at high CBO, HIBT FETs have a higher V_{DSAT} compared to Si DG MOSFETs (see Figs. 3 and 4). As a result, I_D at $(V_{\rm GS}, V_{\rm DS}) = (V_{\rm DD}, V_{\rm DD}/2)$ is lower in HIBT FETs which reduces I_{DEFF}.

Gate current (I_G) comparison of HIBT and Si DG FETs is also shown in Table II. We define I_{GON} as I_G at $V_{\rm GS} = V_{\rm DD}$ and $V_{\rm DS} = 0$ and I_{GOFF} as I_G at $V_{\rm GS} = 0$ and $V_{\rm DS} = V_{\rm DD}$. It can be observed that I_{GON} is higher for HIBT FETs compared to Si DG MOSFETs. This is because, in the ON state, direct tunneling current $(I_{\rm DT})$ is the dominant component of I_G due to high carrier concentration in the channel. Devices with a lower gate workfunction (Φ_G) and lower tunnel barrier at the interface of the channel and gate dielectric exhibit higher $I_{\rm DT}$. Note that HIBT FETs have lower gate tunneling barriers due to CBO and lower Φ_G compared to Si DG MOSFETs. (Recall that lower Φ_G is used in HIBT FETs to achieve iso-$I_{\rm SUB}$ conditions.) As a result, I_{GON} is higher in HIBT FETs, and it increases with increasing CBO. Also, I_{GON} at iso-$L_{\rm SP}$ is higher compared to that at iso-$L_{\rm CH}$ because of lower Φ_G used in the former case.

The comparison of I_{GOFF} in Table II shows that HIBT FETs may exhibit higher or lower I_{GOFF} compared to Si DG MOSFETs depending on the value of CBO. This is explained as follows. For $V_{\rm GS}$ less than the transistor threshold voltage $(V_{\rm TH})$, edge tunneling current $(I_{\rm ET})$ dominates. At iso-$L_{\rm SP}$, the near-dopant straggle-free nature of HIBT FETs leads to larger gate underlap compared to Si DG MOSFETs. This tends to decrease $I_{\rm ET}$. However, lower gate tunneling barriers in HIBT FETs compared to Si DG MOSFETs (as discussed earlier) tend to increase $I_{\rm ET}$. Hence, for low CBO, HIBT FETs have a lower $I_{\rm ET}$ compared to Si DG MOSFETs due to larger gate underlap. However, for large CBO, gate tunneling barriers are relatively low, which increases $I_{\rm ET}$. At iso-$L_{\rm CH}$, gate underlap is comparable to that of Si DG MOSFETs. As a result, the effect of lower gate tunneling barriers in HIBT FETs is more dominant, leading to higher I_{GOFF} for all CBOs.

Table II also show that, in spite of a large increase in I_G in HIBT FETs, OFF current $(I_{\rm OFF} = I_{\rm SUB} + I_{GOFF})$ is similar. Also, the average leakage current (i.e., the average over the ON- and OFF-state leakage) $I_{\rm LEAK} = 0.5 * (I_{GON} + I_{\rm OFF})$ is comparable or only mildly increased. This is because high-k dielectric (HfO_2—Fig. 1) limits I_G and makes $I_{\rm SUB}$ the dominant component of the total leakage.

Lower $I_{\rm ON}$ and I_{DEFF} in HIBT FETs (for certain values of CBO) compared to Si DG MOSFETs limits the application of HIBT FETs to low-throughput systems like implantable devices and sensor nodes. Such systems are typically operated at low $V_{\rm DD}$ to save power. Hence, in addition to standard voltage $(V_{\rm DD} = 0.7$ V), subsequent analysis of HIBT FETs will be performed at low $V_{\rm DD} (= 0.4$ V) as well. In the later sections, we will show the potential of HIBT FETs in low-voltage SRAMs. Note that, since the target applications for HIBT FETs are low-voltage systems, higher gate leakage in HIBT FETs becomes less critical. This is because the contribution of gate leakage to the total leakage decreases at low $V_{\rm DD}$.

TABLE III
DEVICE METRICS FOR HIBT FETs AT $V_{\rm DD} = 0.4$ V NORMALIZED TO THE RESPECTIVE METRICS FOR Si DG MOSFET

	Iso-L_{SP}			Iso-L_{CH}		
CBO (eV) ➡	0.1	0.25	0.35	0.1	0.25	0.35
I_{ON}	1.2X	0.57X	0.32X	1X	0.65X	0.5X
I_{SUB}	1.2X	1.3X	1.43X	1.12X	1.27X	1.41X
I_{GOFF}	0.5X	0.69X	1.09X	1.15X	1.99X	3.49X
$I_{OFF} = I_{SUB} + I_{GOFF}$	1.2X	1.3X	1.43X	1.12X	1.27X	1.41X
I_{GON}	1.4X	4.5X	10.8X	1.84X	5X	10.7X
I_{LEAK} =0.5*(I_{GON} + I_{SUB})	1.2X	1.3X	1.44X	1.12X	1.28X	1.42X
DIBL/T	0.52X	0.49X	0.41X	0.69X	0.54X	0.48X
SS	0.91X	1.05X	1.24X	0.98X	1.09X	1.18X
g_m	1.09X	0.57X	0.34X	1.04X	0.67X	0.55X
g_{DS}	0.42X	0.23X	0.15X	0.72X	0.42X	0.37X
R_{ON}	0.9X	2.5X	5.4X	1X	2X	3.3X
I_{DEFF}	1.4X	0.62X	0.32X	1.1X	0.67X	0.5X

Table III shows the comparison of HIBT FETs and Si DG MOSFETs at $V_{\rm DD} = 0.4$ V. The trends for different device metrics can be understood following the discussion that we presented in this section for $V_{\rm DD} = 0.7$ V. Note that $I_{\rm SUB}$ is higher for HIBT FETs compared to Si DG MOSFETs at $V_{\rm DD} = 0.4$ V due to lower DIBL/T. However, if one wants to optimize the devices for low-voltage operation, it is always possible to design the gate workfunction to achieve equal $I_{\rm SUB}$ at $V_{\rm DD} = 0.4$ V. In this paper, the device comparisons are performed at iso-subthreshold leakage at $V_{\rm DD} = 0.7$ V to explore the design space across the entire range of $V_{\rm DD}$. It may also be mentioned that at $V_{\rm DD} = 0.4$ V, the contribution of intra-band tunneling current to $I_{\rm ON}$ decreases and that due to thermal injection of carriers increases. This relative decrease in intra-band tunneling current is more significant for low CBO. Hence, (unlike the trends at $V_{\rm DD} = 0.7$ V), g_m at iso-$L_{\rm SP}$ is larger than that at iso-$L_{\rm CH}$ for CBO$= 0.1$ eV as a result of lower Φ_G in the former device. For the same reason, $I_{\rm ON}$ at iso-$L_{\rm SP}$ is larger than that at iso-$L_{\rm CH}$ for CBO $= 0.1$eV (Table III). Another point to note is that at $V_{\rm DD} = 0.4$ V, the contributions of $I_{\rm DT}$ and $I_{\rm ET}$ to I_{GON} become comparable. This is due to lower carrier concentration in the channel compared to that at $V_{\rm DD} = 0.4$ V. Hence, the comparison of iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$ for I_{GON} shows different trends for $V_{\rm DD} = 0.4$ V and can be understood from the discussion on $I_{\rm ET}$ and $I_{\rm DT}$ presented before.

To sum up, HIBT FETs show lower $I_{\rm ON}$ at iso-$I_{\rm SUB}$ due to intra-band tunneling and higher I_{GON} due to lower gate tunneling barriers. CBO in HIBT FETs results in reduced

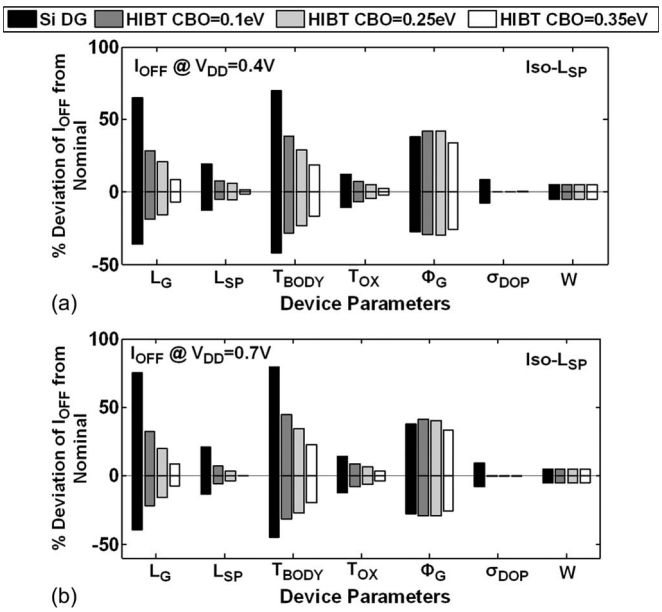

Fig. 5. Variation of $I_{\rm OFF}$ with respect to different device parameters for HIBT FETs and Si DG MOSFET at iso-$L_{\rm SP}$ at (a) $V_{\rm DD} = 0.4$ V and (b) $V_{\rm DD} = 0.7$ V. The range of variation in $\Phi_G = \pm 10$ mV. The range of variation in other device parameters is $\sim \pm 5\%$ of the nominal value.

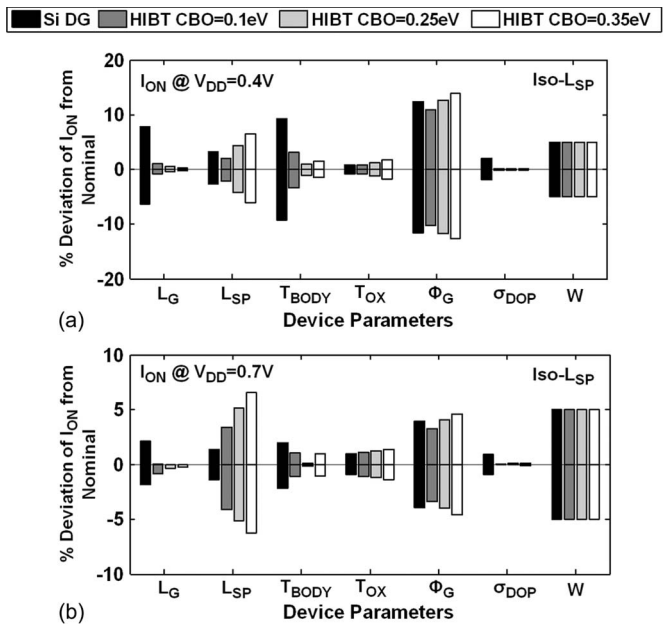

Fig. 6. Variation of $I_{\rm ON}$ with respect to different device parameters for HIBT FETs and Si DG MOSFET at iso-$L_{\rm SP}$ at (a) $V_{\rm DD} = 0.4$ V and (b) $V_{\rm DD} = 0.7$ V. The range of variation in $\Phi_G = \pm 10$ mV. The range of variation in other device parameters is $\sim \pm 5\%$ of the nominal value.

differential of I_D to $V_{\rm GS}$ and $V_{\rm DS}$ leading to higher SS, lower g_m, lower DIBL/T, and lower $g_{\rm DS}$.

The analysis in this section illustrates the role of CBO in reducing the impact of drain and gate biases on I_D. This suggests a possible reduction in the sensitivity of I_D to variations in device parameters due to CBO. In the next section, we perform sensitivity analysis of HIBT FETs and evaluate the effect of CBO on the variations in $I_{\rm OFF}$ and $I_{\rm ON}$.

III. Sensitivity to Parameter Variations

Sensitivity analysis for HIBT FETs and Si DG MOSFETs is performed by varying the device parameters, viz., body thickness ($T_{\rm BODY}$), gate dielectric thickness ($T_{\rm OX}$), spacer length ($L_{\rm SP}$), gate length (L_G), dopant straggle depth ($\sigma_{\rm DOP}$), and device width (W), by $\sim \pm 5\%$ around the nominal values. Gate workfunction (Φ_G) is varied by ± 10 mV around the nominal values. (Note that, at iso-$L_{\rm CH}$, variation in $L_{\rm SP}$ in HIBT FETs is $\sim \pm 17\%$ because of lower nominal value compared to Si DG MOSFET.) The impact of parameter variations on $I_{\rm ON}$ and $I_{\rm OFF}$ is analyzed at $V_{\rm DD} = 0.4$ V and $V_{\rm DD} = 0.7$ V.

Figs. 5 and 6 show the sensitivity of $I_{\rm ON}$ and $I_{\rm OFF}$ with respect to individual parameters at iso-$L_{\rm SP}$. The trends at iso-$L_{\rm CH}$ are similar and are not shown to avoid repetition. However, later, we will discuss the joint effect of all parameters on $I_{\rm ON}$ and $I_{\rm OFF}$ at iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$. It can be observed in Fig. 5 that the sensitivity (S) of $I_{\rm OFF}$ with respect to $T_{\rm BODY}$, $T_{\rm OX}$, $L_{\rm SP}$, and L_G is significantly lower for HIBT FETs compared to that for Si DG MOSFETs. This is attributed to CBO at the S/D–channel interfaces which reduces the impact of parameter variations. Decreasing sensitivity with increasing CBO shows the role played by the heterojunction in lowering the OFF-current variations. Due to near-abrupt S/D junctions in HIBT FETs (see Section II-C), S with respect to dopant straggle depth is negligible. S due to W is comparable for HIBT FETs and Si DG MOSFETs. On the other hand, S due to Φ_G is slightly higher in HIBT FETs compared to that in Si DG MOSFETs. However, the maximum increase in the variability is only 9% for a variation in Φ_G of ± 10 mV. Note that S due to Φ_G is related to SS at $V_{\rm GS} = 0$ V, since the changes in $V_{\rm GS}$ and Φ_G have a similar effect on the drain current. It can be observed from Fig. 3 that HIBT FETs (CBO $= 0.1$ and 0.25 eV) have a slightly lower SS compared to Si DG MOSFETs at $V_{\rm GS} = 0$, which leads to a marginally higher sensitivity due to Φ_G. However, SS averaged over a range of $V_{\rm GS}$ (shown in Tables II and III) is higher for HIBT FETs, as discussed before. It may also be mentioned that, in addition to the variation in Φ_G, the variations in device dimensions, particularly $T_{\rm BODY}$, are critical for highly scaled devices. As discussed before, a significantly large reduction in the sensitivity of $I_{\rm OFF}$ with respect to other parameters is observed in HIBT FETs (Fig. 5). For instance, HIBT FETs show 40%–69% reduction in S for $\pm 5\%$ variability in $T_{\rm BODY}$ compared to Si DG MOSFETs. Also (as we will show later), considering variations in all the device parameters, $I_{\rm OFF}$ in HIBT FETs shows a significant resilience to process variations.

The analysis of $I_{\rm ON}$ (Fig. 6) shows reduced S for HIBT FETs with respect to $T_{\rm BODY}$ and L_G due to CBO. S with respect to dopant straggle depth is negligible, and that with respect to Φ_G and W is comparable. However, S for $I_{\rm ON}$ of HIBT FETs is large with respect to $T_{\rm OX}$ and $L_{\rm SP}$. This is because the tunneling barrier width is significantly affected by the change in $T_{\rm OX}$ and $L_{\rm SP}$, resulting in a large variation in the intra-band tunneling current. Note that, at $V_{\rm DD} = 0.4$ V, S with respect to $L_{\rm SP}$ decreases for CBO $= 0.1$ eV. This is because, at low $V_{\rm DD}$, the current contribution due to intra-band tunneling is reduced for low CBO and the chief transport mechanism is thermal injection of the carriers.

It can also be observed from Fig. 6 that S with respect to L_G decreases with increasing CBO. On the other hand, $I_{\rm ON}$ variations due to $T_{\rm OX}$ and $L_{\rm SP}$ increase for a higher CBO due to the increase in the intra-band tunneling barrier. S with respect to Φ_G is higher for a higher CBO because the nominal value of the current is lower. This increases the relative deviation of $I_{\rm ON}$. One trend that requires a more detailed explanation is the non-monotonic change in $I_{\rm ON}$ variations due to $T_{\rm BODY}$ with increasing CBO. The explanation is as follows. The change in current due to variation in $T_{\rm BODY}$ can be attributed to two main factors: 1) The effect of drain electric fields on the source barrier decreases with decreasing $T_{\rm BODY}$, and 2) quantum confinement effects in the source lead to a larger energy gap between the subbands for a lower $T_{\rm BODY}$. The former effect tends to lower the current, while the latter effect tends to increase the current for lower subbands. The explanation is as follows. Due to the larger energy gap between subbands for lower $T_{\rm BODY}$, the relative contribution of the lowest subband to the total charge density increases. In order to maintain the charge equilibrium in the source and drain regions, the Fermi level is at a higher energy relative to the lowest subband. Hence, as $T_{\rm BODY}$ decreases, the current component due to the lower subbands tends to increase. On the other hand, the current due to higher subbands decreases due to larger energy splitting between the subbands. However, since lower subbands are major contributors to the current, quantum confinement in the source tends to increase the current as $T_{\rm BODY}$ decreases. The overall effect of decreasing $T_{\rm BODY}$ depends on the relative impact of the drain electric field and the quantum confinement effects in the source. For lower CBO, the impact of drain electric field is larger (as discussed earlier); hence, current decreases with decreasing $T_{\rm BODY}$. For higher CBO, the impact of drain electric field is less, due to which current increases as $T_{\rm BODY}$ decreases. In other words, the slope of $I_{\rm ON}$ with $T_{\rm BODY}$ is positive for lower CBO, becomes close to zero as CBO increases, and then becomes negative. Hence, the sensitivity (which is related to the absolute value of the slope) shows a non-monotonic behavior.

Next, we perform an analysis of the joint effect of variations in all the parameters on the device characteristics. The analysis is performed at iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$. As can be observed in Fig. 7, HIBT FETs show a significant reduction in $I_{\rm OFF}$ variations at $V_{\rm DD} = 0.4$ and 0.7 V compared to Si DG MOSFETs at both iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$. Variations in $I_{\rm OFF}$ decrease with increasing CBO. Also, note that variations in $I_{\rm OFF}$ are lower at iso-$L_{\rm SP}$ due to lower short-channel effects compared to those at iso-$L_{\rm CH}$. In addition to reduced $I_{\rm OFF}$ variations, lower $I_{\rm ON}$ variations at $V_{\rm DD} = 0.4$ V are observed in HIBT FETs. At $V_{\rm DD} = 0.7$ V, $I_{\rm ON}$ variations are lower at iso-$L_{\rm CH}$ for HIBT FETs. However, at iso-$L_{\rm SP}$, variations are comparable, particularly for higher CBO. This is because, at iso-$L_{\rm SP}$, larger gate underlap makes the intra-band tunnel barrier more sensitive to the variations in $L_{\rm SP}$. For higher CBO, this effect is more significant (as also observed in Fig. 6), which tends to increase $I_{\rm ON}$ variations. However, lower $I_{\rm ON}$ variations due to other parameters compensate for this effect. The net effect is comparable $I_{\rm ON}$ variations for CBO $= 0.35$ eV.

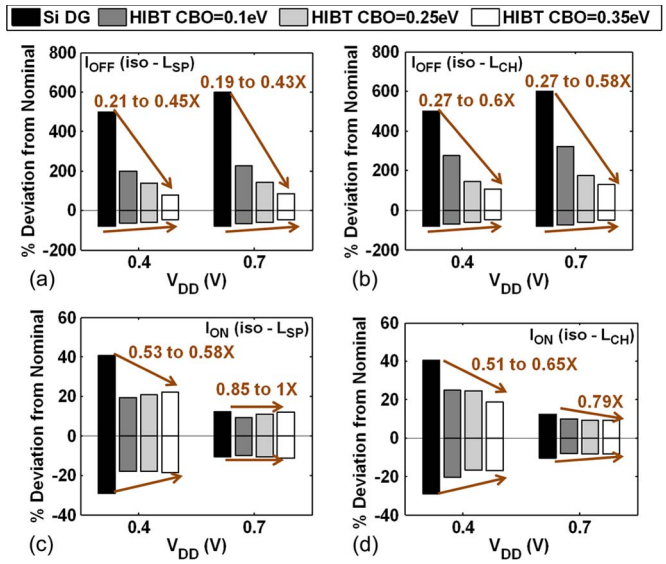

Fig. 7. Variations in (a) and (b) $I_{\rm OFF}$ and (c) and (d) $I_{\rm ON}$ considering the joint effect of variations in all the device parameters at iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$. The range of variation in $\Phi_G = \pm 10$ mV. The range of variation in other device parameters is $\sim \pm 5\%$ of the nominal value.

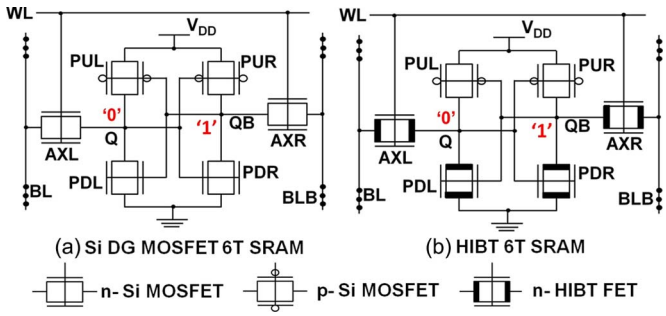

Fig. 8. Schematics of (a) Si-DG-MOSFET-based 6T SRAM and (b) hybrid 6T SRAM with Si DG MOSFETs as PU transistors and HIBT FETs as AX and PD transistors.

To sum up, CBO in HIBT FETs leads to reduced $I_{\rm OFF}$ variations across different voltages and lower $I_{\rm ON}$ variations at low $V_{\rm DD}$. As CBO increases, $I_{\rm OFF}$ variations in HIBT FETs decrease. Due to higher process variation tolerance in HIBT FETs compared to that in Si DG MOSFETs, one potential application for HIBT FETs is in the implementation of SRAMs. In a conventional Si-MOSFET-based 6T SRAM, the mismatch between transistors due to parameter variations leads to a reduction in cell stability and an increase in cell leakage. Lower cell stability may preclude $V_{\rm DD}$ scaling, even though the frequency requirements are low. However, significantly lower variations in $I_{\rm OFF}$ in HIBT FETs make them promising devices for low-power robust SRAMs. In the next section, we will evaluate the impact of low $I_{\rm OFF}$ variations in HIBT FETs on the cell stability and power of SRAMs under process variations.

IV. HIBT-FET-Based 6T SRAMs

We analyze a hybrid 6T SRAM [Fig. 8(b)] with HIBT FETs as pull-down (PD) and access (AX) transistors and Si p-MOSFETs as pull-up (PU) transistors. We also compare HIBT-FET-based 6T SRAM to a standard 6T SRAM [Fig. 8(a)]

TABLE IV
CHANGE IN GATE WORKFUNCTION OF PMOS OF HIBT FET SRAM WITH RESPECT TO THE GATE WORKFUNCTION OF PMOS IN Si DG MOSFET SRAM. CBO REFERS TO THE CBO IN THE AX AND PD TRANSISTORS IN HIBT FET SRAM

CBO (eV)	0.1	0.25	0.35
Iso-L_{SP}	-10meV	-30meV	-60meV
Iso-L_{CH}	0	-25meV	-40meV

in which all the transistors are Si DG MOSFETs. The gate workfunction of p-MOSFETs is optimized separately for HIBT FET and Si-DG-MOSFET-based SRAMs (see Table IV). Since HIBT FETs have a lower drive strength, the strength of the PU devices in HIBT FET SRAM is decreased by lowering Φ_G. This results in optimal read stability and write ability. Note that the Φ_G of PU devices at iso-$L_{\rm SP}$ is lower compared to that at iso-$L_{\rm CH}$ because the strength of the AX HIBT FET is lower in the former case. We perform the analysis for the following two cases: 1) nominal case in which there are no variations in the devices and 2) considering the worst case process variations in the devices, including the variations in the PU Si DG p-MOSFET. The transistor mismatch which has the worst effect on the cell stability and leakage is considered for the analysis [33].

Fig. 9(a) shows the comparison of the cell leakage of HIBT-FET- and Si-DG-MOSFET-based 6T SRAMs at iso-$L_{\rm SP}$ for CBO $= 0.25$ eV. In the nominal case, cell leakage is similar since the devices are designed under iso-$I_{\rm SUB}$ conditions. However, low $I_{\rm OFF}$ variations in HIBT FETs lead to a lower deviation of cell leakage from the nominal values. Hence, a large reduction in cell leakage is observed in HIBT-FET-based SRAM compared to the Si-DG-MOSFET-based SRAM under worst case process variations. (Note that lower Φ_G of PU in HIBT FET SRAM also contributes to reduction in cell leakage. However, decrease in $I_{\rm OFF}$ variations in HIBT FETs is the dominant reason for leakage reduction).

The comparison of read and hold stabilities in Fig. 9(b) and (c) shows that, in the nominal case, Si DG MOSFET SRAM has higher read static noise margin (SNM) and similar hold SNM. This is due to a higher $I_{\rm ON}-I_{\rm OFF}$ ratio in Si DG MOSFETs. However, when process variations are considered, the deviations of read and hold SNMs from their nominal values are lower in HIBT FET SRAM compared to those in Si DG MOSFET SRAM. This is due to the lower variation in $I_{\rm ON}-I_{\rm OFF}$ ratio in HIBT FETs. As a result, HIBT FET SRAM exhibits higher read SNM and similar hold SNM under process variations.

HIBT FET SRAMs also show a higher write margin (WM) at scaled $V_{\rm DD}$ [Fig. 9(d)]. This is because Si p-MOSFETs have higher g_m and lower SS compared to HIBT FETs. Thus, as $V_{\rm DD}$ is lowered, a sharper decrease in the strength of PU (Si DG) compared to AX (HIBT) is observed. This leads to an increase in the WM of HIBT FET SRAM compared to that of Si DG MOSFET SRAM.

Fig. 9 shows the suitability of HIBT FETs for low-voltage SRAM due to reduced cell leakage and higher read, hold, and write stabilities under process variations. Let us now compare the cell stability and cell leakage of Si-DG-MOSFET- and HIBT-FET-based SRAMs for different CBOs (Fig. 10). The results are shown for $V_{\rm DD} = 0.4$ V at iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$, considering worst case process variations. It can be observed that the HIBT FETs with a higher CBO offer reduced cell leakage under process variations due to lower $I_{\rm OFF}$ variations. On the other hand, higher read and hold SNMs are achieved for lower CBO because of higher $I_{\rm ON}-I_{\rm OFF}$ ratio, under process variations. The trend of WM with respect to CBO is different at iso-$L_{\rm SP}$ and iso-$L_{\rm CH}$. This is explained as follows. There are three effects of the increase in CBO of AX and PD devices on WM.

1) As CBO increases, Φ_G for PU MOSFETs is reduced (Table IV) which increases their $|V_{\rm TH}|$. Due to larger $|V_{\rm TH}|$ and reduced overdrive voltage ($|V_{\rm GS}| - V_{\rm TH}|$), the variations in $I_{\rm ON}$ of PU FinFETs increase. This tends to reduce WM under process variations.
2) An increase in CBO leads to lower variability in AX and PD devices. This tends to increase WM under process variations.
3) A larger CBO results in higher SS and lower g_m. This leads to higher strength of the AX transistors relative to the PU transistors at low $V_{\rm DD}$, as explained before. As a result, WM tends to increase.

At iso-$L_{\rm SP}$, the effect of variations in PU devices dominates because their optimal Φ_G is lower ($|V_{\rm TH}|$ is higher) than at iso-$L_{\rm CH}$ (see Table IV). Hence, WM decreases with increasing CBO. On the other hand, at iso-$L_{\rm CH}$, an increase in the variability of p-MOSFETs is relatively less important. Moreover, for low CBO, g_m of HIBT FETs is comparable to that of Si DG MOSFETs at iso-$L_{\rm CH}$. As a result, the decrease in WM with $V_{\rm DD}$ scaling is higher at low CBO than at high CBO. Hence, WM decreases with decreasing CBO. It can also be observed from Fig. 10 that, compared to Si DG MOSFET SRAM, improvement in the read SNM, WM, hold SNM, and cell leakage is achieved in HIBT FET SRAM for all CBOs.

In summary, HIBT FETs exhibit low $I_{\rm OFF}$ variations due to CBO and the absence of dopant straggle. This leads to significant reduction in SRAM cell leakage and higher cell stability at low $V_{\rm DD}$ under parameter variations, compared to Si-DG-MOSFET-based SRAM. As a result, HIBT FETs are suitable for low-voltage SRAMs, in which $V_{\rm DD}$ scaling is limited by cell stability rather than cell performance.

V. CONCLUSION

We have proposed heterojunction intra-band tunnel (HIBT) FETs with different semiconductor materials (with matched lattice constants) in the S/D and channel regions. We showed that a CBO is introduced at the S/D–channel heterojunction and the carrier transport in the ON state occurs by intra-band tunneling. We performed the analysis for different values of CBO. The iso-$I_{\rm SUB}$ comparison of HIBT FETs with Si DG MOSFET showed degradation in $I_{\rm ON}$, I_{GON}, SS, and g_m but improvement in DIBL/T and $g_{\rm DS}$. The trends with respect to CBO showed that DIBL/T decreases with increasing CBO. At the same time, $I_{\rm ON}$, SS, and g_m degrade as CBO increases. However, it was shown that the principal advantage of HIBT FETs is

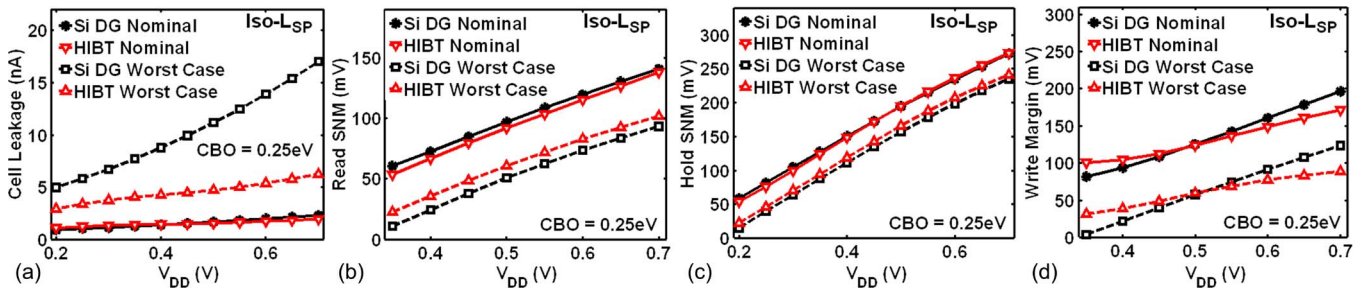

Fig. 9. Comparison of (a) cell leakage, (b) read SNM, (c) hold SNM, and (d) WM of Si DG MOSFET SRAM and HIBT FET SRAM for different V_{DD} values at nominal corner and considering worst case process variations (CBO = 0.25 eV at iso-L_{SP}).

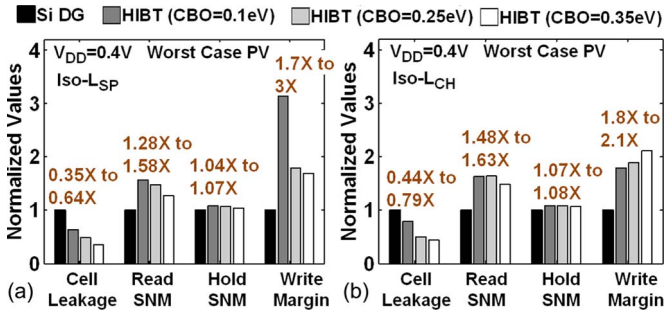

Fig. 10. Comparison of the cell leakage, read SNM, WM, and hold SNM of Si DG MOSFET SRAM and HIBT FET SRAM for different values of CBO considering worst case process variations (PV) (a) at iso-L_{SP} and (b) at iso-L_{CH} (V_{DD} = 0.4 V).

a significant reduction in I_{OFF} variations. At the same time, HIBT FETs showed reduction in I_{ON} variations at low V_{DD}. Variations in I_{OFF} across different V_{DD} and variations in I_{ON} at low V_{DD} were observed to decrease with increasing CBO. Near-dopant straggle-free characteristics of HIBT FETs due to heterovalent S/D and channel materials were also discussed. Based on the device analysis, we explored the application of HIBT FETs in low-voltage SRAMs. An improvement in cell stability and leakage was observed at low V_{DD} under process variations in HIBT FET SRAM compared to Si DG MOSFET SRAM. A higher improvement in read and hold stability was observed for lower CBO, while a larger reduction in cell leakage was observed for higher CBO. The analysis shows that HIBT FETs have a large potential as memory devices for low-voltage SRAMs.

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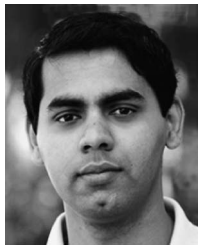
Sumeet Kumar Gupta (S'05) received the M.S. degree from Purdue University, West Lafayette, IN, in 2008, where he is currently working toward the Ph.D. degree in the School of Electrical and Computer Engineering.



Jaydeep P. Kulkarni (M'09) received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN.

He is currently a Staff Research Scientist with the Circuit Research Laboratory, Intel Corporation, Hillsboro, OR.

Suman Datta (SM'06) received the Ph.D. degree from the University of Cincinnati, Cincinnati, OH, in 1999.

He is currently a Professor of electrical engineering with The Pennsylvania State University, University Park.

Kaushik Roy (F'01) received the Ph.D. degree from the University of Illinois, Urbana-Champaign, in 1990.

He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor.