Impact of Contact and Local Interconnect Scaling on Logic Performance

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Abstract: We perform a comparative analysis of metal-Si and metal-insulator-Si (MIS) contacts and quantify the impact of the contact/via resistances on logic performance. Our results show that silicide contacts account for 32% degradation in the ON current of an nFinFET (I_{ON}) compared to ideal contact. MIS contacts which lead to lowering of Schottky barrier height provide 12% performance gain at iso-energy. Technology scaling to 5 nm will make MIS contact contribute 35% to the overall extrinsic resistance, with metal resistance contribution rising to 20%.

Introduction: Physical gate length and electrical oxide thickness scaling along with channel strain engineering has resulted in continual increase in the *intrinsic* transistor drive strength. It is also accompanied by scaling of contacted gate pitch, contact area and the metal line width/pitch (M0/M1 via/local interconnect) as depicted in Fig. 1. These factors lead to significant increase in the extrinsic resistance (R*extrinsic*), which limit the *extrinsic* performance of devices. In this invited paper, we quantify different components of R*extrinsic* and investigate their impact on logic performance. We use a commercial numerical device simulator [1] to model transport in M0/M1 metal layer contact structure, self-consistently with an n-Si-FinFET, calibrated against experiments [2]. Both silicide and MIS contacts are explored in this work. The impact of diffusion barrier scaling on metal resistance is also quantified. We provide scaling projections to underscore the importance of finding novel solutions for extension resistance, contact resistance and metal resistance in future technologies.

Components of Extrinsic Resistance: In order to investigate the relative contributions of various components of the extrinsic resistance, we estimate the contact geometry as well as via and metal layer information (including barrier layers) from published 22 nm technology (Fig. 2(a)). Si-FinFET device architecture is chosen for the active component. The FinFET makes electrical connection with local interconnect M0 (tungsten, W) through a W contact with Ti/TiN serving as the barrier layer. M0 connects to the first metal layer M1 through Cu, via (via0) with TaN/Ta acting as a barrier layer. For nickel silicide-based contacts, the interface between the n+ doped source/drain (S/D) regions and the W contact is characterized by a Schottky barrier height of 0.65 eV. Our analysis shows that S/D extension resistance contributes to 52% of the total extrinsic resistance. Silicide interface resistance is another significant component (44 %) while the contribution of other metal layers is limited to 4%. In order to lower the extrinsic resistance, we first explore the viability of replacing the NiSi silicide contact with the MIS contact.

Interface Contact Engineering:

A. MIS Contact: The Schottky barrier height of 0.65eV at the interface of NiSi and n+ doped Si S/D is due to the metal Fermi level pinning to the charge neutrality level residing within the silicon bandgap. Fermi level pinning arises from the metal electron wavefunction (Ψ) spilling into the metal induced gap states (MIGS) and contributing to a Bardeen barrier [3]. Metal work-function engineering has limited success in reducing the Schottky barrier height (Fig. 3). Hence contact resistivity cannot be easily lowered other than increasing doping level in the S/D region. In order to mitigate the Fermi level pinning and lower the contact resistance, an insulator can be introduced between metal and Si [3] to prevent the penetration of metal wavefunction (Fig. 4). The strength of Fermi level pinning is measured by S factor [4]. The S factor for insulator is higher than that for the metal-semiconductor case (Fig. 5), due to the reduction of density of MIGS, resulting in Fermi level unpinning [4]. TiO_2 or a sub-stoichiometric TiO_x is a promising candidate to obtain low contact resistivity (Fig. 6(a)) as it has a small conduction band offset with Si [4]. The experimental data for Ti-TiO_2-Si shown in Fig. 6(b) indicates 79% reduction in the contact resistance due to unpinning of the Fermi level [3].

B. Extrinsic Resistance in 22 nm Technology: The effect of contact resistance on the output characteristics of n-Si-FinFET is shown in Fig. 7. While silicide contacts lead to 32% degradation in I_{ON}, the impact of MIS contacts on I_{ON} is much less (12%). Fig. 8 shows M0/M1, interface and S/D extension resistances for silicide and MIS contacts. MIS contacts lead to 75% reduction in the interface contact resistance compared to silicide contacts. M0/M1 contributes less than 7% to extrinsic resistance. The breakdown of components of M0/M1 resistance reveals that 61% resistance comes from near the Cu via region, a result of current crowding in thin Cu Via and surrounding high resistive nitride barrier layers.

C. Layout and Circuit Analysis: The impact of extrinsic resistance on logic performance is strongly dependent on the circuit layout. Fig. 9 (inverter layout) shows a single metal contact that sources/sinks the current for two fingers (worst case scenario). This effectively doubles the resistance of the contact and the overlying metal layers relative to the S/D extension and the transistor resistance. Considering the worst case layout, we analyzed the impact of contact resistance on circuit delay. The benefits of MIS contact are evident in Fig. 10. Lower inverter delay for MIS contacts compared to silicide enables V_{DD} scaling and results in 20% energy savings at iso-delay, or 12 % delay reduction at iso-energy.

Scaling Projections

We project impact of scaling on extrinsic resistance from 22 nm to 5 nm technology using ITRS 2011 specifications (Fig. 1). The effect of size dependent resistivity in M0/M1 interconnect scaling is included in this analysis. Fig. 11 shows the trends for metal, contact interface and S/D extension resistance for silicide and MIS contacts. Technology scaling from 22 nm to 5 nm increases the contribution of the interface contact resistance from 44 % to 66 % in silicide case and from 14% to 35% in MIS case. This is due to reduced cross-sectional dimensions of the contact in 5 nm technology. M0/M1 resistance increases from 4% (22 nm) to 10% (5 nm) in silicide case and from 6% to 17 % in MIS case. Primary factors affecting M0/M1 resistance are size dependent resistivity effects (electron scattering from metal surface and grain boundaries) along with increasing fraction of via/interconnect cross-section occupied by resistive diffusion barriers (Fig. 1(b)). We explored the option of replacing TaN/Ta Cu diffusion barrier by RuTaN mixed phase ALD grown thin film barrier [6][7]. RuTaN barrier provides 40% reduction in M0/M1 resistance owing to scaled thickness (3 nm) compared to the 7 nm thick TaN/Ta diffusion barrier as shown in Fig. 12.

Future Outlook

We analyzed the effect of contact and M0/M1 metal resistance on the logic performance in current and future technologies. The silicide contact resistance remains a key performance bottleneck

along with S/D extension. The extrinsic resistance can be lowered by replacement of silicide with MIS contact. To reduce overall extrinsic resistance in future technologies, new diffusion barrier materials and novel insulators for MIS contacts need to be explored.

References

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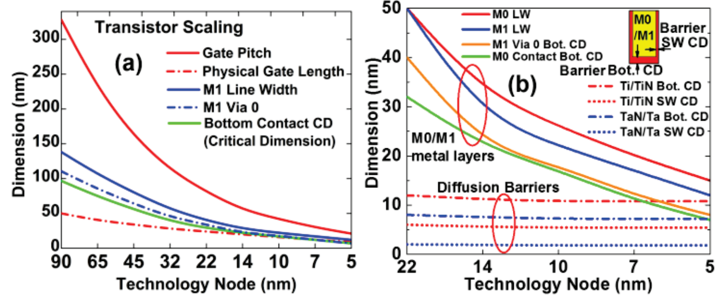

Fig.1. (a) Transistor scaling reduces source-drain contact areas (b) M0/M1 Line Width (LW) scaling in contrast to almost constant diffusion barrier CD; both increase contact resistance.

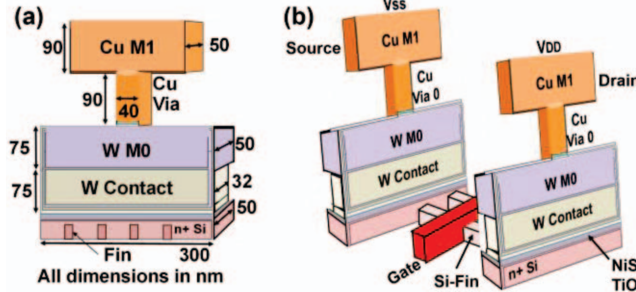

Fig. 2 (a) 22 nm process, reference dimensions [2]; view orthogonal to Si-Fin (b) Si-FinFET with source and drain contact structure.

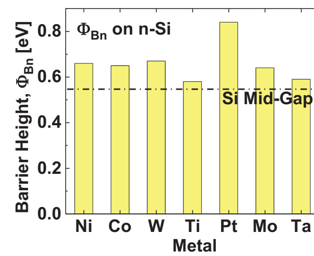

Fig. 3. Schottky barrier height (SBH) for metals on n-Silicon.

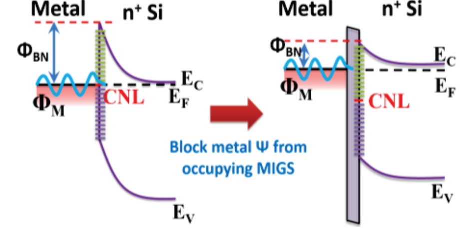

Fig. 4. Inserting insulator between metal and silicon alleviates Fermi-level pinning. MIGS and CNL denote metal induced gap states and Si charge neutrality level.

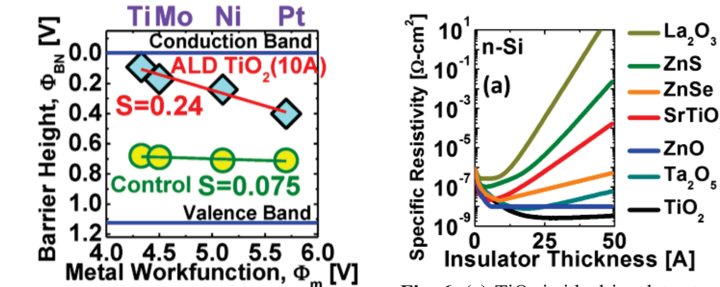

Fig. 5. Experimental SBH vs. workfunction for metal/n$^-$ Si and metal/TiO_{2-x}/n$^-$ Si. A 3.2× higher S factor of 0.24 is obtained, with SBH reduced to 0.15eV, for MIS with low workfunction metal Ti, compared to metal/n$^-$ Si.

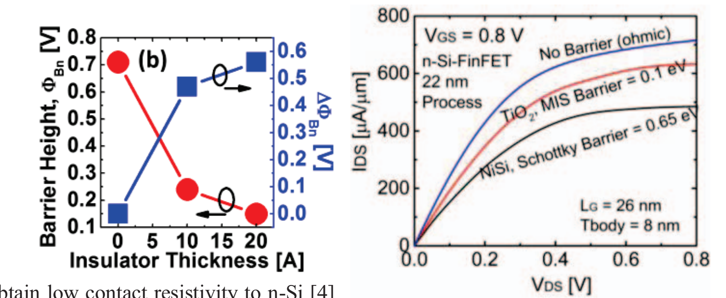

Fig. 6. (a) TiO_2 is ideal insulator to obtain low contact resistivity to n-Si [4] (b) Barrier height reduction from 0.7V for M-S case to 0.15V for 20Å TiO_2 [3].

Fig. 7. Output characteristics of Si-FinFET with no barrier, Schottky barrier and MIS barrier at contact interface.

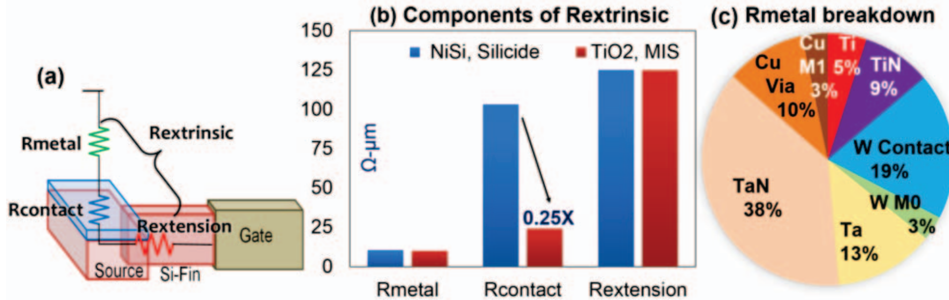

Fig. 8. (a) Components of total extrinsic resistance. The contribution of M0/M1 metal layers is modeled as Rmetal (b) Extension resistance of Si-Fin and contact resistance are dominant contributors to Rextrinsic. The contact resistance of TiO_2 MIS contact is 75% reduced compared to NiSi silicide contact (c) Analysis of individual components of Rmetal. 61% of Rmetal comes from near via region due to current crowding in via and surrounding high resistive nitride barrier layers

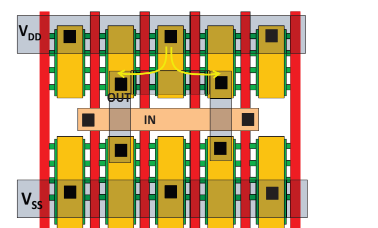

Fig. 9. Shared contact/diffusion drive double the number of fins, worsening impact of source/drain resistance on cell performance.

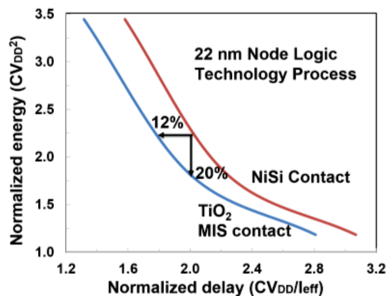

Fig. 10. TiO_2 MIS contact exhibits improved energy-delay performance compared to NiSi silicide contact. Ieff is calculated as described in [5].

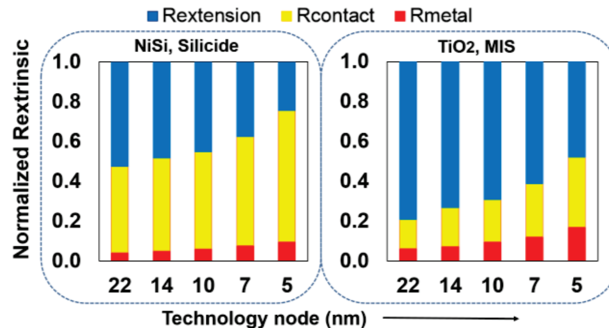

Fig. 11. Relative contributions of contact resistance and M0/M1 resistance increase with scaling. Rmetal amounts to 17% of total Rextrinsic at 5nm technology node in MIS contact.

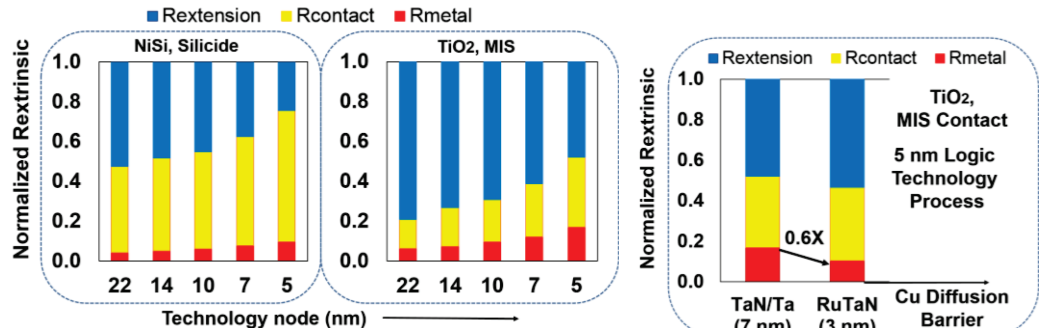

Fig. 12. ALD grown thin mixed phase RuTaN diffusion barrier [6][7] reduces Rmetal by 40%.