Tunnel Transistors for Energy Efficient Computing

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***Abstract*— Tunnel transistor (TFET) is a potential steep slope device enabling supply voltage scaling. TFET is explored at the device and circuit level. Hetero-junction TFET is demonstrated with high drive current and high on-off current ratio. Hetero-junction TFETs with scaled device geometry can outperform Si FinFET at V_{cc}<0.3V. Design considerations of TFET based circuits for logic and SRAM applications are investigated and performance benchmarked with Si FinFET technology.**

Index Terms- Tunnel FET; III-V semiconductors; steep slope; switching slope; interface states; MBE TFET Verilog-A model; TFET circuit implementation; TFET adder design; TFET SRAM design; noise margin

I. INTRODUCTION

The miniaturization of the transistor and it's ever growing density on the chip has resulted in an increased overall power consumption. Supply voltage scaling results in a quadratic reduction in the dynamic power consumption thereby achieving energy efficient operation in digital circuits. However, reducing the supply voltage of a transistor requires that the threshold voltage be scaled proportionately in order to achieve the same performance. But this also results in an exponential increase in the static power consumption arising from the fundamental limitation of sub-threshold swing limited to 60mV/decade at room temperature in a MOSFET. Tunneling Field Effect Transistors (TFETs), in principle, can achieve sub-60mV/decade switching slope (SS) at room temperature due to the energy filtering achieved by band to band tunneling [1-2], thus enabling voltage scaling [3]. However, the drive current that can be achieved is limited due to the tunneling barrier present at the source-channel interface. III-V semiconductor based TFETs are attractive due to their direct band-gap and wide range of compositionally tunable band-alignment [4].

Due to the asymmetrical p-i-n structure constituting the source-channel-drain, Tunnel FET exhibits uni-directional conduction, steep slope and delayed saturation characteristics. Thus the circuit implementation of HTFET requires modification in the traditional CMOS design. In order to achieve the best energy efficiency using HTFET, novel circuit design techniques in SRAM and logic are being explored taking into account the practical limitations of Tunnel FETs and the resulting operating voltage range. Given the increase in the sensitivity to variation and the delay in the circuit application using sub-threshold Silicon FinFET, circuit-level benchmarking comparing sub-threshold Si CMOS with HTFET can provide more insight in potential performance improvement and energy savings for low supply voltage (V_{CC}) application.

This paper is divided into five sections. In section II, the design of nTFETs to achieve high on-current and high on-off current ratio is discussed. Section III covers the growth challenges and electrical characterization of the fabricated hetero-junction TFETs. The projected characteristics of nTFET and pTFET with scaled device geometries are discussed in section IV. In section V, circuit level design considerations for implementing TFETs as energy efficient devices are explored and benchmarked with super-threshold and sub-threshold Si FinFETs.

II. N-CHANNEL TFET DESIGN

The current generation mechanism in a TFET involves tunneling through a barrier and, hence, the drive current can be severely limited. To mitigate this limitation, III-V material systems, with their direct and tunable band-gaps are being explored. However, the drive current enhancement with reduced band-gap of such materials comes at the expense of increased off-state leakage current (I_{OFF}) through bulk Shockley-Read-Hall generation and the drain side band to band tunneling current [5-7]. The switching slope (SS) in a TFET, unlike MOSFET, is a function of the drain current and, hence, the reduction in the off state leakage floor (I_{OFF}) is essential to the demonstration of the steeper part of the transfer characteristics just when the band edges separate [5-7]. Hetero-junction TFETs enable simultaneous enhancement of the higher drive current as well as lower I_{OFF} [8]. The higher drive current in a hetero-junction TFET comes from the reduction in the effective tunneling barrier (Eb_{eff}) at the source-channel junction without reducing the band-gap of the channel material. In this invited paper, two TFET material systems with varying band-alignment at the source-channel interface are studied: (a) $In_{0.7}Ga_{0.3}As$ homo-junction TFET (HomJ) and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-junction TFET (HetJ). By changing the source material to GaAsSb, the band-alignment at the source-channel interface changes to a staggered gap alignment and Eb_{eff} reduces to 0.25eV.

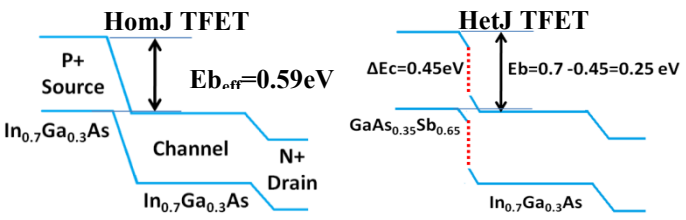

Fig. 1. Schematic energy band-diagram showing band-alignment and effective tunnel barrier for the different TFET systems

III. N-CHANNEL TFET GROWTH AND ELECTRICAL CHARACTERIZATION

Solid source Molecular Beam Epitaxy (MBE) is used to grow the TFET layers which can produce high quality multi-layer epitaxial wafers with in-situ doped abrupt tunnel junctions. Both layers are grown metamorphically on lattice mis-matched InP substrates using linearly graded $Al_xIn_{1-x}As$ buffer. In comparison to HomJ TFET which is lattice matched to InP substrate, the MBE growth of the HetJ TFET poses significant challenge. The change of group V flux from Antimony (Sb) to Arsenic (As) in the mixed anion GaAsSb to mixed cation InGaAs layers can introduce interface intermixing of cations and anions which can lead to uncontrolled layer composition at the hetero-junction interface. While switching from Sb rich source to As rich channel, there is likelihood of formation of a binary material, either GaAs or InAs layer at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-interface. Strained mono-layers of GaAs is 5.3% lattice mismatched to $In_{0.7}Ga_{0.3}As$, while strained InAs is 1.9% lattice mismatched. While switching, if the growth of this binary layer is beyond the critical thickness, then the chances of forming threading dislocations is higher for the GaAs like interface, than that for InAs. High density of threading dislocations and interface material intermixing can result in large amount of interface defects or Tamm states.

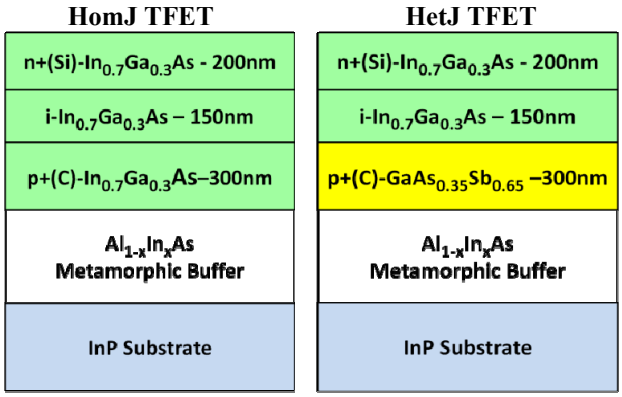

Fig. 2. MBE grown epitaxial layers for (a) HomJ and (b) HetJ TFET

In this invited paper, two different growth conditions were implemented for the HetJ TFET: (a) **GaAs like surface**: While switching the Sb flux was stopped and under As over pressure the temperature of the Ga cell was ramped up for the growth of $In_{0.7}Ga_{0.3}As$. (b) **InAs like surface:** In this growth, while the cell temperature of Gallium (Ga) was ramped up, Indium (In) was preferentially flown to avoid formation of GaAs layer and form a few mono-layer of InAs instead. Figs. 3 (a,b) show asymmetric (115) reciprocal space maps of the High HetJ TFET structures. In both cases, the growth of the metamorphic buffer results in an $In_{0.65}Al_{0.35}As$ "virtual" substrate with $\geq$ 90% strain relaxation. However, the subsequent $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ active device layers differ in their strain with respect to the "virtual" substrate. With the GaAs terminated hetero-interface, the active layers are strain relaxed and susceptible to defect formation, whereas the device layers in the InAs terminated interface are pseudomorphic to the $In_{0.65}Al_{0.35}As$ "virtual substrate" and likely "defect-free".This is evident in Fig. 3 (c,d) where atomic force microscopy (AFM) images reveal lower surface roughness(4.5nm) and 2D cross-hatch pattern for InAs terminated wafer compared to the GaAs terminated one (with roughness of 5.6nm and no cross-hatch pattern).

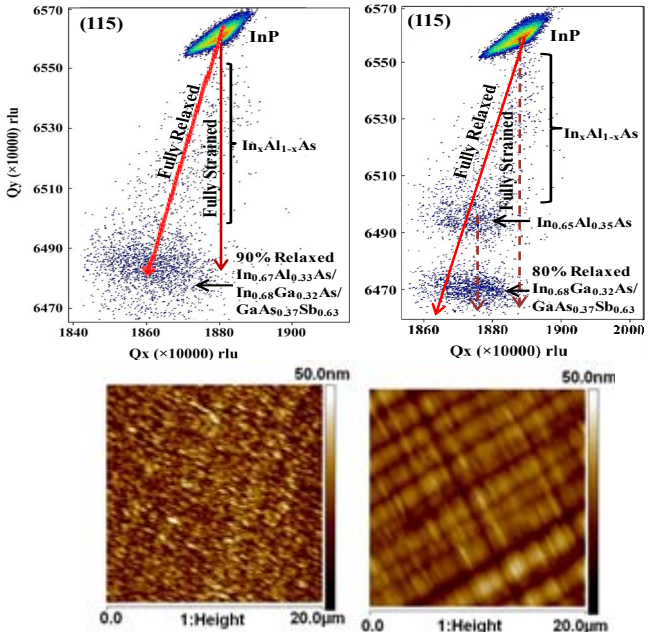

Fig. 3 (a,b). Asymmetric (115) reciprocal space map and (c,d) 20x20 μm2 atomic force microscopy image of High HetJ TFET layers for the cases with GaAs and InAs terminated hetero-interfaces

Fig. 4(a-d) shows the electrical characteristics of the fabricated HomJ and HetJ TFETs at room temperature. HetJ TFETs exhibit higher drive current with comparable I_{ON}/I_{OFF} ratio to HomJ TFETs. More than three order of magnitude improvement in I_{on}/I_{off} ratio achieved in HetJ TFET is due to the reduction in defect assisted conduction with InAs termination. The improvement in heteroepitaxy with InAs termination is reflected in the improved electrostatics (smaller SS and DIBT) for the same device geometry. I_{on} progressively increases by 325% with decreasing Eb_{eff} (from 0.58eV to 0.25eV) due to the increase in tunneling transmission coefficient. Second, the drain induced barrier thinning (DIBT) improves with reducing Eb_{eff} due to inter-band generation occurring closer to the source/channel junction, thus improving device electrostatics . The SS vs I_{ds} curve also shifts with reducing Eb_{eff}, with the minimum SS occurring at higher I_{ds} which is essential for TFET operation with MOSFET like performance. However, the minimum SS at room temperature is still much higher than 60mV/decade. The SS in all the fabricated devices is greater than 60 mV/dec at room temperature due to the presence of high density of interface

states D_{it} at the high-k/channel interface [5] and can be improved by including proper surface passivation and high-temperature anneal process steps.

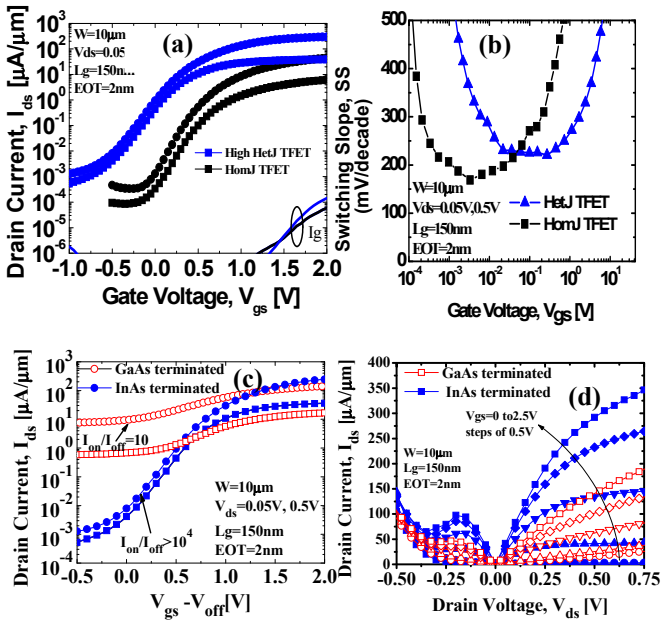

Fig. 4 (a,b). Measured transfer characteristics and SS of HomJ and HetJ TFETs at room temperature (c,d) Comparison of InAs terminated and GaAs terminated HetJ TFETs.

IV. TFET PROJECTIONS

Fig. 5(a-b) shows comparison of the simulated TFETs with body thickness (T_{body}) of 7nm, electrical oxide thickness (Toxe) of 0.8nm and gate length (Lg) of 26nm with the 22nm Trigate transistor [9].TFET TCAD model calibrated with the atomistic non-equilibrium Greens function (NEGF) simulations has been used for simulations. Steep slope broken-gap nTFETs clearly outperform Si FinFETs at Vcc=0.3V. Broken-gap pTFETs on the other hand, though can achieve higher drive currents than Si FinFET, the SS is limited to 60mV/decade which is attributed to source side degeneracy issue as discussed below.

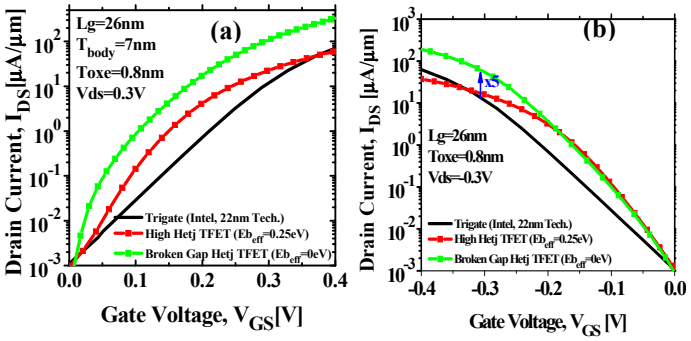

Fig. 5 (a,b). Projected TFET characteristics with UTB device dimensions and scaled oxide.

Boosting the drive current in a TFET requires higher junction electric field and hence the source material is heavily doped. In pTFETs, due to low density of states (DOS) in the conduction band, the Fermi level moves deep in to the conduction band. As a result, a large portion of the temperature dependent part of the source Fermi function participates in tunneling leading to a temperature dependent and kT/q limited sub-threshold slope (Fig 7B). Thus design of a pTFET involves a trade-off between achieving high drive currents and steep SS. One possible solution is to incorporate strain and orientation effects under confinement to improve the density of states of the conduction band.

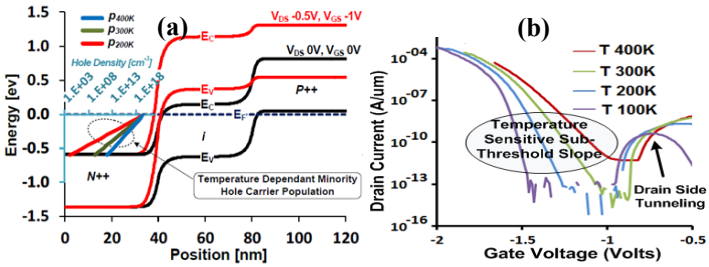

Fig. 6 (a,b). kT/q limited SS in pTFETs under heavy doping due to low DOS in conduction band of n-type source [10].

Thus, hetero-junction TFETs with scaled oxide and ultra-thin body dimensions can outperform MOSFETs for supply voltage <0.3V. However, realization of a complimentary TFET logic will need further investigation to address the source degeneracy issue existing in pTFETs.

V. TFET LOGIC DEISGN

A. TFET Modeling For Circuit Simulation

Because a compact SPICE model for TFET has yet to be developed, we generated a Verilog-A model from a Sentaurus device simulation to perform the circuit implementations of HTFETs and comparing with Si FinFETs circuits. Our device models have been calibrated with atomistic simulations and experimental data for GaSb-InAs HTFET and Si FinFET respectively [11]-[12] as shown in Fig. 7. Comparing with Si FinFET for LOP application with same off-state leakage (I_{off}=5nA/um), HTFET shows 7x on-current improvement at V_{DD}=0.3V with an average sub-threshold slope of 30mV/Dec .

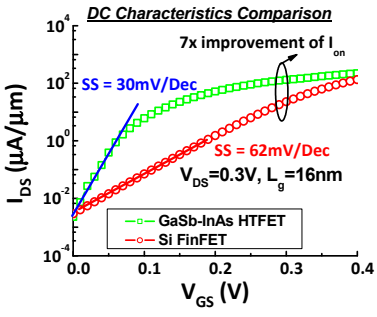

Fig. 7. I_{ds}-V_{gs} HTFET characteristics comparing with Si FinFET at L_g=16nm. HTFET shows 7x on-current improvement at V_{CC}=0.3V with 30mV/dec average subthreshold slope.

In order to perform circuit simulation, the transfer characteristics (I_{ds}-V_{gs}) of the HTFET and Si FinFET were obtained through DC simulation using TCAD Sentaurus [13] across a range of V_{ds} in a Verilog-A lookup table [14]. The device transient characteristics were also captured using small-signal analysis. $I_{ds}(V_{gs}, V_{ds})$, $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ characteristics are formed into two dimensional look-up tables and employed by the Verilog-A models for Spectre [15] circuit simulation. Fig. 8 shows the Verilog-A small-signal model for HTFETs with the voltage transfer characteristics and the transient output characteristic of a HTFET inverter (V_{CC}= 0.5V), assuming the same drive strength for both pHTFET and nHTFET. It shows the validity of this Verilog-A lookup table based method as an efficient and accurate way of modeling the emerging device based circuits. In the following analysis, the device characteristics are generated from the double-gate device model with 20nm gate-length and 0.7 nm equivalent oxide thickness (EOT). An iso-performance pHTFET is assumed in the circuit simulation.

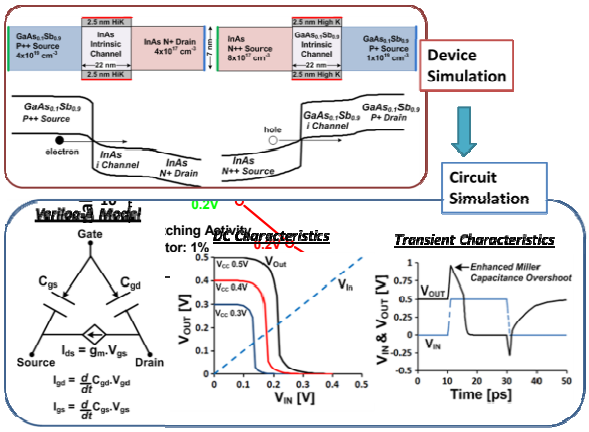

Fig. 8. Look-up table based verilog-A model generated from Sentaurus TCAD device simulation to perform TFET circuit analysis. DC and transient characterisitcs can be successfully captured.

In order to apply the steep slope device technology to the desired application domain for power reduction, the I_{on} versus I_{on}/I_{off} characteristics are shown in Fig. 9 comparing HTFET and Si FinFET by considering different operating points along the I_{ds}-V_{gs} curve for a given V_{CC} window [16]. At V_{CC} = 0.7V (Fig. 8(a)), 20nm Si FinFET provides the highest I_{on} and I_{on}/I_{off} ratio, making it the preferred device for operation at high V_{CC}. For V_{CC}=0.3V operation, Si FinFET performance is limited by the 60 mV/dec bottleneck of the sub-threshold slope, which cannot provide both high I_{on} and high I_{on}/I_{off} ratio(Fig. 8(b)). HTFET, on the other hand, shows the desired operation corner for both high I_{on} and I_{on}/I_{off} ratio at low V_{CC} due to steep subthreshold slope.

The energy-delay performance of a HTFET FO1 inverter is shown in Fig. 10 in comparison to that of a Si FinFET based FO1 (fanout of one) CMOS inverter. HTFET inverter shows a cross-over at V_{CC}=0.5V in the energy-delay characteristics with a better energy-delay tradeoff comparing Si FinFET for below 0.5V operation. Other logic gates, such as NAND, OR, NOR and XOR [14] also present similar cross-over which is consistent with the discussion above.

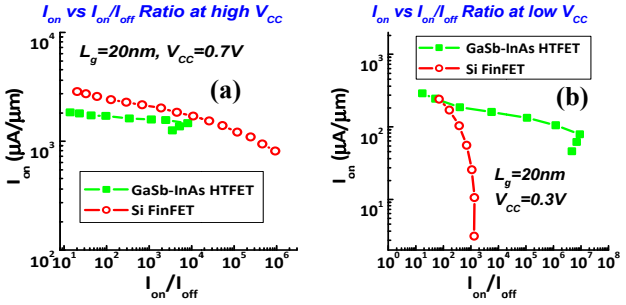

Fig. 9. Comparison of I_{on} versus I_{on}/I_{off} ratio for different operating points on the I_{ds}-V_{gs} for (a) a V_{CC} window of 0.7V and (b) a V_{CC} window of 0.3V. Si FinFET shows desired operation corner for high V_{CC}=0.7V, while HTFETE shows improved operation corner for V_{CC}=0.3V.

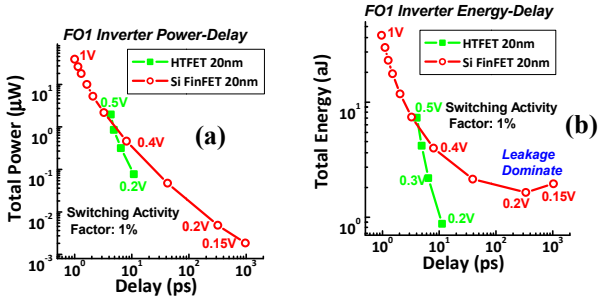

Fig. 10. FO1 inverter (a) power-delay and (b) energy delay comparison for 20nm Si FinFET and HTFET. HTFET shows improved energy efficiency for below 0.5V operation, while Si FinFET reaches the leakage bound at V_{CC}= 0.15V.

B. TFET Adder Design and Benchmarking

Based on the logic gates evaluation, a standard 32-bit Han-Carlson Adder is implemented with iso-performance pHTFET and nHTFET comparing with Si FinFETs for low power application. Fig. 11 shows the energy-delay performance of the 32-bit prefix-tree based Han-Carlson Adder [14] with 554 logic gates (constituting 162 NAND, 112 OR, 184 INV and 96 XOR). Due to the excessive computational cost of look-up table model based circuit simulation, the Energy-Delay was computed analytically using the Energy-Delay estimation for the gates. Critical-path analysis of the Han-Carlson Adder was applied in the Adder delay estimation. As shown in Fig. 11, a similar crossover is observed for the 32-bit Adder implemented using Si FinFET and HTFETs at V_{CC}=0.5V, where the HTFET-based 32-bit Adder can outperform Si FinFET-based 32-bit Adder with a favorable Energy-Delay trade-off. Moreover, as the leakage energy dominates the total energy consumption at low-activity level (1%) and low V_{CC}, Si FinFET-based 32-bit Adder reaches the energy minima at V_{CC}=0.4V and shows increased energy consumption for V_{CC}<0.3V operation. The HTFET-based 32-bit Adder, in contrast, shows continued energy reduction with V_{CC} scaling down to 0.15V because of its steep switching slope.

Due to the challenges of pTFET development as discussed in Section IV, nTFET-only logic based on pass transistors and

dynamic circuits has been studied and implemented for Sparse Prefix-tree Adder [17]. In MOSFET based circuit designs, only pFETs are employed as pull-up transistors due to the V_T drop of nFET caused output voltage range degradation. Because nTFET does not exhibit a significant V_T drop, it can be used in the pullup network without affecting the robustness of the circuit. Fig. 12 shows the Sparse Prefix Tree Adder which uses

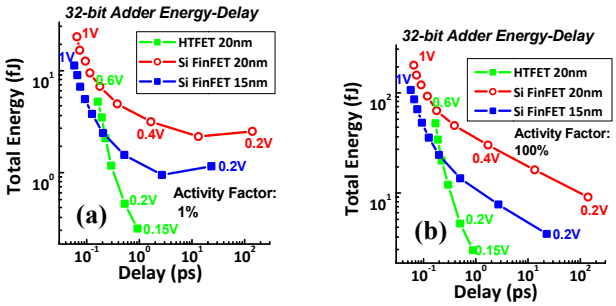

Fig. 11. 32-bit Han-Carlson Adder energy-delay evaluation for 20nm HTFET and Si FiFET and 15nm Si FinFET at activitity factor of (a) 100% and (b) 1% respectively.

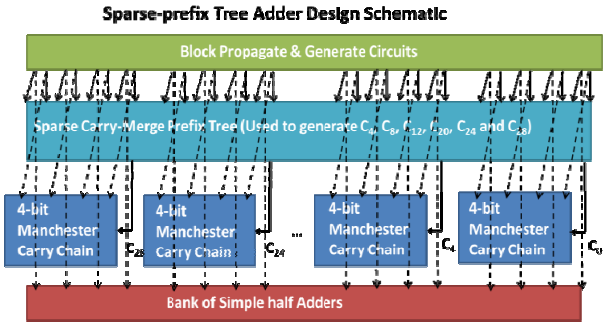

Fig . 12. Structural design of the Sparse-prefix tree adder schematic, including P and G and carries generation block, sparse carry-merge prefix tree and 4-bit macnchester carry chain.

smaller Manchester Carry Chain (MCC) units in addition to the prefix tree and provides the trade-off availability of all internal carry signals to obtain better area, energy and performance characteristics The 32-bit adder is partitioned into eight 4-bit blocks and each contains a 4-bit MCC to accept the appropriate propagate (P) and generate (G) signals for each pair of input bits as well as carry signals. The carries produced by the MMC and P signals are finally combined in the bank of single bit adders to produce the final sum. The proposed adder design was implemented with Si Fin-FETs (baseline reference) and two TFET explorations: both pHTFETs and nHTFETs (P/N HTFET), and nHTFET-only nTFETs. Fig. 13 shows the dynamic nHTFET-only MCC circuit schematic. The timing behavior and energy consumption over a range of voltages are evaluated, as shown in Fig. 14. P/N HTFET circuit is competitive with the Si FinFET implementation, which outperforms Si FinFET design for $V_{CC} < 0.5V$ in terms of both energy and delay metrics. nHTFET-only Adder design can further extend th marked Energy-Delay benefits and outperform Si FinFET Adder design at V_{CC}=0.6V with further improved energy efficiency at lower V_{CC}. This nTFET-only Sparse Tree Adder design outperforms the complementary HTFET design at all supply voltage nodes.

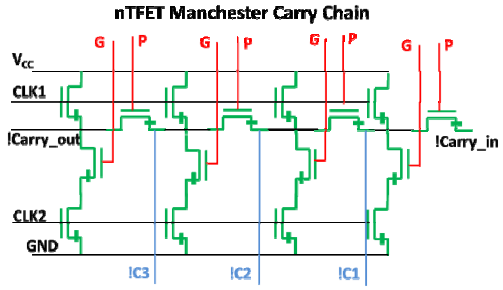

Fig. 13. nFET-only dynamic Machester Carry Chain (MCC) circuit design schematic. nTFET source terminal is illustrated.

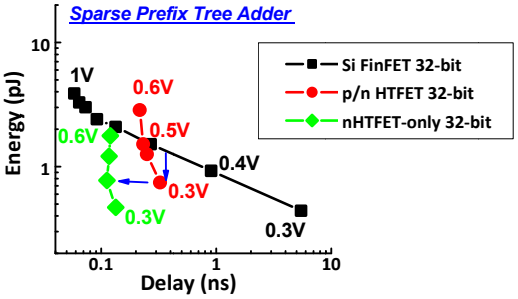

Fig. 14. 32-bit Sparse prefix tree adder energy-delay evaluation for 20nm Si FinFET design, complementary (P/N HTFET) HTFET design and nHTFET only design. nHTFET-only adder design shows significant energy efficienty improvement for V_{CC}< 0.6V.

C. TFET SRAM Design and Benchmarking

The unidirectional conduction in TFETs due to the asymmetrical p-i-n structure and delayed saturation output characteristics have strong impact on TFET Static Random Access Memory (SRAM) design. In order to maintain the desired read and write noise margin for low voltage application, traditional 6T CMOS SRAM needs to be modified for TFET application [11] with higher transistor count (8T or 10T).

Fig. 15 shows various 8T and 10T SRAM cell designs schematics using HTFET. The 8T HTFET Transmission-Gate (TG) SRAM cell has both inward and outward facing TFET access transistors to overcome the uni-directional conduction. Read is performed by enabling the inward-facing TFET access transistors AXL_{rd}(AXR_{rd}) using the read word-line (RWL), while write is performed by enabling both read and write word-lines (RWL/WWL). The 8T/10T dual-port (DP) SRAM cell has separated read and write access ports. Read is performed by enabling the RWL, while write is performed by only one-side of the access transistors (left or write) due to the uni-directional conduction property of the outward facing access transistors. The TFET Schmitt-Trigger (ST) SRAM cells (ST-1 and ST-2) have different orientation of the access transistors compared to the CMOS Schmitt-Trigger designs [18]. The TFET ST-1 SRAM cell has inward facing access transistors (AXL_{rd}/AXR_{rd}) and feedback transistors (NFL/NFR). Read is performed by enabling the inward-facing TFET access transistors AXL_{rd}(AXR_{rd}) using the word-line (WL), while

feedback is provided by the inward-facing NFR(NFL) transistors. Write is also performed by on-side of the access transistors with feed-back transistors disabled due to the uni-directional conduction. The TFET ST-2 SRAM cell has outward-facing access transistors (AXL_{wr}/AXR_{wr}) but inward-facing feedback transistors (NFL/NFR). Read is then performed by enabling the inward-facing TFET feedback transistor NFL (NFR) using the read word-line (RWL), while feedback is provided by the other inward-facing transistor NFR (NFL). Write is performed by enabling both read and write word-lines (RWL/WWL).

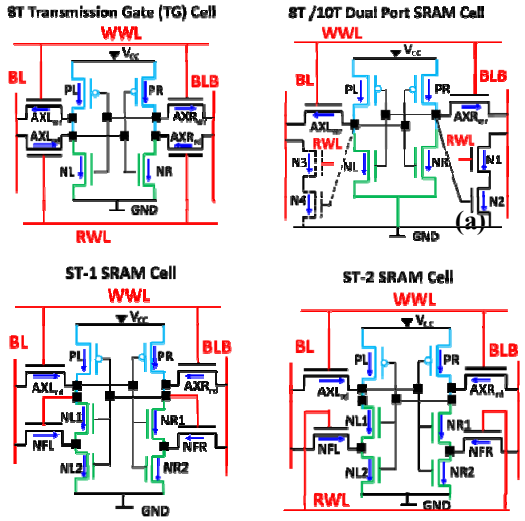

Fig. 15. Various SRAM designs using HTFETs including 8T Transmission Gate (TG) cell, 8T (10T) dual port (DP) cell, ST-1 and ST-2 with Schmitt-feedback. The unidirectional conduction is illustrated in each design.

Due to the write operation is uni-axial with only one-side HTFET participating, device-sizing has to be carefully studied for HTFET SRAM cell design with desired noise margin. Table I shows the sizing strategy of HTFET SRAM cells with iso-area comparing with the Si FinFET SRAM cells for SRAM figure-of-merit evaluation [11].

Table I Device Sizing Summary for Different SRAM Cell Designs

	NL1, NR1	NL2, NR2	PL, PR	AXL_{wr}, AXR_{wr}	AXL_{rd}, AXR_{rd}	NFL, NFR	N1-N4
6T CMOS 4x sized	8W	-	4W	4W	-		-
8T TG	2W	-	W	3W	W	-	
8T DP	2W	-	W	3W	-	-	W
10T DP	2W	-	W	2W	-	-	W
ST-1	2W	2W	0.1W	-	W	2W	-
ST-2	2W	2W	W	2W	-	2W	-

Fig. 16 (a-c) shows the comparison between the hold, read and write noise margin (SNMs) of various TFET and CMOS SRAM cells. For both hold and read-SNMs, Si FinFET SRAMs present a better SNM at high V_{CC}. For V_{CC}<0.3V, the HTFET SRAM cells provide improved read-SNM due to the drive current enhancement at low V_{CC}. The ST-1 and ST-2 HTFET cells exhibit better hold-SNM than the 8T HTFET Transmission-Gate cell due to the feedback. For read-SNMs, 8T Transmission-Gate SRAM cell is considerably degraded due to the delayed saturation, while the ST-2 cell shows 4x improvement due to the feedback. HTFET ST-2 cell shows better read-SNM comparing with HTFET ST-1 cell due to the sizing of the pull-up transistor (PL/PR). The HTFET SRAM cells present desired write-SNM comparing with Si FinFET SRAM design. The TFET ST-2 cell and the 8T Transmission-Gate SRAM cell have the best write-SNM due to the write-assist. 8T (10T) dual-port SRAM cells have the weakest write-SNM due to the uniaxial write operation. The utility of the Schmitt-Feedback in ST-1 and ST-2 can provide significant noise-margin benefits in HTFET SRAM cell design.

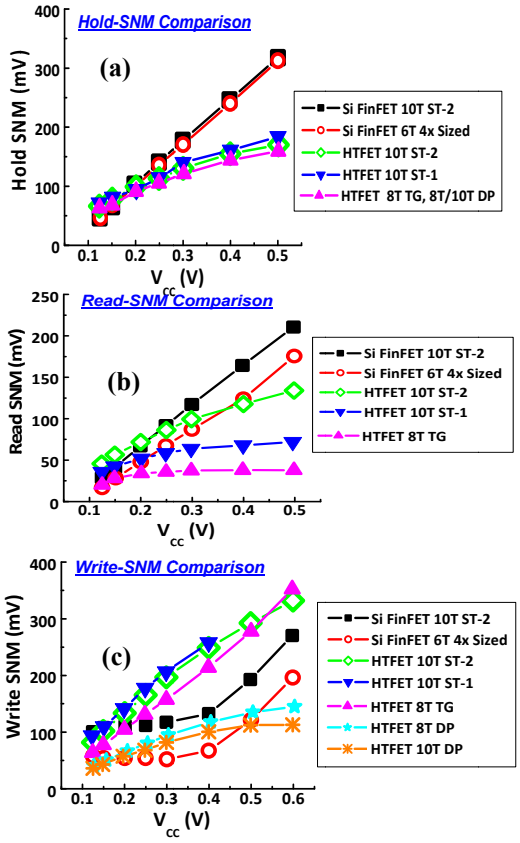

Fig. 16. (a) Hold-SNM, (b) Read-SNM and (c) Write-SNM evaluation for different TFET SRAM cell designs and Si FinFET 6T baseline design and 10T ST cell design. HTFET 10T ST-2 design shows desired noise margin for low V_{CC} operation.

In order to perform the benchmarking of the HTFET and Si FinFET-based memory, a 256×256 SRAM array with 50fF bit-line capacitance has been employed to estimate the dynamic energy consumption and the read access delay for different SRAM configurations [11]. As shown in Fig. 17(a), HTFET based SRAM designs present significant delay reduction for V_{CC} < 0.4V operation due to the drive-current enhancement compared to subthreshold Si FinFET operation. Fig. 17(b) shows the dynamic energy comparison for HTFET and Si FinFET SRAM array with a cross-over at V_{CC}=0.3V. For subthreshold Si FinFET operation, the off-state leakage dominates the power consumption. For HTFET SRAM cells, the outward facing access-transistors are forward biased p-i-n junctions in the hold-state, which can induce high p-i-n leakage energy for V_{CC} > 0.3 V.

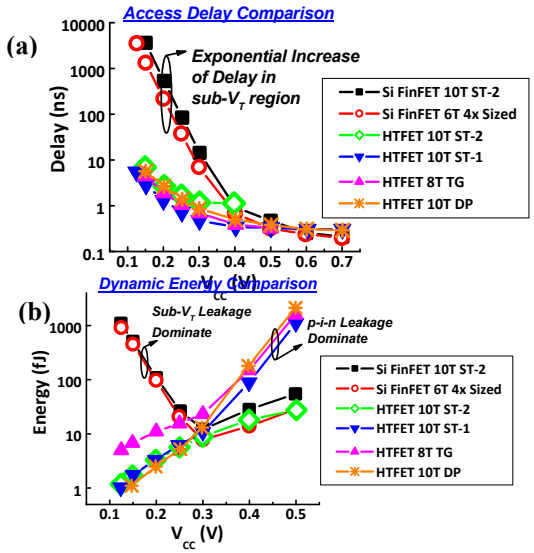

Fig. 17. Performance benchmarking of (a) access delay and (b) energy consumption with supply voltage scaling for different TFET SRAM cell designs comparing with Si FinFET SRAM cell designs. HTFET SRAM cells exhibt reduced delay and improved energy efficiency for low V_{CC} operation.

VI. Conclusions

In this invited paper, we have explored the energy efficiency computing using steep slope Tunnel FET from the device design and circuit implementation perspectives. Hetero-junction n-channel TFET is demonstrated with high I_{ON} and high I_{ON}/I_{OFF} ratio. With body-thickness and EOT scaling, nTFET and pTFET exhibits better performance than Si FinFETs at low V_{CC}. TFET based circuit design has been studied through Verilog-A model based circuit simulation with certain circuit elements modification. Compared to Si FinFET implementation, HTFET based logic circuits (e.g. logic gates, adders) exhibit improved energy efficiency for below 0.5V operation. A sparse prefix tree 32-bit adder with nTFET-only design shows significant energy saving for below 0.6V operation. Various SRAM cell designs based on TFET have been benchmarked considering the impact of TFET characteristics on the SRAM cells stability. Over a wide design space of SRAM cells comparing with Si FinFET implementation, desired read/write noise margin and improved energy efficiency can be obtained by using higher transistor count (8T and 10T) TFET SRAMs. The Schmitt-Trigger-based (10T) TFET SRAM cell for low-V_{CC} operation shows promising performance gain compared to sub-threshold Si FinFET design.

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