Performance Enhancement of InAsSb QW-MOSFETs with *in-situ* H_2 Plasma Cleaning for Gate Stack Formation

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Introduction: Antimonide (Sb) based quantum-well (QW) heterostructures such as InAsSb and InGaSb are of interest for III-V CMOS due to their superior electron and hole transport properties, and ability to be grown on a common metaphoric buffer [1-2]. However, a major challenge towards realizing Sb-based complementary MOSFET technology is the successful integration of a high-κ gate dielectric. Sb-based materials when exposed to the atmosphere readily form complex and defective native oxides which results in Fermi level pining and ineffective surface Fermi level modulation. In this work, we integrate an ultra-thinHfO_2 dielectric with the GaSb/$In_{0.2}Al_{0.8}Sb$/ $InAs_{0.8}Sb_{0.2}$ QW heterostructure (Fig. 1a). Incorporation of *in-situ* H_2 plasma cleaning of GaSb prior to thermal Atomic Layer Deposition (ALD) of HfO_2 results in a HfO_2/GaSb interface with significantly improved electrical quality; we demonstrate a 35% improvement in the sub-threshold slope (SS) over devices that employ *ex-situ* chemical cleaning process.

Device Fabrication: Fig. 1 shows the schematic device structure and band diagram of the $InAs_{0.8}Sb_{0.2}$ QW-MOSFET. The $InAs_{0.8}Sb_{0.2}$ QW structure was grown on a semi-insulating (SI) GaAs substrate with an $Al_{0.8}Ga_{0.2}Sb$ metamorphic buffer using molecular beam epitaxy (MBE). A GaSb cap is utilized to enable the integration of a high-κ gate dielectric while preventing oxidation of the $In_{0.2}Al_{0.8}Sb$ barrier layer. The device structure differs from the $InAs_{0.8}Sb_{0.2}$ QW-MOSFET by Ali *et al.* [1] with respect to the thickness of the as grown GaSb cap layer (6nm in the current device versus 2.5 nm in previous device). The increased GaSb thickness is to ensure that cap is not completely oxidized before surface preparation and deposition of a high-κ dielectric. An initial *ex-situ* etch is used to thin the GaSb cap to 3 nm immediately prior to *in-situ* H_2 plasma cleaning.

As noted before, the GaSb surface is susceptible to the formation of a Sb rich surface with a native oxide composed of Ga_2O_3, Sb_2O_4, and Sb_2O_3 [4] when exposed to the atmosphere. Further, at temperatures > 200°C relevant to ALD high-κ deposition, additional elemental Sb is formed as a result of the reaction between the Sb-oxide and the underlying GaSb surface [5]. These Sb rich oxides are responsible for pinning the Fermi level [1] resulting in poor surface Fermi level movement, and degrades the MOSFET performance. *In-situ* H_2 plasma cleaning removes Sb, Sb_2O_4, and Sb_2O_3 from the GaSb surface, leaving behind a Ga rich surface and an interfacial Ga oxide layer that forms a high quality interface with the HfO_2. The superior interface enables efficient Fermi-level movement and consequently superior charge modulation in the quantum-well (Fig. 2) [3]. Pd/Ti/Pt metallization was used for the source/drain contact formation due to the resilience of Pt to H_2 plasma exposure. Conventional Pd/Pt/Au based contacts degrade upon exposure to H_2 plasma [6]. The fabrication process flow for the QW-MOSFET is detailed in Fig. 3.

Results: The measured split capacitance-voltage (CV) characteristics are shown in Fig. 4. The combination of an *in-situ* H_2 plasma cleaned GaSb cap with a scaled 4.5 nm thick HfO_2 gate dielectric results in higher C_{ox} versus the ex-situ HCl cleaned 1 nm Al_2O_3/10 nm HfO_2 gate stack.Fig. 5 shows the transfer characteristics (I_D-V_G) of the $InAs_{0.8}Sb_{0.2}$ QW-MOSFETs with an L_G=5 μm. The ON current of the long channel MOSFET is 30 μA/μm with a peak G_m of 100 μS/μm and threshold voltage of -0.2V. The SS slope is calculated to be 215 mV/dec. It is evident that the *in-situ* H_2 plasma clean results in a 35% improvement over similar QW-MOSFET devices that used an *ex-situ* HCl clean (SS= 350 mV/dec) [1] (Fig. 9). Fig. 5 shows the corresponding output characteristics (I_D-V_D) exhibiting current saturation at low gate voltages. However, external access resistance dominates I_D-V_D characteristics at high V_G. The access resistance was calculated to be R_{EXT}= 5.8 kΩ-μm (Fig. 7). The effective mobility corrected for access resistance as a function of carrier density is shown in Fig. 8. The *in-situ* H_2 plasma processed MOSFET exhibits a peak mobility of 4,000 cm^2/Vs which represents an increase of 17.5× over Si NMOSFET.

Conclusion: In summary, we have demonstrated a 35% improvement in SS for $InAs_{0.8}Sb_{0.2}$ QW-MOSFET by using *in-situ* H_2 plasma to create a high quality interface between GaSb and HfO_2 over the *ex-situ* cleaned counterpart The resulting $InAs_{0.8}Sb_{0.2}$ QW-MOSFET shows 17.5 times increase in electron mobility over present day silicon MOSFETs.

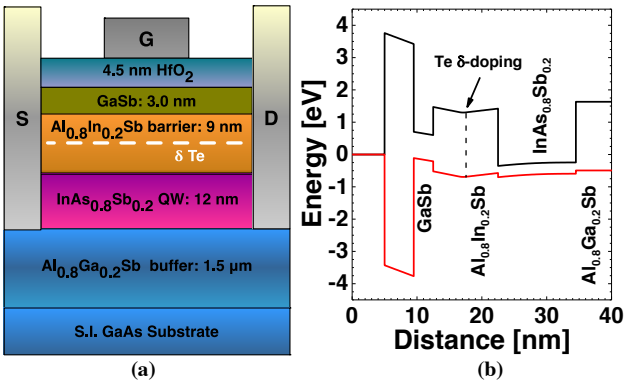

Fig.1: (a) Schematic of InAsSb QW-MOSFET device structure fabricated on semi-insulating (S.I.) GaAs substrate. (b) Corresponding energy band diagram of the quantum well heterostructure simulated using aself-consistent Schrodinger-Poisson solver.

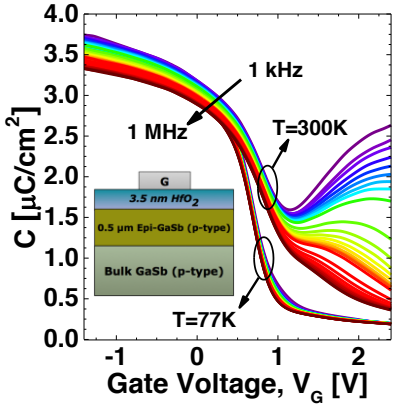

Fig.2: Measured capacitance voltage characteristics of *in-situ* H_2 plasma cleaned Ni / 3.5 nm HfO_2 / GaSb MOSCAP yielding an EOT = 0.8 nm at 300 K and 77K [3].

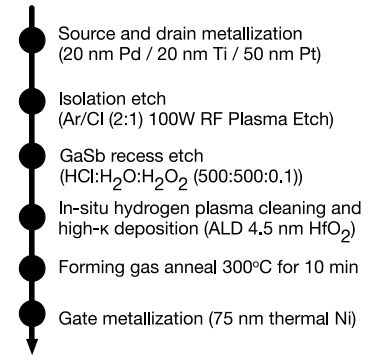

Fig.3: Fabrication process flow for InAsSb QW-MOSFET incorporating *in-situ* H_2 plasma clean of the GaSb surface prior to the HfO_2 deposition.

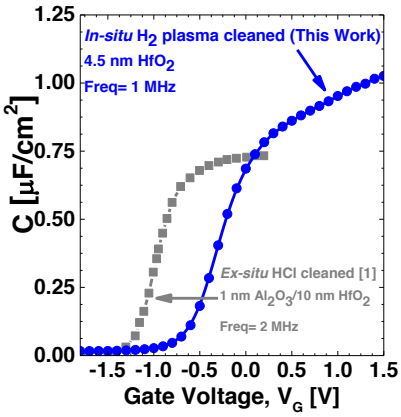

Fig.4: Experimental split C-V characteristics of the InAsSb QW-MOSFET at T=300 K. The *in-situ* H_2 plasma clean results in a higher C_{max} than the C-V characteristics] using *ex-situ* HCl clean [1].

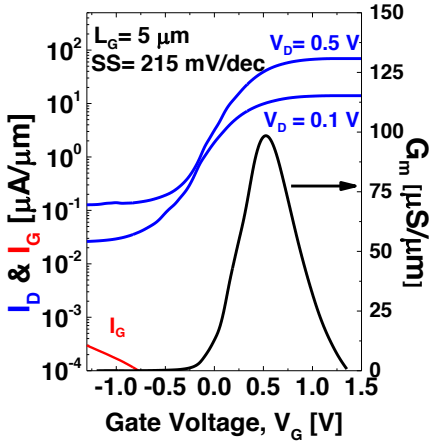

Fig.5: Experimental transfer characteristics (I_D-V_G) of the InAsSb QW-MOSFET with L_G=5 μm at T=300K. The device exhibits a V_T of -0.2V, a I_{ON} of 30.0 μA/μm, a peak G_m of 100 uS/um (V_D=0.5V) and a SS of 215 mV/dec.

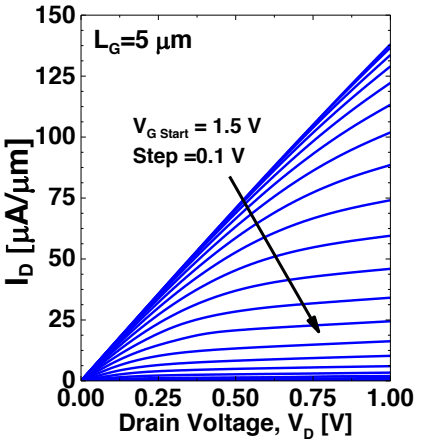

Fig.6: Experimental output characteristics (I_D-V_D) of the InAsSb QW-MOSFET (L_G=5 um) at T=300 K.

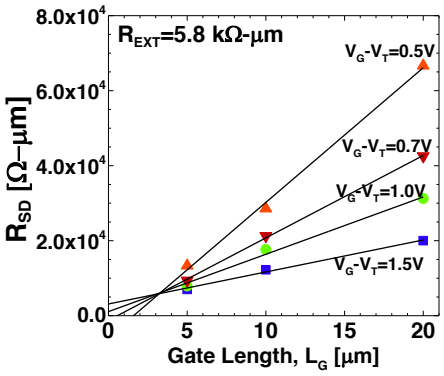

Fig.7: On-state resistance (R_{SD}) of InAsSb QW-MOSFETversus L_G . Access resistance, R_{EXT}, is extracted to be 5.8 kΩ-μm limiting FET performance at high V_G.

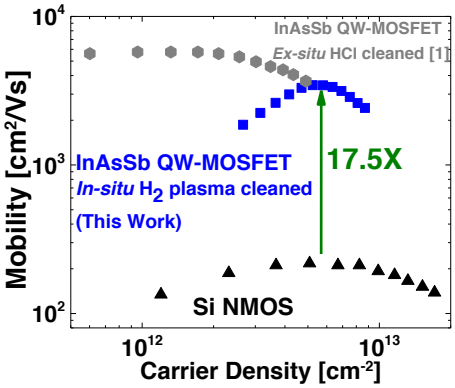

Fig.8: Extracted room temperature effective mobility as a function of carrier density. The mobility has been corrected for access resistance, R_{EXT}.

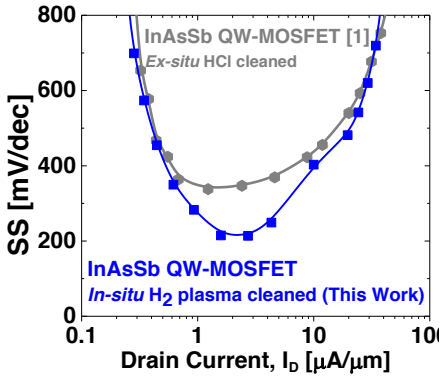

Fig.9: Comparison of SS versus drain current characteristics for L_G=5 μm InAsSb QW-MOSFET using in-situ H_2 plasma cleaning and ex-situ HCl cleaning. The *in-situ* plasma clean results in a 35% improvement in SS.

References: [1] A. Ali et. al., VLSI Technology (VLSIT), 2012 Symposium on, pp.181,182, (2012) [2] A. Nainani, et. al., J. Appl. Physics vol.110, 14503-14509 (2011). [3] M. Barth, et. al Applied Physics Letters 105, 222103, (2014) [4] S. McDonnell, et. al., Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 32, 041201–041201 (2014). [5] G. P. Schwartz,et. al Journal of The Electrochemical Society 127, 2488– 2499 (1980) [6] B. Eren et. al Journal of Physics D: Applied Physics, 47(2), 025302 (2013)