liar kind: the skull hinges against the shoulder girdle, only allowing up-and-down head movement (see **B** in the figure).

The neck region of extant jawed vertebrates contains a distinctive set of neck muscles (*6*). Precursors of hypobranchial muscles (muscles of the tongue and the floor of the mouth) are present in both cyclostomes and placoderms (*7*, *8*). Another major component of the neck muscles is the cucullaris muscle, which stretches between the skull and shoulder blade. The cucullaris is not apparent in the lamprey (*9*) and is thus regarded as defining character of the gnathostome crown group.

By observing the soft tissues preserved in fossil placoderms from Upper Devonian Gogo Formation of West Australia, Trinajstic *et al*. found two pairs of muscles between the skull and dermal shoulder girdle, which was articulated with the skull by a hinge, or neck joint (see **B** in the figure); each of these muscle pairs functioned to depress and elevate the head. The authors argue that these muscles enabled the movement of the head at the hinge between shoulder girdle and skull, and that the depressor is equivalent to the cucullaris in the gnathostome crown group (see **A** in the figure). The muscle differs in both shape and function from the cucullaris of sharks, which is not associated with a hinge joint. Trinajstic *et al*. also note differences in the morphology of segmented trunk muscles in placoderm from those of the shark, as well as the presence of the abdominal transverse-like muscles.

From the developmental perspective, jawed vertebrate muscles are characterized by modification of some rostral trunk muscles to create the "neck." Myoblasts of these neck muscles can migrate over long distances to reach their targets, where they differentiate into various shapes (*10*). This developmental program is particularly elaborated around the time of jaw acquisition, leading to the extensive incorporation of trunk muscles into the head (such as in the case of the human tongue), as well as the acquisition of a highly movable neck. The primitive shoulder girdle in placoderms, as suggested by Trinajstic *et al*., may be an intermediate state of neck evolution that simultaneously reveals the beginnings of a jawed vertebrate novelty, the cucullaris. The presence of the transverse abdominal muscles in placoderms is another mysterious finding of Trinajstic *et al*., because this muscle has been thought to be present only in tetrapods. Phylogenetic importance or homology aside, this muscle is potentially similar to a component of the trunk muscle in tetrapods, the abaxial muscle (*11*), which also develops as the result of myoblast migration and interactions between myoblasts and the embryonic mesenchymal environment of the lateral body wall.

If the muscle patterns reported by Trinajstic *et al*. are found to reflect the general morphology of the placoderms, it would suggest that the developmental bases for the muscle anatomy of modern jawed vertebrates were present, in primitive form, around the time of the appearance of the functional jaw. This would stimulate even greater curiosity about the anatomy of more ancient stem gnathostomes such as ostracoderms, because the beginning of the jawed vertebrate body plan is likely to be buried in the anatomy of these animals.

References and Notes

1. K. Trinajstic *et al*., *Science* **341**, xxxx (2013).
2. P. Janvier, *Early Vertebrates* (Oxford Scientific Publications, New York, 1996).
3. M. D. Brazeau, *Nature* **457**, 305 (2009).
4. S. P. Davis, J. A. Finarelli, M. I. Coates, *Nature* **486**, 247 (2012).
5. G. C. Young, *Biol. Lett.* **4**, 110 (2008).
6. T. Matsuoka *et al*., *Nature* **436**, 347 (2005).
7. S. Sanchez *et al*., *PLoS ONE* **8**, e56992 (2013).
8. Z. Johanson, *J. Vertebr. Paleontol.* **23**, 735 (2003).
9. S. Kuratani, *Dev. Growth Differ.* **50**, (Suppl 1), S189 (2008).
10. C. Birchmeier, H. Brohmann, *Curr. Opin. Cell Biol.* **12**, 725 (2000).
11. A. C. Burke, J. L. Nowicki, *Dev. Cell* **4**, 159 (2003).
12. R. Ericsson, R. Knight, Z. Johanson, *J. Anat.* **222**, 67 (2013).

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ENGINEERING

Nanoscale Transistors—Just Around the Gate?

Advanced geometries for gate electrodes that reduce current leakage can decrease the size of high-performance transistors.

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Further reduction in the size of the metal-oxide semiconductor field-effect transistors (MOSFETs) used in computer chips will require more complex geometries to enhance the gate control of the current flow in the transistor channel (*1*). These advanced designs allow transistor scaling (maintaining performance as size decreases) and minimize the leakage of current when the device is in the off-state. The voltage of operation can be reduced without loss of performance, making the devices function with less power dissipation per operation. The optimal MOSFET geometry surrounds a cylindrical channel with the gate electrode (*2*). This "gate-all-around" (GAA) enhances electrostatic control of the entire channel surface (see the figure), and when used with superior charge transport materials, should deliver enhanced performance. Franklin *et al*. (*3*) now report on nanoscale complementary MOSFETs in which suspended single-walled carbon nanotubes (SWCNTs) form the channel with a GAA geometry. This work marks a milestone in moving SWCNT nanoelectronics from laboratory prototypes toward a manufacturable technology.

The electronic properties of SWCNTs depend on their diameter and chirality. These materials are synthesized as mixtures, but scalable separation methods for electronic type and chirality based on ultracentrifugation (*4*) and column chromatography (*5*) provide monodisperse SWCNT samples with well-defined properties. Franklin *et al*. used substrate-driven growth of horizontally aligned SWCNTs via chemical vapor deposition (*6*–*8*) to create their devices; recently these techniques have been combined to create chirality-controlled, aligned SWCNTs (*9*). This "cloning" method provides a path toward high-yield, high-throughput manufacturing of SWCNT nanoelectronic devices. Electronically, the intrinsic channel region of SWCNTs consists of ballistic conductors displaying length-independent transport at distances below ~50 nm (*10*). The on-current of SWCNT MOSFETs with 9-nm channel lengths exceed that of state-of-the-art Si

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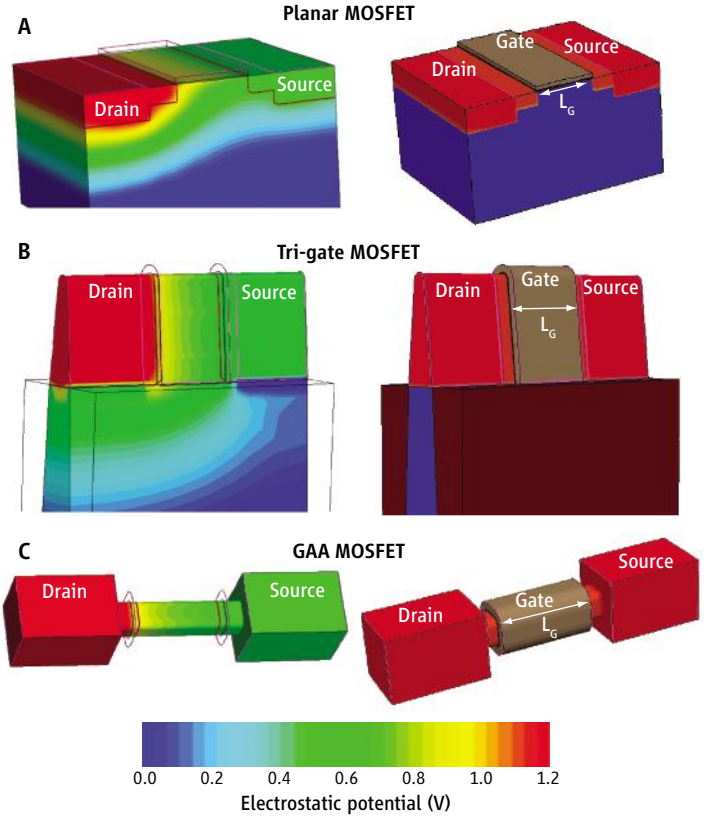
MOSFETs with comparable dimensions (*11*).

Controlling the chirality, alignment, and density of SWCNT channels remains a considerable but surmountable hurdle. The lack of an established technique for controlling the spatial equilibrium carrier density (achieved in many semiconductors by substitutional doping) poses a more fundamental challenge. As intrinsic semiconductors, SWCNT devices rely on work function engineering of electrical contacts that create electron- or hole-blocking Schottky barriers (*12*). Franklin *et al*. achieved complementary MOSFET performance by trapping charge in the gate oxides of their devices, which electrostatically dope the channel to yield predominantly p- or n-channel devices. However, the reliability of this approach remains to be proven along with its compatibility with work function engineering of the metal source and drain contacts.



Optimizing transistor electrostatics. Transistors switch current on and off by modulating the height of an energy barrier that controls the flow of charge carriers through the channel between the source and the drain. Drain-induced barrier lowering (DIBL) is a detrimental short-channel effect that increases the off-state leakage current and drain-bias–dependent threshold voltage. (**A**) The planar n-channel MOSFET depicted here, with n-type contacts and a p-type channel region with a channel length L_G of 26 nm, displays signs of DIBL. The higher electrostatic potential of the drain (1.2 V) extends into the channel toward the source electrode. (**B**) The gate bias in the trigate n-channel MOSFET couples to the channel from three surfaces and reduces the impact of the drain potential on the source side of the barrier. (**C**) The gate-all-around (GAA) geometry further reduces the drain potential spreading, enabling nanoscale transistors with shorter L_G that do not exhibit increases in off-state leakage current.

The GAA geometry is key to achieving optimal electrostatic control, but it is not specific to SWCNT channels; silicon (Si) and alternative high-mobility channel materials, including germanium and compound semiconductors ["III-V" materials such as indium-gallium-arsenide (InGaAs)], are also under investigation. Gate lengths below 15 nm in GAA transistors were achieved with vertical nanowires made by etching Si were recently implemented with metallic source and drain contacts, and displayed an immunity to drain-induced barrier lowering (DIBL; see the figure) with nanowire diameters less than 40 nm (*13*). However, parasitic resistance remains an issue.

Compound semiconductors offer opportunities for independent channel and source-drain engineering for transport enhancement and parasitic resistance reduction, respectively. Tomioka *et al*. (*14*) recently demonstrated position-controlled growth of vertically aligned InGaAs nanowires on Si by selective-area metal-organic vapor-phase epitaxy. Vertical GAA transistors were fabricated by using modulation-doped core–multishell (MD-CMS) nanowire structures in which the device layering is cylindrical rather than planar. These devices exhibit high drive current, transconductance, and excellent gate electrostatics, albeit at a gate length of 200 nm. Aggressive diameter scaling via simplification of the MD-CMS multilayer structure, such as that recently proposed for a III-V trigate transistor by Radosavljevic *et al*. (*15*), needs to be demonstrated in GAA configuration.

Other GAA geometries are possible; Gu *et al*. (*16*) used top-down (lithographic) fabrication techniques to form horizontally aligned InGaAs nanowires stacked vertically, providing an additional degree of freedom to scale on-current independently from the area. This approach may circumvent packing density limitations associated with the vertical nanowire approach, yet self-heating needs to be carefully managed.

The era of nonplanar transistors is upon us as multigate (three-dimensional) transistors have begun to replace planar gate devices in high-performance computing. We expect Si compatibility to drive the choice of non-Si channel material (Ge, III-V, and SWCNTs) to be adopted first. Breakthroughs in crystal growth such as the use of stress-compliant substrates will allow selective growth of high-mobility channel materials on large-area silicon substrates. Different material solutions are likely for n-channel and p-channel devices and will necessitate heterogeneous materials integration at the wafer level. For dielectric barriers, low-temperature atomic-layer deposition and atomic-layer epitaxy techniques will likely be needed to produce passivation layers for non-silicon channel materials that are prone to oxidation. The advantages of the GAA architecture make it the geometry of choice for future generations of MOSFET transistors.

References and Notes

1. M. Lundstrom, *Science* **299**, 210 (2003).
2. The electrode defines the gate length L_G, and the physical spacing between the source and drain junction regions defines the channel length L_C.
3. A. D. Franklin *et al*., *Nano Lett.* **13**, 2490 (2013).
4. M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, M. C. Hersam, *Nat. Nanotechnol.* **1**, 60 (2006).
5. H. Liu, D. Nishide, T. Tanaka, H. Kataura, *Nat. Commun* **2**, 309 (2011).
6. C. Kocabas, M. Meitl, A. Gaur, M. Shim, J. Rogers, *Nano Lett.* **4**, 2421 (2004).
7. S. Han, X. Liu, C. Zhou, *J. Am. Chem. Soc.* **127**, 5294 (2005).
8. A. Ismach, L. Segev, E. Wachtel, E. Joselevich, *Angew. Chem. Int. Ed.* **43**, 6140 (2004).
9. J. Liu *et al*., *Nat. Commun* **3**, 1199 (2012).
10. A. D. Franklin *et al*., Device Research Conference (DRC) **2010**, 275 (2010).
11. A. D. Franklin, A. A. Bol, Z. Chen, IEEE International Electron Devices Meeting (IEDM) **2011**, 23 (2011).
12. Z. Zhang *et al*., *ACS Nano* **3**, 3781 (2009).
13. G. Larrieu, X. L. Han, *Nanoscale* **5**, 2437 (2013).
14. K. Tomioka *et al*., *Nature* **488**, 189 (2012).
15. M. Radosavljevic *et al*., IEEE International Electron Devices Meeting (IEDM) **2011**, 33 (2011).
16. J. J. Gu *et al*., Device Research Conference (DRC) **2012**, 1 (2012).

10.1126/science.1240452