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Low-Temperature Atomic-Layer-Deposited High-κ Dielectric for p-Channel $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ Heterojunction Tunneling Field-Effect Transistor

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The interface quality of a low temperature atomic-layer-deposited (ALD) HfO_2/Al_2O_3 bilayer high-κ gate dielectric on a $GaAs_{0.35}Sb_{0.65}$ channel for heterojunction p-channel tunneling FETs is investigated. Lowering the ALD temperature from 250 to 110 °C results in improved capacitance–voltage characteristics and lower interface trap density in metal–oxide–semiconductor capacitor structures. Using the low-temperature ALD high-κ dielectric, a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterojunction p-channel tunneling FET is demonstrated with an improved switching slope and higher on–off current ratio. X-ray photoelectron spectroscopy is performed to investigate the effect of the deposition temperature on the chemical composition of the high-$\kappa/GaAs_{0.35}Sb_{0.65}$ interface.

Tunneling field-effect transistors (TFETs) can achieve a sub-60 mV/decade switching slope at room temperature and thus enable supply voltage scaling.[1–3] III–V-semiconductor-based heterojunction TFETs are of interest as they allow a high on–off current ratio (I_{ON}/I_{OFF}) and high I_{ON} through reduction in the tunneling barrier height.[4,5] A wide range of tunable effective barrier heights (Eb_{eff}) can be achieved with mixed arsenide-antimonide-based (e.g., Eb_{eff} of 0.25 eV in $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$) heterojunction TFETs. An $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ n-channel hetero-junction TFET was recently demonstrated with a MOSFET-like on current of 135 μA/μm and a high I_{ON}/I_{OFF} ratio of $\sim 10^4$ at a drain bias voltage (V_{DS}) of 0.5 V.[6] Realizing energy-efficient complementary logic circuits requires the development of a high-performance p-channel TFET (pTFET) within the same material system. A major challenge is the integration of the gate stack with acceptably low values of interface state density across the bandgap. Recent efforts have focused on the upper part of the bandgap and the quality of high-κ/III–As compound semiconductor interfaces has been considerably improved by employing surface passivation schemes, such as $(NH_4)_2S$ or NH_4OH solution,[7] in situ As decapping,[8] surface cleaning, and native oxide removal using hydrogen or nitrogen plasma.[9,10] A few studies have reported on the integration of high-κ dielectrics with an antimonide such as GaSb with focus on the lower part of the bandgap between the midgap and the valence band,[11–16] whereas mixed arsenide/antimonides have not been addressed.

In this letter, we study the effect of the temperature used in the atomic layer deposition (ALD) process on the quality of a high-$\kappa/GaAs_{0.35}Sb_{0.65}$ interface. We show that reducing the deposition temperature from 250 to 110 °C results in improved charge modulation of the semiconductor and a reduced interface trap density (D_{it}) response in a metal oxide semiconductor capacitor (MOSCAP), as determined by the Terman method. Furthermore, $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-junction pTFET devices with gate stacks deposited at a low temperature shows an improved I_{ON}/I_{OFF} ratio and switching slope performance.

Epitaxial $GaAs_{0.35}Sb_{0.65}$ layers were grown on a lattice-mismatched InP substrate employing a linearly graded $Al_{1-x}In_xAs$ metamorphic buffer layer grown using solid-source molecular beam epitaxy (MBE). The doping concentration of $GaAs_{0.35}Sb_{0.65}$ is 1×10^{16} cm^{-3}. For MOSCAP fabrication, samples were degreased in acetone and methanol for 5 min each and rinsed in isopropyl alcohol (IPA), followed by a dipping in concentrated HCl solution ($HCl : H_2O = 1 : 1$) for 5 min and an IPA rinse. The samples were then immediately loaded into the ALD chamber and 10 cycles of Al_2O_3 were deposited followed by 35 cycles of HfO_2 at deposition temperatures (T_{dep}) of 250 °C (sample A) and 110 °C (sample B). Pd/Au gate and substrate contact metallization was carried out using electron-beam evaporation after defining gate patterns by electron-beam lithography [Fig. 1(a)]. No postdeposition annealing was performed. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were obtained using a HP 4285A precision LCR meter. X-ray photoelectron spectroscopy (XPS) measurements were carried out using a monochromatic Al Kα X-ray source with a photon energy of 1486.7 eV coupled with a seven-channel hemispherical analyzer operated at a pass energy of 15 eV, with all scans taken at an angle of 45° with respect to the sample normal.

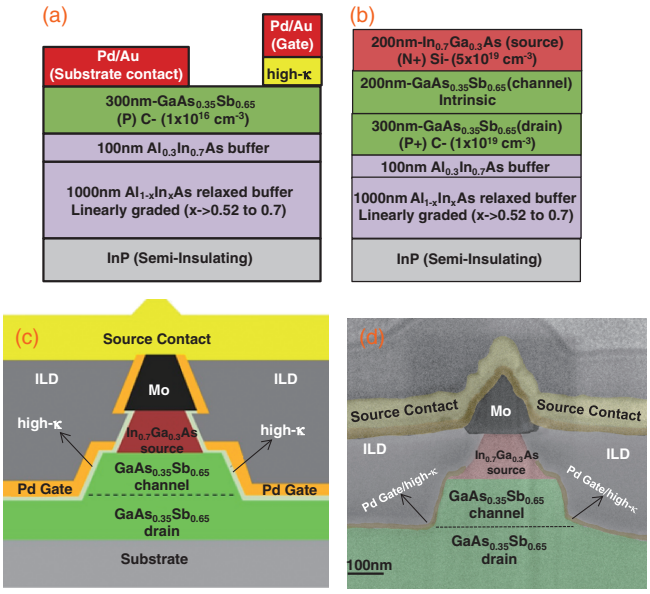

Fig. 1. Schematic of (a) MOSCAP structure, (b) MBE-grown pTFET layer structure, (c) fabricated pTFET using inte-layer dielectric (ILD) to isolate the source and gate contacts. (d) False-colored cross-section SEM of the fabricated pTFET.

AANALYZER software was used to deconvolute the XPS peaks.[17] For XPS measurements, ALD oxide thicknesses were kept at 1 nm for Al_2O_3 and 1.4 nm for HfO_2 for the two deposition temperatures of 250 °C (sample A) and 110 °C (sample B). A heterojunction TFET layer was grown by MBE on a linearly graded $Al_xIn_{1-x}As$ metamorphic buffer to accommodate lattice mismatch to the InP substrate as shown in Fig. 1(b). A self-aligned gate nanopillar process flow was applied for the fabrication of vertical TFETs, as detailed in Ref. 18. Figures 1(c) and 1(d) respectively show the schematic and a false-colored cross-section scanning electron micrograph (SEM) image of the fabricated pTFET. For the gate dielectric deposition, high (250 °C, sample A) and low ALD temperatures (110 °C, sample B) were employed, followed by the self-aligned gate metal deposition process to deposit Pd. The electrical characterization of pTFETs were performed using an HP 4156A parameter analyzer.

Figures 2(a) and 2(b) show the C–V measurements for MOSCAP samples A and B respectively. Sample A showed only a small capacitance modulation with a gate bias at 300 K, indicating strong Fermi level pinning. Despite the strong frequency dispersion at negative gate bias, the C–V characteristics at 150 K are more well-behaved with a smaller minimum capacitance of $C_{min} = 9.5 \times 10^{-8}$ F/cm^2 suggesting larger band bending. However, an ideal minimum capacitance of 3.9×10^{-8} F/cm^2 was calculated, thus the semiconductor was not fully depleted. The enhanced capacitance modulation at 150 K is attributed to two effects: 1) the lower temperature suppresses the D_{it} response and increases the Fermi level movement efficiency; 2) the reduced exponential tail of the electron distribution results in more pronounced carrier modulation and thus enhanced capacitance modulation for a fixed band bending. In contrast, the samples with high-κ deposition at the lower temperatures (sample B) showed much improved C–V characteristics, achieving a much smaller minimum capacitance compared to sample A. The C–V curves are stretched out and have considerable frequency dispersion indicating a high D_{it}. Figures 2(c) and 2(d) show two additional MOSCAP samples with high-κ dielectrics deposited at 80 and at 150 °C, respectively. Higher frequency dispersion and a drop in the C–V curve for a high gate bias due to high gate leakage are observed for the sample with ALD at 80 °C. This is due to the poor quality of the deposited film at the lower deposition temperature. Furthermore, higher stretch-out in the C–V curve is observed in the 150 °C ALD sample in comparison with the 110 °C ALD sample. A deposition temperature of 110 °C was thus found to be optimum. Hence, for further analysis (D_{it} extraction, pTFET fabrication, and XPS analysis), we restrict ourselves to samples A and B which represent a compromise between improved interface quality and reduced dielectric quality, such as leakage and permittivity. We applied the Terman method to quantify the interface trap density D_{it} and band bending for both the samples at 300 K. It is to be noted that the conductance method would severely underestimate the D_{it} response since a D_{it} level larger than $C_{ox}/q \sim 8 \times 10^{12}$ cm^{-2} eV^{-1} is expected in this case.[19] The ideal high frequency C–V curve of $GaAs_{0.35}Sb_{0.65}$ was calculated for 300 K with parameters from Ref. 20 using the approach published in Ref. 21. Light and heavy holes with masses

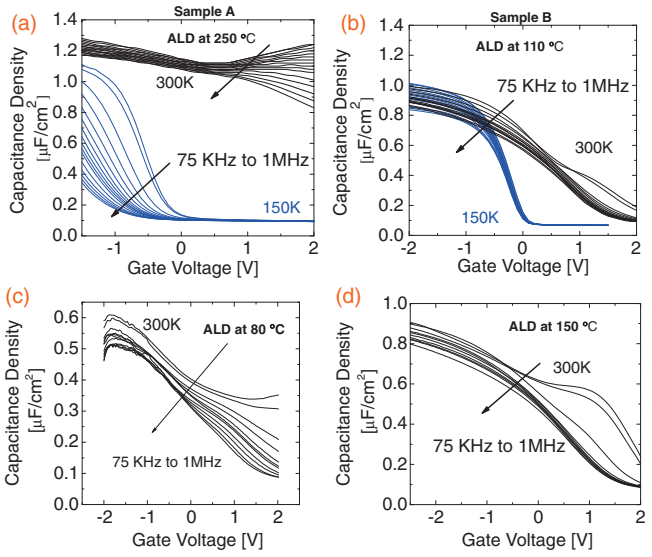

Fig. 2. C–V characteristics of p-type $GaAs_{0.35}Sb_{0.65}$ MOSCAP in the frequency range of 75 kHz to 1 MHz measured at 300 and 150 K with Al_2O_3/HfO_2 deposited at (a) 250 °C (sample A) and (b) 110 °C (sample B). C–V characteristics of p-type $GaAs_{0.35}Sb_{0.65}$ MOSCAP in the frequency range of 75 kHz to 1 MHz measured at 300 K with Al_2O_3/HfO_2 deposited at (c) 80 °C and (d) 150 °C.

$m_{lh} = 0.06m_e$ and $m_{hh} = 0.29m_e$ respectively, where m_e is the free electron mass, were taken into account for the valence band. The effect of split-off band population is small at room temperature due to the large energy offset (0.4 eV) and was therefore neglected. The high-frequency C–V branch at positive gate bias was calculated from Ref. 22. For a p-type dopant concentration of 1×10^{16} cm^{-3}, the flat band condition is met if the Fermi level is 0.17 eV above the valence band edge. Figures 3(a)–3(d) show a comparison between the calculated ideal high frequency and measured 1 MHz C–V curves as well as the extracted band bending and D_{it}. For the MOSCAPs deposited at 250 and 110 °C oxide capacitance densities of 1.4 and 1.1 μF/cm^2 were determined, respectively. For the high-κ dielectric film deposited at 250 °C a total band bending of around 0.12 eV was achieved. The Fermi level barely moved away from the valence band edge and did not reach the flat band at positive gate bias. Therefore, the flat-band voltage shift could not be determined. High D_{it} levels in the low 10^{14} cm^{-2} eV^{-1} range were extracted [inset in Fig. 3(b)]. In contrast, for the MOSCAPs with dielectrics deposited at 110 °C the total band bending considerably improved (0.31 eV) and the flat band condition was reached at a gate bias of 1.1 V. The interface trap density was found to be considerably reduced with typical values in the mid to high 10^{13} cm^{-2} eV^{-1} range [inset in Fig. 3(d)]. The lowest D_{it} value of $\sim 3 \times 10^{13}$ cm^{-2} eV^{-1} was extracted close to the flat-band condition. The Fermi level moved higher into the bandgap reaching close to the midgap. The D_{it} profile extracted by the Terman method suggests that high interface trap densities are still present close to the midgap and at the valence band edge. The low temperature deposition allowed a reduction of the interface trap density within these bounds.

Figure 4(a) shows the measured transfer characteristic (I_{DS}–V_{GS}) of the pTFET at 300 K for V_{DS} of −0.05 and −0.5 V. I_{ON}/I_{OFF} improves from 1×10^2 in sample set A

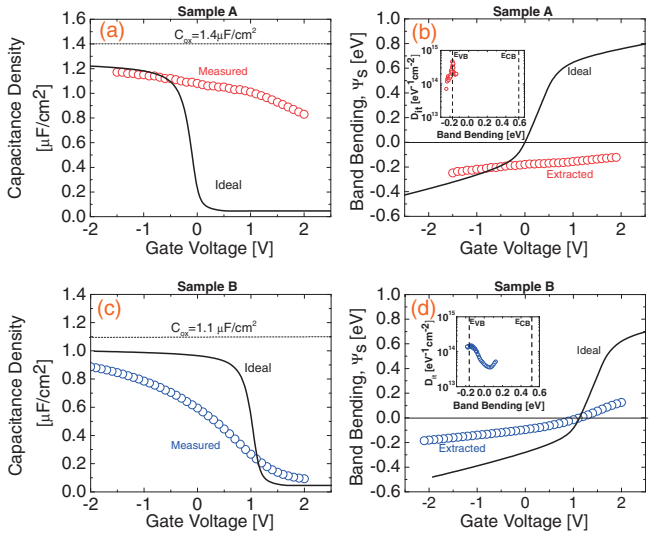

Fig. 3. (a) Comparison of measured (1 MHz) and ideal high frequency C–V curves and (b) ideal and extracted band bending for sample A MOSCAP with Al_2O_3/HfO_2 deposited at 250 °C. (c) Comparison of measured (1 MHz) and ideal high-frequency C–V curves and (d) ideal and extracted band bending for sample B MOSCAP with Al_2O_3/HfO_2 deposited at 110 °C. The insets in (b) and (d) show the interface trap distribution D_{it} for MOSCAPs with the high-κ dielectric deposited at 250 and 110 °C, respectively.

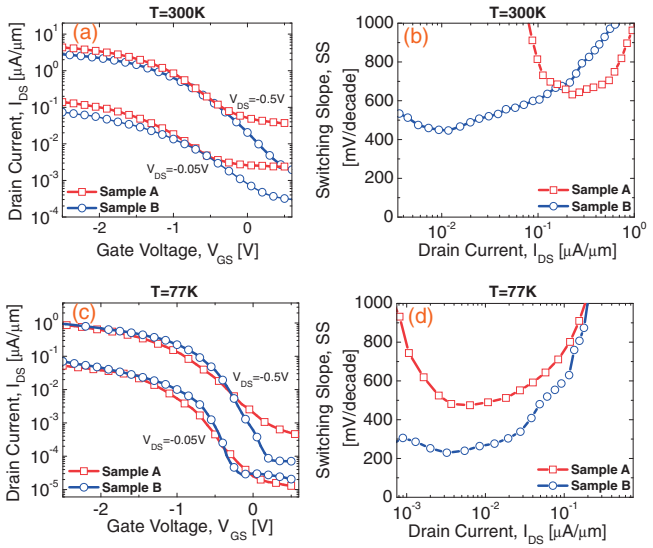

Fig. 4. (a, b) I_{DS}–V_{GS} and SS characteristics of pTFET with Al_2O_3/HfO_2 deposited at 250 °C (sample A, red squares) and Al_2O_3/HfO_2 deposited at 110 °C (sample B, blue circles) for $V_{DS} = -0.05$ and -0.5 V measured at (a, b) 300 K showing improvement in I_{ON}/I_{OFF} and SS with lower deposition temperature, (c, d) 77 K showing improvement in I_{ON}/I_{OFF} and SS due to reduction in SRH leakage floor and suppression of D_{it} response in both samples due to the lower measurement temperature.

(red squares) to 1.5×10^3 in sample set B (blue circles). The improvement in the I_{ON}/I_{OFF} ratio stems from the improved Fermi level movement efficiency achieved in the channel as seen from the C–V analysis [Fig. 3(d)]. I_{ON}/I_{OFF} is expected to increase with further improvement in the Fermi level movement until I_{OFF} is limited by the Shockley–Read–Hall (SRH) generation-recombination current.[23] Comparable I_{ON} is observed in both samples at 300 K [Fig. 4(a)] as expected, as both samples have similar bandbending and D_{it} for high V_{GS} corresponding to the on-state [Figs. 3(b) and 3(d)]. Figure 4(b) shows a comparison of the switching slope characteristics of the two samples at 300 K. Sample B has a minimum SS of 400 mV/decade, compared with 600 mV/decade sample for sample A. Figures 4(c) and 4(d) respectively show the I_{DS}–V_{GS} and SS characteristics measured at 77 K. The lower I_{ON} at 77 K than that at 300 K is due to an increase in the bandgap of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ at 77 K, resulting in changes in the bandalignment at the heterojunction and an increased tunneling barrier height.[23] SS is improved significantly at 77 K in comparison to at 300 K due to the reduction in the D_{it} response as well as due to the reduction in the leakage floor. However, the minimum SS achieved even at 77 K is only 200 mV/decade (sample B). This is due to a lower value of C_{ox} of 1.1 μF/cm^2; with further scaling of the oxide, an improved SS can be achieved.

To better understand the improvement of both MOSCAP and pTFET characteristics using the low-temperature ALD process, the chemical composition at the high-κ/$GaAs_{0.35}Sb_{0.65}As$ interface was investigated using ex situ XPS. Figures 5(a)–5(c) show the high resolution Ga 3d (and Hf 4f), As 3d, and Sb $3d_{3/2}$ core level spectra of the two samples with a high-κ oxide stack of ~1 nm Al_2O_3 and ~1.4 nm HfO_2 deposited at 250 °C (sample A) and 110 °C (sample B). These XPS samples were subjected to the same chemical pretreatment as the MOSCAP structures. Figure 5(a) shows the Ga 3d peak, which is suppressed by the Hf 4f core level. This makes it difficult to estimate the amount of gallium oxides present at the interface. An increased signal from the arsenic and antimony oxidation states was seen for the sample processed at 110 °C [Figs. 5(b) and 5(c), respectively]. Similarly, a large contribution from As–As and Sb–Sb-like states with respect to the bulk As–GaSb and Sb–GaAs components was observed in the case of the lower deposition temperature. The presence of group-V elements and native oxide in sample B, which exhibits better electrical characteristics in the MOSCAP and pTFET, appears counterintuitive. However, the fact that the peak area of the oxides and elemental states is greater in sample B is not an indication that these states are present at the high-κ/GaSb interface. These states may reside closer to the surface of the HfO_2, which was further confirmed by more surface sensitive As 2p spectra (not shown) where arsenic oxidation and As–As states were detected in sample B, while these states were below the XPS detection limit in sample A. The elemental states are most likely to be generated by the decomposition of the native oxides as a result of the "clean-up" effect during the ALD process,[7] which subsequently migrate through the high-κ oxide, with the variation in the deposition temperature and corresponding modifications to the composition of the native oxide also a possible factor.[24] Upon diffusion to the surface through the high-κ stack, these states should oxidize due to atmospheric exposure. The 250 °C ALD temperature in sample A could be sufficiently high to allow for removal of the metallic species from the surface of the HfO_2, and could explain the large variation in native oxide states between the two samples. The fact that the Ga 3d peak profile is very similar for both samples, and there is no detectable signal observed in the more surface-sensitive Ga 2p spectra (not shown), suggests that there is no Ga diffusion to the surface within XPS detection limits in sample A or B, as any Ga

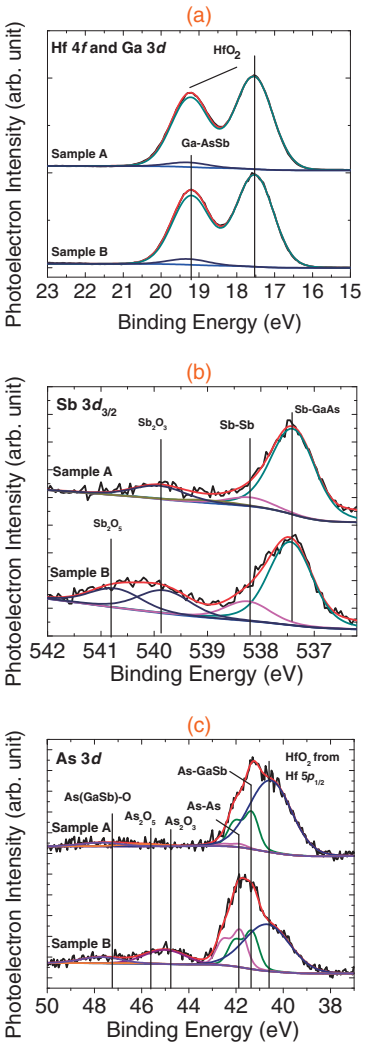

Fig. 5. Ga 3d, As 3d, and Sb $3d_{3/2}$ spectra for Al_2O_3/HfO_2 deposited at 250 °C (sample A) and at 110 °C (sample B) with ~1 nm Al_2O_3 and 1.4 nm HfO_2 showing (a) Ga 3d spectrum suppressed by Hf 4f core level. (b) As 3d showing presence of Asoxide in sample B (c) Sb $3d_{3/2}$ showing high Sboxide content in sample B.

located at the surface of the HfO_2 would be expected to dominate the Ga 3d spectra due to the suppression of the bulk signal by the high-κ oxide overlayer. In addition, the observed trend of the presence of group-V native oxides leading to a better interface is consistent with a reported study on improvement of a dielectric/GaSb interface using low-temperature (200 °C) plasma-enhanced ALD (PEALD) Al_2O_3.[11] In the PEALD GaSb sample, Sboxide was detected at the interface whereas no Sboxide was detected in the ALD sample with the oxide deposited at 300 °C. Further investigation is needed to unambiguously identify the exact surface conditions leading to better dielectric/$GaAs_{0.35}Sb_{0.65}$ interfaces.

In summary, we demonstrated the effect of deposition temperature on the quality of a high-κ/$GaAs_{0.35}Sb_{0.65}$ interface. Lowering the high-κ oxide deposition temperature from 250 to 110 °C significantly improved the characteristics of MOSCAP and pTFET devices, which resulted in larger band bending, a reduced D_{it} response, a larger I_{ON}/I_{OFF} and a reduced switching slope. This is the first demonstration of p-channel heterojunction tunneling FETs in a compound semiconductor material system. XPS measurements show the presence of group-V native oxide, which is in agreement with the reported findings on an improved dielectric/GaSb interface employing low temperature PEALD oxide. Further improvements in the gate dielectric deposition process are needed to enable complementary TFET logic.

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