Correlated Flicker Noise and Hole Mobility Characteristics of (110)/<110> Uniaxially Strained SiGe FINFETs

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Abstract—Hole mobility and flicker noise characteristics of uniaxially strained (110)/<110> Si_{0.75}Ge_{0.25} pFINFETs (SSGOI_{0.25}) are investigated in this letter. Equivalent gate referred flicker noise in SSGOI_{0.25} is dominated by correlated number and mobility fluctuation in the low bias regime and Hooge mobility fluctuation in the high bias regime. The extracted Hooge parameter in SSGOI_{0.25} and in Si pFINFETs is 10^{-5} and 10^{-4}, respectively. Lower value of Hooge parameter in SSGOI_{0.25} pFINFETs is attributed to improved phonon limited mobility compared to the SOI pFINFETs. SSGOI_{0.25} pFINFETs are found to exhibit the lowest equivalent gate referred flicker noise among any non-planar devices reported till date.

Index Terms— Flicker noise, FINFETs, (110)/<110> Uniaxial Strain, SiGe, Hole mobility, Hooge parameter.

I. INTRODUCTION

FINFETs are an attractive replacement for MOSFETs due to their superior electrostatics compared to their planar counterpart [1]. Strain engineered FINFETs provide higher drive current along with smaller channel effects [1]. Uniaxial compressive strain combined with 110 channel orientation with SiGe as the channel material is found to give the best hole mobility enhancement in FINFETs [2]. An important figure of merit for analog and RF devices is the low frequency noise or flicker noise [3] which increases with technology downscaling [4] and is becoming a major concern for analog and RF applications at scaled technology nodes. Thus, it is important to understand the flicker noise characteristics of SSGOI_{0.25} FINFETs and in this letter we present, to the best of our knowledge, the first flicker noise characterization of a SiGe FINFET.

II. FLICKER NOISE CHARACTERISTICS

30nm thick biaxially compressively strained Si_{0.75}Ge_{0.25} layer was epitaxially grown on 10nm thick (100) SOI wafers which, upon patterning, produced uniaxially strained 20nm wide and 40nm tall fins with (110)<110> channel orientation. Silicon fins were also fabricated for comparison. Gate stack comprising of atomic layer deposited (ALD) HfO_{2}/high-κ dielectric,TiN, and poly-silicon gate electrode was deposited followed by nitride spacer formation, source/drain implantation, activation anneal and silicidation. Fig. 1(a) shows the cross-sectional TEM micrograph of SSGOI_{0.25} FINFET. Finite element method simulation study on SSGOI_{0.25} FINFET with a fin length of 10µm shows that, after strain relaxation through amorphized source-drain regions, an average sidewall stress of ~1.6GPa is retained (Fig. 1(b)) which corresponds to a 1% compressive strain.

Noise measurements are performed on SOI and SSGOI_{0.25} pFINFETs with gate length and width of 100 nm and 10 µm, respectively. The DC transfer characteristics have been reported in [2]. The measurement setup consists of a SRS 570 low-noise preamplifier and HP35670A dynamic signal analyzer. All the measurements are done at room temperature and at a constant drain-source bias of -50mV. The drain current noise is converted to the equivalent gate referred noise (\(S_{\text{VG}}\)) by normalizing with the transconductance of the device (Fig. 2(a)). Over a frequency range of 10-100Hz and a gate bias ranging from sub-threshold to strong inversion, the frequency exponent of the flicker noise characteristics is close to 1 indicating that the traps are uniformly distributed from the oxide-channel interface into the oxide [5]. Fig. 2(b) plots \(S_{\text{VG}}\) as a function of gate overdrive voltage (\(V_g - V_t\)). For a given gate overdrive voltage, \(S_{\text{VG}}\) of SSGOI_{0.25} is lower than that of SOI pFINETs. In order to understand the physical mechanisms that determine
the flicker noise performance, the experimentally calculated $S_{f}$ is modeled using different noise models. In SSGOI$_{0.25}$ pFINFETs under low bias, correlated mobility and number fluctuation (CMF) [6] is dominant whereas for high bias the Hooge model becomes dominant (Fig. 2(c)). CMF is modeled using: $S_{v} = S_{o} [1 - a_{o} \cos(V_{g} - V_{t})]^{2}$ where $S_{o} = kTqN_{i}/\gamma Y W L C_{ox}^{2}$, $k$ is the Boltzmann constant, $T$ is the temperature in Kelvin, $N_{i}$ is the interface states density per unit volume, $W$ is the width of the FINFET, $L$ is the length of the FINFET, $C_{ox}$ is the capacitance per unit area, and $Y$ is the attenuation coefficient of the wave function in the oxide. From the WKB theory, $Y = \frac{4\pi/\sqrt{2m_{f}q\phi_{b}}}{h}$ where $h$ is the Planck’s constant, $m_{f}$ is the effective mass in the direction of confinement, and $\phi_{b}$ is the height of the tunneling barrier at the oxide-semiconductor interface. Hooge mobility fluctuation is modeled as: $S_{v} = \frac{\alpha \mu C_{ox}}{W L^{2} t}$ [7] where $\alpha$ is the Hooge parameter, and $\mu_{1}$ and $\mu_{2}$ are the mobility attenuation coefficients. For Si FINFETs the entire gate bias range is modeled using the Hooge model (Fig. 2(d)) and CMF does not play a significant role. Calculated Hooge parameter in SSGOI$_{0.25}$ FINFETs is $10^{-5}$ whereas in Si FINFET the Hooge parameter is $10^{-3}$. In the Hooge model, the flicker noise arises from fluctuations in the phonon limited mobility [8]. For this reason the Hooge parameter is often treated as a material specific parameter and used as a quality metric of the material [9]. Temperature and field dependent mobility study was done to extract the phonon limited mobility component for further examination, as explained in the next section.

Fig. 2. (a) Gate referred flicker noise for both SSGOI$_{0.25}$ and SOI shows slope of close to 1 (b) Comparison of $S_{v}$ as a function of gate over drive voltage shows that SSGOI$_{0.25}$ FINFETs have lower noise levels compared to SOI FINFETs. (c) CMF is dominant in the low gate bias range and Hooge model in the high gate bias range in SSGOI$_{0.25}$ pFINFETs. (d) Hooge model covers the entire gate bias range in SOI pFINFETs.

III. MOBILITY MODELING

Split C-V technique was used to extract the hole mobility. SSGOI$_{0.25}$ exhibits a 57% net enhancement in the hole mobility over SOI FINFETs at sheet carrier density ($N_{s}$) of $1 \times 10^{12}$ cm$^{-2}$ (Fig. 3(a)) at 300K. This enhancement is negated at 77K, due to the presence of alloy scattering mobility enhancement in SSGOI$_{0.25}$ is negated. (c) Excellent agreement between the extracted and fitted mobility values is seen in both SSGOI$_{0.25}$ and SOI pFINFETs. (d) At $N_{s}=1 \times 10^{12}$ cm$^{-2}$ and $T=300$K, the percentage contribution of phonon scattering is smaller in SSGOI$_{0.25}$ than SOI.

Fig. 3. (a) SSGOI$_{0.25}$ FINFETs exhibit 57% enhancement in hole mobility over SOI at $N_{s}=1 \times 10^{12}$ cm$^{-2}$, $T=300$K (b) At $T=77$K, due to the presence of alloy scattering mobility enhancement in SSGOI$_{0.25}$ is negated. (c) Excellent agreement between the extracted and fitted mobility values is seen in both SSGOI$_{0.25}$ and SOI pFINFETs (d) At $N_{s}=1 \times 10^{12}$ cm$^{-2}$ and $T=300$K, the percentage contribution of phonon scattering is smaller in SSGOI$_{0.25}$ than SOI.

Hole mobility extracted across temperatures (77K, 150K, 220K and 300K) was fitted with empirical models which capture the dependence of different scattering mechanisms. In both SOI and SSGOI$_{0.25}$ FINFETs, bulk coulomb scattering is ignored due to low channel doping levels used and remote high-k phonon scattering ignored due to the screening effect by metal gate [10]. The scattering mechanisms considered for modeling SOI pFINFET mobility data are: interface charge scattering [11] ($\mu_{int} \propto N_{s}^{-1.5} V^{-1}$), surface roughness scattering [12] ($\mu_{SR} \propto N_{s}^{1/2}$) and phonon scattering.

Fig. 4. (a) Subthreshold slope as a function of temperature at $V_{ds}=50$ mV shows higher interface states density in SSGOI$_{0.25}$ than SOI. (b) Measured interface state profile via charge pumping measurements.
TABLE I

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[12] (μphonon ≈ T^4.735*Ns^-0.33). For modeling SSGO1.25 FINFET mobility, additional mechanism of alloy scattering [13] (μ_{alloy} ≈ Ns^-0.33) is included. Excellent agreement is seen between measured and modeled mobility values (Fig. 3(c)). Mobility in SSGO1.25 and SOI pFINFETs at 300K and at Ns=1×10^13 cm^-2 is dominated by phonon scattering but its percentage contribution to total mobility is lower in SSGO1.25 compared to SOI pFINFETs (Fig. 3(d)) thus resulting in lower value of Hooge parameter.

Assuming m_e = 2m_0 which is the reported value for (110) <110> biaxially strained SGO1.25 PMOSFET [14] Ns is calculated from $S_{vb}$ as 2×10^18 cm^-3 for SSGO1.25 pFINFETs. Spatial extent of traps into the oxide is calculated to be 1.0 nm [20] and thus the average interface states density per unit area is found to be 2×10^11 cm^-2 which is in reasonable agreement with the Ns value of 5×10^11 cm^-2 calculated from the subthreshold slope as a function of temperature (Fig. 4(a)) and further confirmed from charge pumping measurements (Fig. 4(b)).

IV. CONCLUSION

Table I summarizes the normalized input referred noise spectral density for different non-planar transistors as a function of the oxide thickness and vertical electric field. SSGO1.25 FINFETs exhibit the lowest gate referred flicker noise ($S_{g} * L * W = 6.4 × 10^{-12} \text{ um}^{-1}\text{V}^{-2}\text{Hz}$, $S_{gd}/L^2 * L * W = 4 × 10^{-11} \text{ um}^{-1}\text{V}^{-2}\text{Hz}$) among any non-planar devices reported till date. We conclude that this improvement arises due to: a) reduced interface states at the oxide-SiGe interface resulting in lower $S_g$ at lower gate bias and b) lower value of the Hooge parameter due to improved phonon limited mobility, thus resulting in lower $S_g$ at higher gate bias.

REFERENCES