Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ Near Broken-gap Tunnel FET with I_{ON}=740µA/µm, G_M=700µS/µm and Gigahertz Switching Performance at V_{DS}=0.5V

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Abstract: We demonstrate high frequency switching characteristics of TFETs based on the $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system. These near broken-gap TFETs (NBTFETs) with 200nm channel length exhibit record drive current (I_{ON}) of 740µA/µm, intrinsic RF transconductance (G_M) of 700µS/µm, and a cut-off frequency (F_T) of 19GHz at V_{DS}=0.5V. Numerical simulations calibrated to the experimental data are used to provide insight into the impact of vertical architecture on switching performance of TFETs at scaled technology nodes.

Introduction: TFETs can achieve sub-60mV/decade switching slope (SS) at room temperature thereby enabling supply voltage scaling without penalty on the off state leakage. High band to band tunneling (BTBT) current density can be achieved by band-gap engineering [1-2] and implementing near broken gap tunnel barrier in $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system (Fig. 1(a)). Implementing NBTFETs in a vertical architecture provides added advantage in terms of increased device density [3]. In this work, we demonstrate high frequency switching characteristics of NBTFET, for the first time. Through detailed RF characterization coupled with numerical simulations, an optimal vertical NBTFET structure is designed for DC and RF performance with low DC power consumption.

Materials Characterization: Fig. 1(b) shows the schematic of the NBTFET layer structure grown by molecular beam epitaxy (MBE). Effective tunnel barrier height (Eb_{eff}) of 0.04eV is expected in NBTFET (Fig. 1(c)). Internal photoemission (IPE) spectroscopy is performed to measure the band-alignment of NBTFETs by using graphene as a transparent electrode (Figs. 2(a)-(d)). The barrier height for holes (Φ_h) from the $In_{0.9}Ga_{0.1}As$ conduction band (CB) to the Al_2O_3 valence band (VB) is found to be 3.05eV from the field independent yield plot (Fig. 2(b)). Φ_h for the $GaAs_{0.18}Sb_{0.82}$ CB to the Al_2O_3 VB is measured to be 3.72eV (Fig. 2(c)). Within the limits of measurement accuracy, the effective tunneling barrier (Eb_{eff}) of the NBTFET is determined to be 0.02eV with the band-gap of $GaAs_{0.18}Sb_{0.82}$ of assumed to be 0.69eV [4].

Device Fabrication: Fig. 3(a) shows the schematic of the vertical NBTFET fabricated by using the process flow described in Fig. 3(b). Implementation of inter-layer dielectric (ILD) and via process technology to contact the sidewall gate and bottom source electrodes reduces the parasitic capacitances, enabling evaluation of the switching characteristics of the vertical NBTFET. The high resolution TEM cross-section image of the fabricated NBTFET shows a sidewall tapering angle of 53^0, gate-drain overlap of 120nm and gate-source overlap of 40 nm (Fig. 3(c)).

DC Characterization: Fig. 4(a) shows the temperature dependent transfer (I_{DS}-V_{GS}) characteristics of the NBTFET. The weak observed dependence of I_{ON} on temperature is consistent with the band to band tunneling dominated conduction mechanism (Figs. 4(a)-(b)). The NBTFET exhibits I_{ON}=740µA/µm at V_{GS}=2.5V, V_{DS}=0.5 V. Saturation is observed in the output characteristics at lower V_{GS} range; however, for higher V_{GS}, series resistance affects the saturation characteristics. At T=300K, V_{DS}=0.5V the NBTFET exhibits peak extrinsic DC G_M of 680µS/µm (Fig. 4(c)). Activation energy of 0.21eV is obtained from the Arrhenius plot in Fig. 4(d), which is close to half of the band-gap (E_g) of $In_{0.9}Ga_{0.1}As$ indicating a SRH dominated leakage floor (I_{OFF}). InAs homo-junction p-i-n diodes fabricated for comparison showed significantly lower I_{OFF} (Fig. 4(d)). Hence, the I_{OFF} in NBTFET at T=300 K is attributed to SRH generation-recombination current arising from a high density of defect states.

Pulsed-IV Characterization: Numerical simulation is calibrated with the measured I_{DS}-V_{GS} characteristics at T=300 K, V_{DS}=0.5 V by introducing interface states density (D_{it}) of $5x10^{12}$ $cm^{-2}eV^{-1}$. The electron quasi Fermi level in the channel is obtained from numerical simulation and is found to move from deep inside the CB in the on-state to near mid-gap (MG) as V_{GS} is reduced until bulk leakage currents dominate the electrical characteristics (Fig. 5(a)). 100ns gate pulsing suppresses D_{it} response in the energy range from MG to 0.1eV farther from MG, whereas 1µs gate pulsing suppresses D_{it} response in the energy range only 0.035 eV farther from MG (Fig. 5(b)). Fig. 5(c) shows the I_{DS}-V_{GS} characteristics at V_{DS}=0.5 V for varying gate voltage pulse widths. Fig. 5(d) shows the corresponding SS as a function of drain current. SS is found to improve with faster gate voltage pulsing and further improves with reduction in I_{OFF} (T=77 K) and EOT scaling.

RF Characterization: A coplanar ground-signal-ground (GSG) waveguide structure is used to inject RF signal into the NBTFET (Fig. 6(a)). Fig. 6(b) shows the measured and modeled scattering parameters of NBTFET from 40MHz to 20GHz which are in excellent agreement with each other. Fig. 6(c) shows the measured and modeled small signal current gain, h_{21} as a function of frequency. The 200nm L_{ch} NBTFET exhibits F_T of 10GHz and 19GHz at V_{DS}=0.3V and 0.5V (RF G_M=700µS/µm) respectively. Numerical simulation of the NBTFET structure matched to the HRTEM image is carried out taking into account the various parasitic capacitances and resistances (Figs. 7(a-b)) [3]. Simulated $C_{gs,extrinsic}$ and $C_{gd,extrinsic}$ values are in agreement with the measured values from the RF measurements (Figs. 8(a-d)). $C_{gs,ov}$ and $C_{gd,ov}$ are the dominant parasitic capacitances which when de-embedded result in F_T of 22GHz and 39GHz

at 0.3V and 0.5V V_{DS} respectively (Figs. 9(a)-(b)). Further, gate-drain overlap results in increased gate capacitance ($C_{gg,extrinsic}$) as well as reduced series resistance corresponding to improved G_M. NBTFETs with a gate-drain underlap of 40 nm deliver maximum F_T (Figs. 10(a-b)). Figs. 10(c-e) show the impact of the sidewall tapering angle on the switching performance of TFETs. Increased gate capacitance due to tapering is countered by improved G_M arising from the longer spread of BTBT generated carriers. An optimum tapering angle of 80^0 maximizes F_T. Vertical NBTFET with scaled dimensions (Table I) are found to outperform both the DC and RF performance of 32nm CMOS (Figs. 11 (a-c)).

Conclusion: 200 nm L_{ch} NBTFETs have been demonstrated with record high I_{ON}=740μA/μm, RF G_M=700μS/μm and F_T=19 GHz. Vertical NBTFETs with scaled device dimensions, optimized gate-source overlap, gate-drain underlap, and sidewall tapering angle outperform CMOS in terms of both DC and RF characteristics with lower DC biasing power.

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References: [1] D. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu and S. Datta, *IEDM Tech. Digest*, pp. 33.5.1-33.5.4 (2011). [2] D. Pawlik, B. Romanczyk, P. Thomas, S. Rommel, M. Edirisooriya, R. Contreras-Guerrero, R. Droopad, W-Y Loh, M. H. Wong, K. Majumdar, W.-E Wang, P. D. Kirsch, and R. Jammy, *IEDM Tech. Digest*, pp. 812-814 , (2012) [3] H. Liu, D. K. Mohata, A. Nidhi, V. Saripalli, V. Narayanan and S. Datta, DRC Tech. Digest, pp. 233-234, (2012). [4] I. Vurgaftman, J. R. Mayer and R. Ram-Mohan, J. Appl. Phys. 89, 5815 (2001). [5] P. VanDerVoorn, M. Agostinelli, S.-J. Choi, G. Curello, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, K.-J. Koh, K. Komeyli, H. Lakdawala, J. Lin, N. Lindert, S. Mudanai, J. Park, K. Phoa, A. Rahman, J. Rizk, L. Rockford, G. Sacks, K. Soumyanath, H. Tashiro, S. Taylor, C. Tsai, H. Xu, J. Xu, L. Yang, I. Young, J.-Y. Yeh, J. Yip, P. Bai, and C.-H. Jan, *VLSI Tech. Digest*, pp. 137-138 (2010).

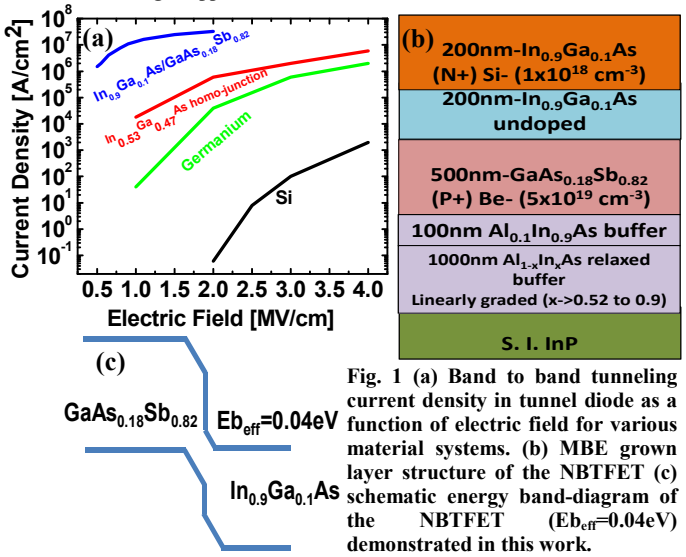


Fig. 1 (a) Band to band tunneling current density in tunnel diode as a function of electric field for various material systems. (b) MBE grown layer structure of the NBTFET (c) schematic energy band-diagram of the NBTFET (Eb_{eff}=0.04eV) demonstrated in this work.

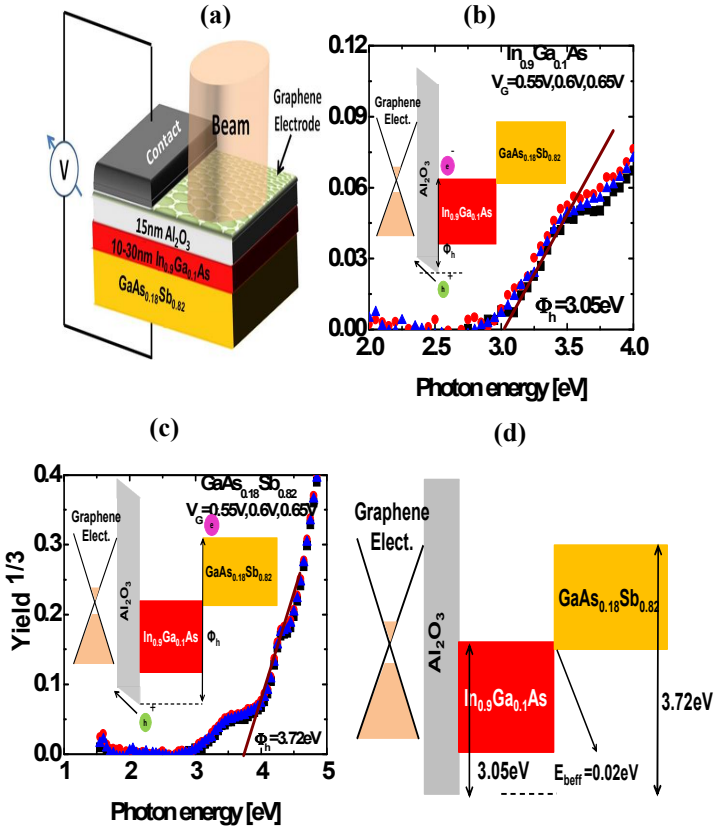


Fig. 2 (a) Internal photo emission spectroscopy experiment setup using graphene as a transparent electrode. (b) Barrier height for hole emission from $In_{0.9}Ga_{0.1}As$ is measured to be 3.05eV. (c) Barrier height for hole emission from $GaAs_{0.18}Sb_{0.82}$ is measured to be 3.72eV. (d) The as-grown NBTFET has an effective barrier height of 0.02eV.

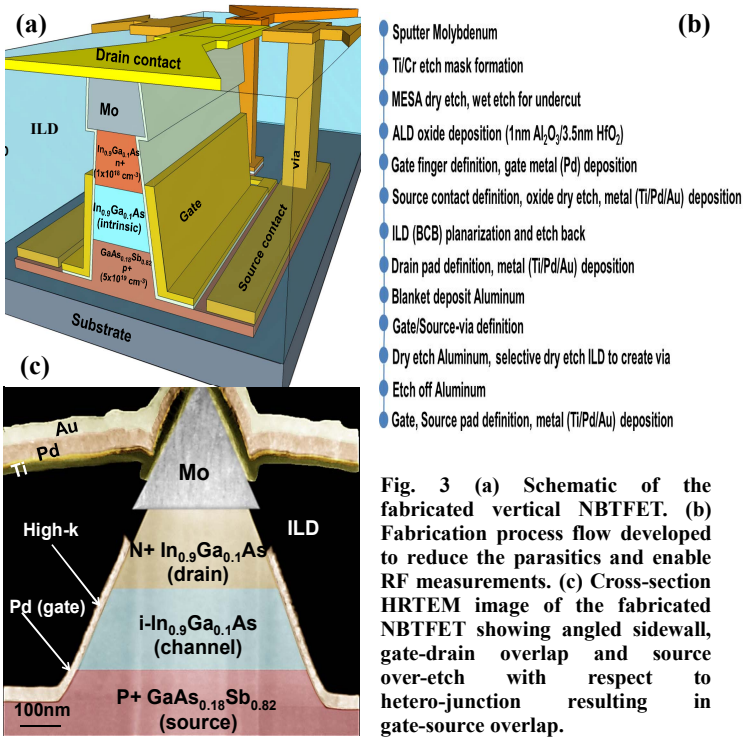


Fig. 3 (a) Schematic of the fabricated vertical NBTFET. (b) Fabrication process flow developed to reduce the parasitics and enable RF measurements. (c) Cross-section HRTEM image of the fabricated NBTFET showing angled sidewall, gate-drain overlap and source over-etch with respect to hetero-junction resulting in gate-source overlap.

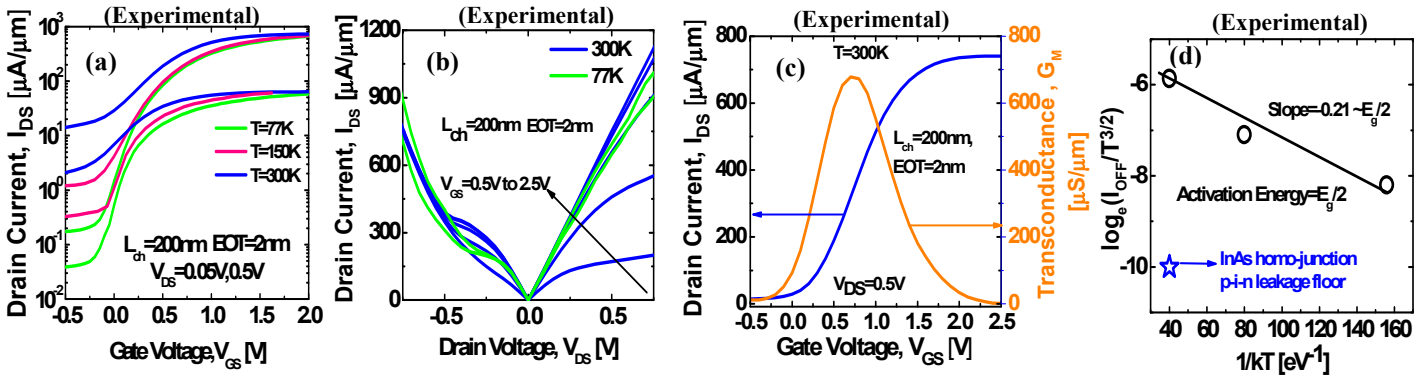


Fig. 4 (a) Temperature dependent transfer characteristics of NBTFET showing improved I_{ON}/I_{OFF} at low temperature. (b) Output characteristics of NBTFET at T=300K and T=77K. (c) NBTFET exhibits peak extrinsic G_M of 680μS/μm at T=300 K, V_{DS}=0.5V. (d) Activation energy of $E_g/2$ confirms SRH generation-recombination in $In_{0.9}Ga_{0.1}As$ as the mechanism setting I_{OFF}. InAs homojunction p-i-n leakage floor at T=300K is much lower in comparison.

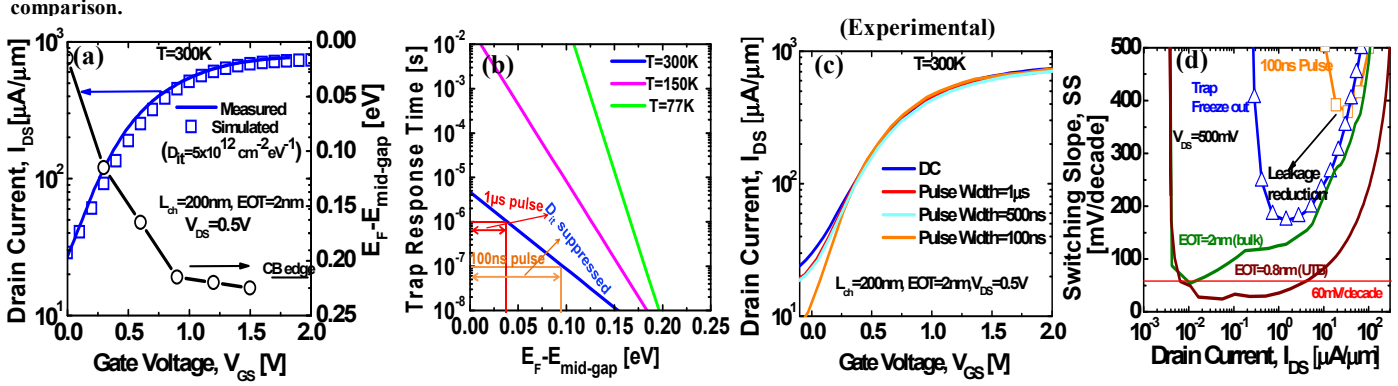


Fig. 5 (a) Numerical simulation calibrated to measured I_{DS}-V_{GS} characteristics at T=300K is used to map the electron quasi-Fermi level movement in the channel (b) Simulated electron trap response time in $In_{0.9}Ga_{0.1}As$ is used to estimate the gate voltage pulse width required to suppress D_{it} response. (c) Transfer characteristics at T=300K, V_{DS}=0.5V for varying gate pulse widths. (d) SS as a function of drain current at V_{DS}=0.5V showing improvement with pulsing, reduction in leakage floor and EOT scaling.

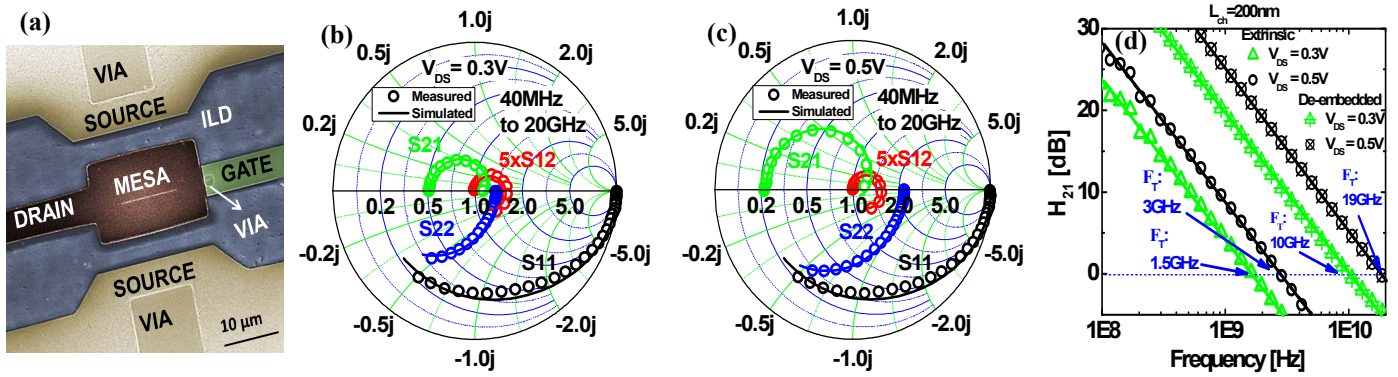


Fig. 6 (a) SEM image of the fabricated NBTFET under GSG configuration. (b-c) Modeled and measured s-parameters at V_{DS}=0.3V and 0.5V respectively. (d) Measured and modeled H_{21} parameter at V_{DS}=0.5V and 0.3V. After de-embedding, F_T of 10GHz and 19GHz are measured at V_{DS}=0.3V and 0.5V respectively. RF G_M=700μS/μm is measured at V_{DS}=0.5V.

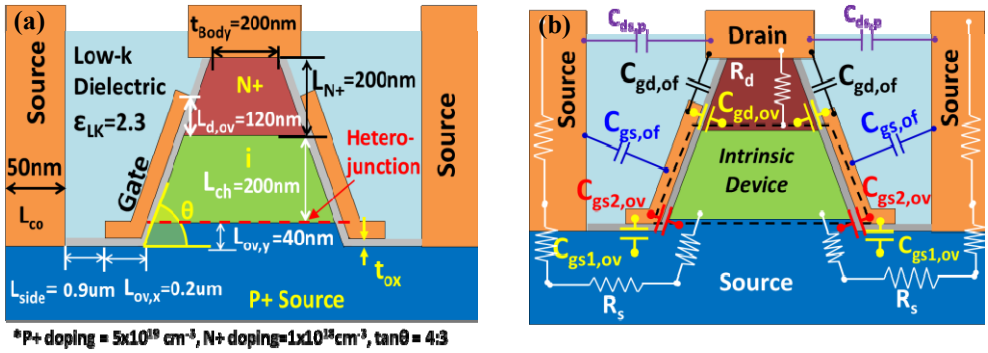


Fig. 7 (a) 2D schematic of the NBTFET used to perform numerical simulation. The geometric parameters were obtained from the HRTEM image of the NBTFET shown in fig. 3(c). (b) Illustration of the parasitic resistances and capacitances taken into consideration for numerical simulation of the NBTFET to evaluate the RF performance.

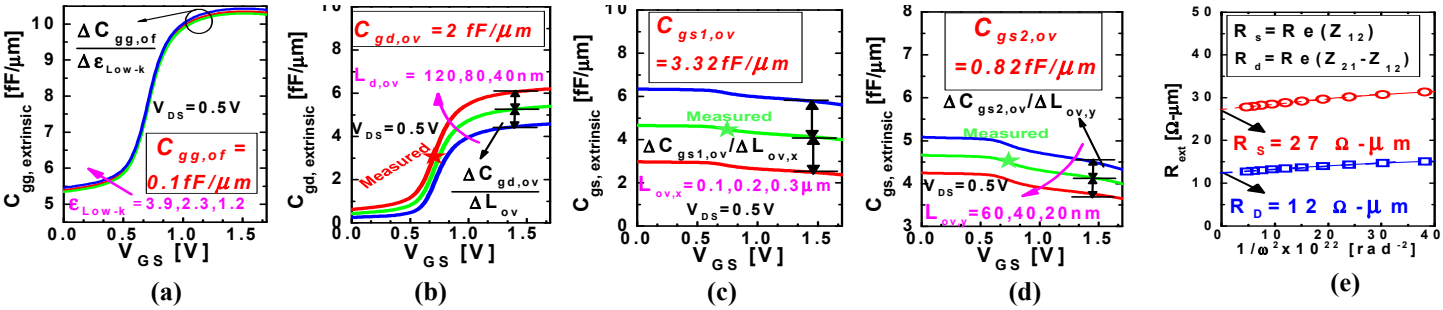


Fig. 8 Extraction of (a) total fringe capacitance $C_{gg,of}$ (b) gate-drain overlap capacitance $C_{gd,ov}$ (c) lateral gate-source overlap capacitance $C_{gs1,ov}$ (d) gate-source overlap capacitance along the sidewall $C_{gs2,ov}$ (e) series resistances R_S and R_D.

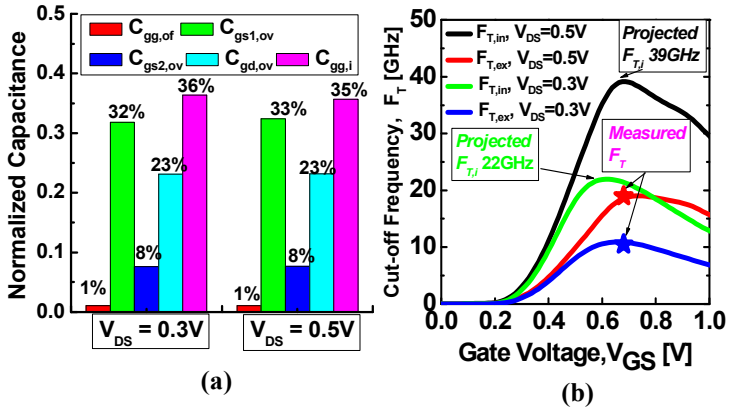
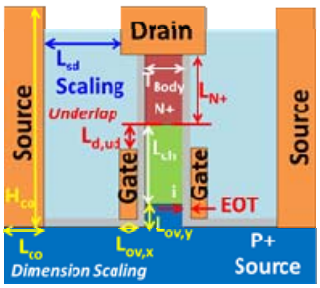


Fig. 9 (a) Percentage contribution of various capacitance components at V_{DS}=0.3V and 0.5V showing the dominance of gate-source and gate-drain overlap capacitances. (b) Measured F_T is in agreement with the simulations. After de-embedding the overlap capacitances, NBTFET with L_{ch}=200nm is expected to achieve F_T of 22GHz and 39GHz at V_{DS}=0.3V and 0.5V respectively.



(a)

L_{ch} (nm)	40nm	20nm	15nm
T_{body} (nm)	5	5	5
EOT(nm)	**0.5**	0.5	0.5
L_{sd} (nm)	100	50	30
$L_{d,ud}$ (nm)	20	10	7
$L_{ov,x}$ (nm)	10	5	5
$L_{ov,y}$ (nm)	5	2	1
L_{co} (nm)	20	10	10
L_{N+}(nm)	40	40	40

Table I-Vertical TFET Scaling Parameters

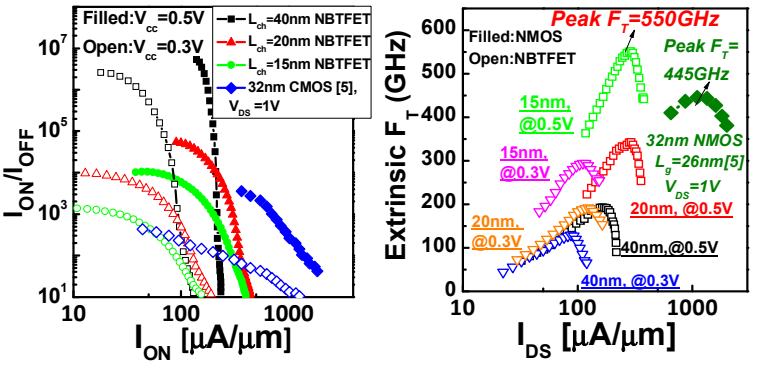
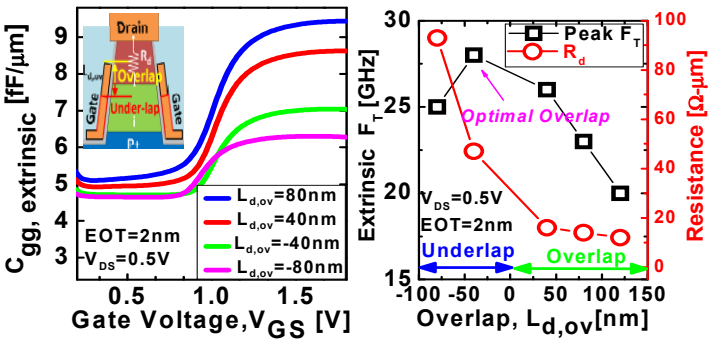
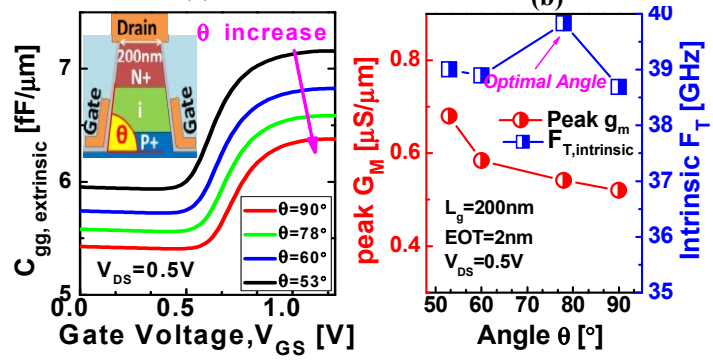


Fig. 11 (a) Schematic of the scaled NBTET, the device parameters are shown in table I. (b) I_{ON} vs I_{ON}/I_{OFF} plot of the NBTFET for different L_{ch} compared to 32nm CMOS. (c) Comparison of the projected extrinsic F_T of NBTFET compared to 32nm CMOS.





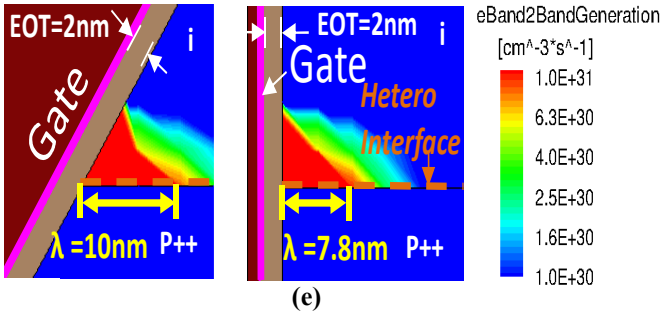


Fig. 10 (a) Extrinsic gate capacitance, C_{gg} as a function of the gate bias showing increase with increasing gate-drain overlap. Inset shows the schematic of the structure simulated (b) The drain side series resistance R_d reduces with increased gate-drain overlap, however due to increase in C_{gg} with gate-drain overlap, overall extrinsic F_T is found to be optimum at underlap of 40nm. (c) C_{gg} as a function of gate bias showing increase in magnitude as the sidewall becomes more tapered. Inset shows the schematic of the structure simulated (d) Peak G_M reduces as the etched sidewall becomes less tapered, with intrinisc F_T optimum corresponding to $\theta=80^0$ (e) The spread in the electron band to band generation rate is higher with a tapered sidewall giving rise to increased peak G_M.