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Insight into the output characteristics of III-V tunneling field effect transistors

Bijesh Rajamohanan,[a] Dheeraj Mohata, Ashkar Ali, and Suman Datta
Department of Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802, USA

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The mechanism of the drain current saturation in the output characteristics of III-V tunneling field effect transistor (TFET) is explained in detail using numerical simulations as well as physics-based analytical models. We clearly identify the impact of the source doping on delayed output saturation, and non-linear turn on behavior observed in the output characteristics of TFET. Our model uses Wentzen-Krammel-Brillouin approximation and considers the exponentially decaying potential profile in the channel. The choice of source doping in III-V p-channel TFET requires tradeoff between maintaining steep switching and delayed saturation voltage which is of importance for complementary TFET logic. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4794536]

With the recent demonstrations of sub 60 mV/decade switching slope (SS) and metal oxide semiconductor field effect transistor (MOSFET) like on-currents at room temperature, III-V tunneling field effect transistor (TFET) has gained tremendous interest as a low supply voltage (V_{CC}) switch for future low power logic applications.[1,2] The demonstrated TFET devices have bulk geometries, and if the device geometry can be scaled to ultra-thin body (body thickness <7 nm), double gate configurations, TFETs possess the potential to replace conventional MOSFET for $Vcc < 0.5$ V.[3] TFET drain current is strongly dependent on the electric field at the source-channel tunnel junction, set by the source doping density (N_S). Source doping affects the transfer and output characteristics of the TFET. The impact of N_S on the transfer characteristics has been established previously using numerical simulations and analytical models.[4–6] However, its impact on the output characteristics and the drain current saturation has not been well understood. Both output and transfer characteristic ultimately determine the gain of a transistor, given by the ratio of transconductance to output conductance, which in turn affects the noise margin of TFET static random access memory (SRAM) circuits.[7]

In this letter, we study the drain current saturation mechanism in $In_{0.53}Ga_{0.47}As$ homo-junction TFETs through physics based analytical models and technology computer aided design (TCAD) simulations employing dynamic non-local tunneling models. We show that the drain current saturation mechanism is intrinsic to any TFET and is fundamentally different from that of a MOSFET. We use Wentzen-Krammel-Brillouin (WKB) approximation for tunneling current generation in our analytical model to explain the output characteristics obtained from TCAD simulations. Our analytical model does not rely on the empirical tunneling current equation which assumes a constant junction electric field,[8–11] rather we assume an exponentially decaying potential profile in the channel. Thus tunneling current is calculated non-locally as a function of position along the tunneling path which is needed to accurately capture the output characteristics. We establish the dependence of the drain current saturation voltage (V_{DSAT}) on N_s using physics-based analytical model and confirmed by TCAD simulations. We further evaluate the dependence of source doping on the switching slope of the device and show that the choice of source doping in a III-V p-channel TFET requires tradeoff between maintaining steep switching and delayed saturation voltage which is of importance for complementary TFET logic.

Fig. 1(a) shows the schematic of the ultra-thin body (UTB) double gate TFET studied in this letter. For simplicity of explanation, we consider $In_{0.53}Ga_{0.47}As$ homo-junction TFET in this work with body thickness (T_{body}) of 7 nm and electrical oxide thickness (EOT) of 1 nm. Simulations of the TFET characteristics are carried out using Synopsis Sentaurus TCAD simulator. Dynamic non-local band to band tunneling model is used to compute the non-local tunneling transitions and hence the current.[12,13]

We define ψ_s as the available energy window for tunneling between the valence band (VB) edge of the source and the conduction band (CB) edge of the channel. As will be discussed later, ψ_s is controlled both by the gate-source and the drain-source potentials. Figs. 2(a) and 2(b) show the simulated output characteristics of the MOSFET and TFET, respectively, at $V_{GS} = 0.5$ V and for two different source doping of $N_s = 5 \times 10^{19}\ cm^{-3}$ and $6 \times 10^{18}\ cm^{-3}$. We define V_{DSAT} to be the drain voltage needed to reach 95% of the peak current. The saturation characteristics of a MOSFET are unchanged by source doping. However, delayed drain current saturation and non-linear turn on are observed in the output characteristics of TFET for lower source doping. As the source doping is increased, the drain current saturation voltage (V_{DSAT}) is seen to reduce progressively as shown in Fig. 2(c). The turn-on at low V_{DS} becomes linear at higher N_s. In order to explain the source doping dependence observed in the output characteristics, we first present an understanding of the saturation mechanism in the homo-junction TFET.

The tunneling current density in a direct band gap homo-junction bulk or UTB TFET can be calculated based on WKB model as[12,13]

[a]Electronic mail: bor5067@psu.edu.

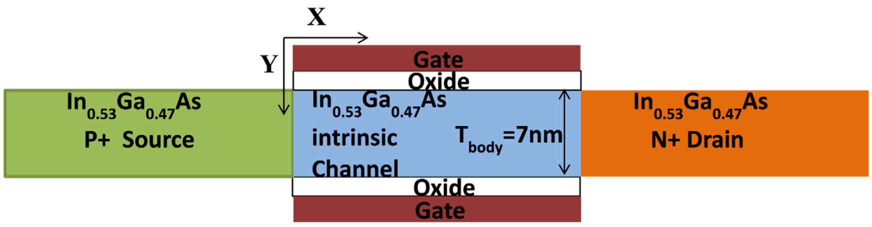

FIG. 1. Schematic of ultra-thin body TFET studied in this letter.

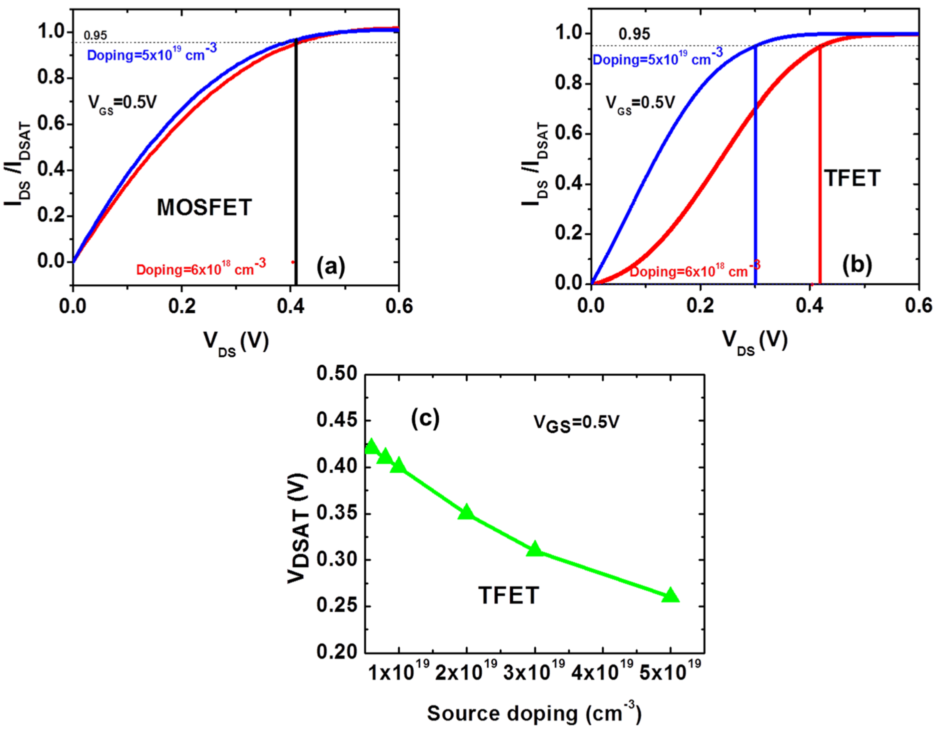

FIG. 2. (a) Simulated output characteristics of $In_{0.53}Ga_{0.47}As$ MOSFET for two values of source doping. (b) Simulated output characteristics of $In_{0.53}Ga_{0.47}AS$ TFET for two values of source doping. (c) V_{DSAT} of TFET as a function of source doping for a fixed V_{GS}.

$$J_{ds} = \int_{\psi_s} \frac{g\pi}{36h} \int_0^l \left(\frac{dx}{k(x)}\right)^{-1} T1(E)T2(E) \times \left[\left(\exp\left[\frac{\varepsilon - E_{F,n}(l)}{kT}\right] + 1\right)^{-1} - \left(\exp\left[\frac{\varepsilon - E_{F,p}(0)}{kT}\right] + 1\right)^{-1}\right] dE, \quad (1)$$

$$T1(E) = \exp\left(-2\int_0^l k(x)dx\right) \text{ and}$$

$$T2(E) = 1 - \exp\left(-k_m^2 \int_0^l \frac{dx}{k(x)}\right).$$

k(x) is the imaginary wave vector in the band gap, g is the degeneracy factor, l is the length of the tunneling path from VB in the source to CB in the channel, E_{Fn} is the Fermi level in the channel, E_{Fs} is the Fermi level in the source. k_m is the maximum transverse (perpendicular) momentum determined by the maximum valence-band energy (ε_{max}) and minimum conduction band energy (ε_{max}) and is given by

$$k_m^2 = \min(k_{vm}^2, k_{cm}^2),$$

$$k_{vm}^2 = \frac{2m_v(\varepsilon_{max} - \varepsilon)}{\hbar^2}, \quad k_{cm}^2 = \frac{2m_c(\varepsilon - \varepsilon_{min})}{\hbar^2},$$

k_{vm} is the maximum transverse momentum in the VB and k_{cm} is the maximum perpendicular momentum in the CB. The perpendicular momentum needs to be conserved in the tunneling process and hence the transmission probability is reduced when k_m is higher.[12,13] Since the tunneling window is defined by ψ_s, it is important to know how the gate and the drain bias influence ψ_s. It has been shown previously that the gate to channel capacitance in a TFET (C_{GG}) is dominated by the gate to drain capacitance (C_{GD}) which leads to enhanced miller capacitance.[14] The enhanced miller capacitance is also found to affect the electrostatics of TFETs as discussed below. Fig. 3(a) shows the simulated energy band diagram of TFET at $V_{DS} = 0$ V. The channel is inverted due to injection of electrons from the drain. At higher drain bias (Fig. 3(b)), due to the large barrier for electrons from the drain into the channel, the net charge in the channel is low. Lower charge in the channel reduces the voltage drop across the oxide and the surface potential in the channel increases. Hence the surface potential in the channel is controlled not only by the V_{GS}, but also by V_{DS}. This is an intrinsic property of TFET and is not related to short channel effects. In MOSFET on the other hand, under high drain bias, gate to source capacitance dominates and the channel is still under inversion due to carriers from the source and the energy barrier for mobile charge injection is controlled by gate alone.[14] Drain current saturation in a long channel MOSFET is due to pinch-off region that is developed near the drain.

The work function of the gate is chosen in such a way that at $V_{GS} = 0$ V the VB in the source and the CB in the

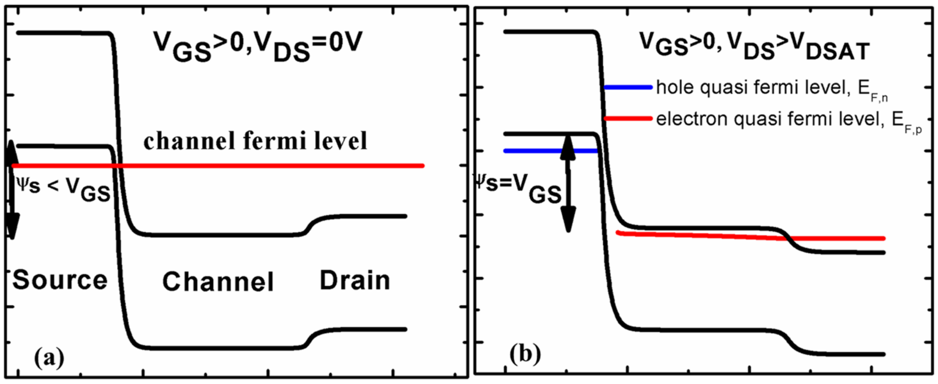

FIG. 3. (a) Energy band diagram of TFET for $V_{DS} = 0$ V showing channel inversion. (b) Energy band diagram at high V_{DS} showing weak inversion of channel due to larger barrier for charge injection from the drain.

channel are aligned. Hence ψ_s is also the surface potential in the channel and $\psi_s = 0$ V for $V_{GS} = V_{DS} = 0$ V. In order to obtain the tunneling window, the change in surface potential of the channel needs to be self consistently calculated as

$$\psi_s(Q_{ch}) = V_{GS} - \frac{Q_{ch}}{2C_{ox}}, \tag{2}$$

$$Q_{ch} = N_c \int_0^{\infty} \frac{\varepsilon^{0.5} d\varepsilon}{1 + \exp(\varepsilon - \eta_F)}, \tag{3}$$

$$\eta_F = \left(\frac{E_{Fch} - E_{Cch}}{kT} \right), \tag{4}$$

where C_{ox} is the gate oxide capacitance, Q_{ch} is the net charge in the channel, N_c is the effective electron density of states of the channel material, E_{Fch} is the electron quasi-fermi level in the channel, and E_{Cch} is the conduction band edge in the channel. The electrons generated in the channel due to tunneling are low compared to the drain injected electrons and ignored in Eqs. (2) and (3).[14] The applied drain bias drops across the tunnel junction and hence E_{Fch} remains flat in the channel and is moved by the amount of applied drain bias. However, beyond V_{DSAT} E_{Fch} is not flat, and V_{DS} drops across the channel (Fig. 3(b)). The maximum surface potential is set by the applied gate bias, and it occurs when the channel is weakly inverted. Fig. 4 shows ψ_s as a function of V_{DS} obtained from numerical TCAD simulations, as well as analytical model discussed in Eq. (2) assuming a flat E_{Fch} in the channel, which are in excellent agreement with each other. Increasing V_{DS} increases the allowed energy window or the available density of states for tunneling and hence the drain current increases. The drain current begins to saturate when the allowed energy window reaches the maximum value set by V_{GS}. For lower source doping, higher V_{DS} is needed to attain the maximum surface potential. The physical explanation for this mechanism is as follows: Under low V_{DS}, the channel is inverted due to injection of electrons from the drain. Thus a p-n junction like built-in potential is formed which is controlled by the source doping and the gate bias. Lower the built-in potential at $V_{DS} = 0$ V, higher is the drain bias needed to increase ψ_S to the maximum value of V_{GS} and TFET enter into saturation. Hence V_{DSAT} is strongly modulated by N_s and V_{GS}.

In order to further confirm the drain current saturation mechanism, we analytically evaluated the tunneling current for the TFET structure shown in Fig. 1 using Eq. (1). Instead of a constant junction field assumption, we assume a realistic potential profile in the channel ψ_{ch} given by

$$\psi_{ch} = \left(\psi_s + \frac{E_g}{q} \right) e^{-x/\lambda},$$

where E_g is the band-gap, λ is the electrostatic scaling length given by $\lambda = \sqrt{\frac{\varepsilon_{ch} t_{body} t_{ox}}{2\varepsilon_{ox}}}$,[9,15] ε_{ch} is the dielectric constant of the channel material, t_{body} is the body thickness, ε_{ox} is the dielectric constant of the oxide, and t_{ox} is the oxide thickness.

We use Flietner's two band relation[16] to determine the imaginary wave vector through the tunneling trajectory as

$$\frac{\hbar^2 k^2}{2m_r} = \frac{E\left(\frac{E}{E_g} - 1\right)}{\left(1 - \alpha + \alpha \frac{E^2}{{E_g}^2}\right)},$$

where m_r is the reduced effective mass given by

$$\frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v},$$

m_c is the effective mass of electrons, m_v is the effective mass of holes, and $\alpha = 1 - \sqrt{m_c/m_v}$.

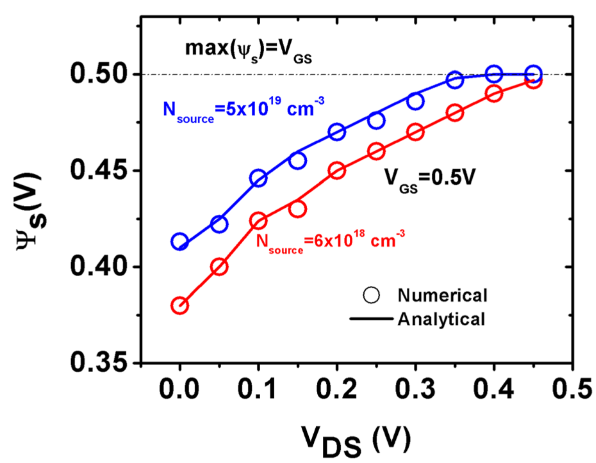

FIG. 4. Simulated and modeled surface potential as function of V_{DS} for two different source doping illustrate delayed saturation.

Only light hole is considered since heavy hole and split off bands contribute to smaller tunneling probability.[17] The tunneling integrals are thus calculated as a function of energy (E) for the UTB TFET as

$$2\int_0^l k(x)dx = \frac{2\lambda\pi\sqrt{2m_r}}{\hbar\sqrt{E_g}}\left[\frac{2\psi_s + Eg - 2E}{2} - \sqrt{\psi_s + Eg - E}\sqrt{\psi_s - E}\right], \quad (5)$$

$$\int_0^l \frac{dx}{k(x)} = \frac{\hbar\lambda\pi\sqrt{E_g}}{\sqrt{2m_r}\sqrt{\psi_s - E}\sqrt{\psi_s + E_g - E}}. \quad (6)$$

Finally, the net drain current is calculated by integration over the cross section of the TFET as $I_{ds} = \iint J_{ds}dA$. The potential in the transverse direction is assumed to be constant due to ultra-thin body dimensions and symmetric double gate. Fig. 5 shows the comparison of simulated and modeled output characteristics. The peak current has been scaled (scaling factor is ∼0.9 for high doping and is ∼0.1 for low doping) to match simulations, and this anomaly could be due to: (a) ignoring the depletion region in the source, (b) assumption of uniform current density throughout the body, (c) approximating $m_c = m_v$ ($\alpha = 1$). Nevertheless, we could capture saturation as well as non-linear turn on seen in simulations for low source doping. Fig. 6(a) shows the different components of transmission probability calculated analytically as a function of energy. We highlight the point that that the factor T1 itself does not result in the non-linear turn on characteristics of TFET as reported in a recent work.[18] In fact, it is the component of transmission probability due to the perpendicular momentum (T2) that results in overall transmission probability to decay towards the band edges (CB in the channel and VB in the source). In the output characteristics this results in low currents for low V_{DS} when the transmission probability is decreased due to the higher magnitude of perpendicular momentum (Fig. 6(b)). Assuming a constant ψ_s for low and high source doping values, it can be seen from Fig. 6(b) that for higher source doping, TFET operates at higher transmission probability for the same energy window, and hence the output characteristic is a linear function. The effect of perpendicular momentum in the transfer characteristics, on the other hand, is to reduce the overall tunneling probability and hence is usually modeled using an increase in the effective bandgap.[19]

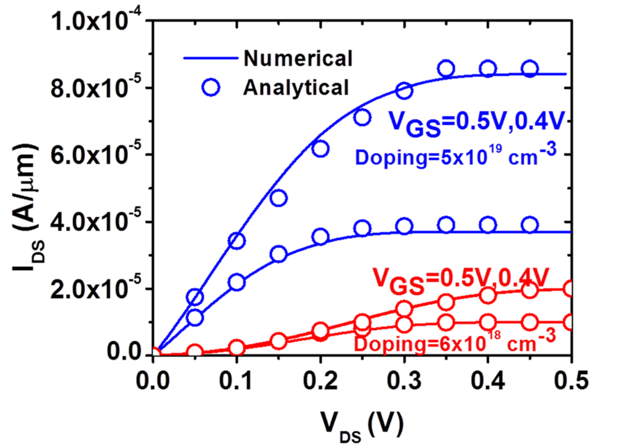

FIG. 5. Modeled output characteristic is in agreement TCAD simulations and capture output saturation and non-linear turn on.

Does this mean that the source doping should be made as high as possible? In this regard, we want to bring focus on p channel TFET (pTFET) where the source is n-type. High values of source doping are required to reduce source depletion and improve the drive current (Fig. 7(a)). However, due to the low density of states in the conduction band, the

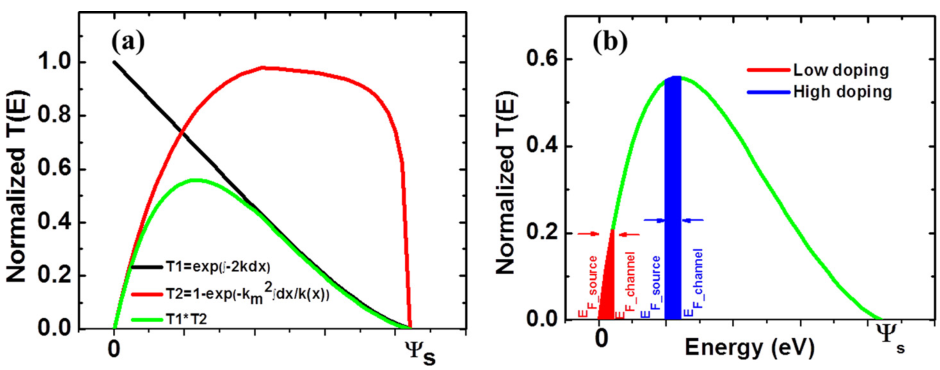

FIG. 6. (a) Impact of perpendicular momentum is to reduce the overall transmission probability towards the band edges. (b) Shaded region indicates the energy range which participates in tunneling under low V_{DS} for two source doping values.

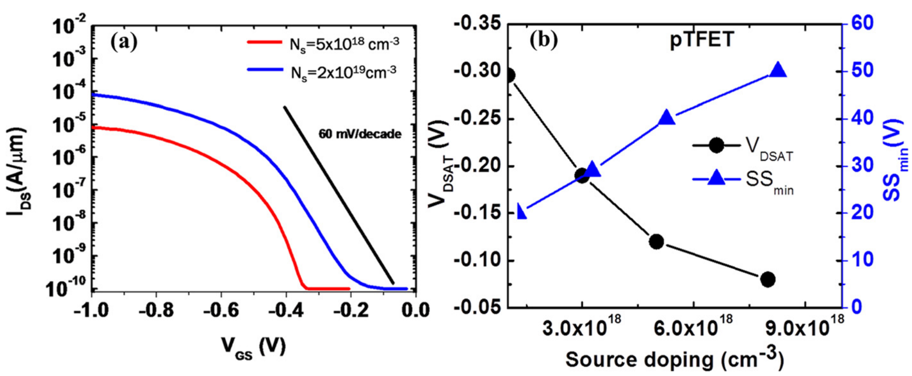

FIG. 7. (a) Simulated transfer characteristics of pTFET which show dependence of SS on the source doping. (b) Lower doping results in steeper switching slope but also results in delayed output saturation.

source is significantly degenerate which can result in to dilution of the expected steep SS (Fig. 7(a)). Thus for III-V p-TFET additional constraint on delayed saturation needs to be addressed due to trade off between V_{DSAT} and SS (Fig. 7(b)). However, this tradeoff is not seen strongly in n channel TFET because the Fermi level has lower sensitivity to source doping arising from the higher effective mass for holes compared to electrons. The impact of delayed saturation is to degrade the voltage transfer characteristics of inverter based on TFET which in turn translates to poor noise margins of TFET based SRAM.[7] Exploring strain and orientation engineering to boost the conduction band of pTFET is a possible solution to circumvent this problem.

In conclusion, we show the impact of source doping on the output characteristics of a III-V TFET. Lower source doping results in delayed saturation as well as non-linear turn on behavior in the I_D-V_D curve. Further, due to low density of states effective mass for electrons in source for pTFET, there is a trade-off between delayed saturation in the output characteristics and the minimum SS achievable.

[1]G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, IEDM Tech. Dig. **2011**, 33.6.1.
[2]D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. Fastenau, D. Loubychev, A. Liu, and S. Datta, IEDM Tech Dig. **2011**, 33.5.1.
[3]M. Luisier and G. Klimeck, IEDM Tech Dig. **2009**, 1.
[4]V. Saripalli, D. K. Mohata, S. Mookerjea, S.Datta, and V. Narayanan, in 68th Annual Device Research Conference (DRC) (IEEE, DRC, 2010), p. 103.
[5]J. Knoch and J. Appenzeller, IEEE Electron Device Lett. **31**, 305 (2010).
[6]M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, IEEE Trans. Electron Devices **57**, 827 (2010).
[7]V. Saripalli, J. P. Kulkarni, N. Vijaykrishnan, and S. Datta, Nanoarch **2011**, 45.
[8]A. S. Verhulst, D. Leonelli, R. Rooyackers, and G. Groeseneken, J. Appl. Phys. **110**, 024510 (2011).
[9]J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, J. Appl. Phys. **110**, 104503 (2011).
[10]B. Bhowmick and S. Baishya, Int. J. Appl. Inf. Syst. **1**, 25 (2012).
[11]K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Sorée, G. Groeseneken, and K. D. Meyer, Solid State Electron **69**, 31 (2012).
[12]*TCAD Sentaurus Device Manual* (Synopsys, Inc., Mountain View, CA, 2010).
[13]E. O. Kane, J. Phys. Chem. Solids **12**, 181 (1960).
[14]S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, IEEE Electron Device Lett. **30**, 1102 (2009).
[15]L. Liu, D. Mohata, and S. Datta, IEEE Trans. Electron Devices **59**, 902 (2012).
[16]H. Fliener, Phys. Status Solidi B **54**, 201 (1972).
[17]K. Ganapathy and S. Salahuddin, J. Appl. Phys. **111**, 124506 (2012).
[18]L. De Michielis, L. Lattanzio, and A. M. Ionescu, IEEE Electron Device Lett. **33**, 1523 (2012).
[19]W. G. Vandenberghe, A. S. Verhulst, K. Kao, K. D. Meyer, B. Soree, W. Magnus, and G. Groesenken, Appl. Phys. Lett. **100**, 193509 (2012).