Correlated Flicker Noise and Hole Mobility Characteristics of $(110)/\langle 110\rangle$ Uniaxially Strained SiGe FINFETs

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***Abstract*—Hole mobility and flicker noise characteristics of uniaxially strained $(110)/\langle 110\rangle$ $Si_{0.75}Ge_{0.25}$ pFINFETs ($SSGOI_{0.25}$) are investigated in this letter. Equivalent gate referred flicker noise in $SSGOI_{0.25}$ is dominated by correlated number and mobility fluctuation in the low-bias regime and Hooge mobility fluctuation in the high-bias regime. The extracted Hooge parameter in $SSGOI_{0.25}$ and in Si pFINFETs is 10^{-5} and 10^{-4}, respectively. The lower value of the Hooge parameter in $SSGOI_{0.25}$ pFINFETs is attributed to improved phonon-limited mobility compared to the SOI pFINFETs. $SSGOI_{0.25}$ FINFETs are found to exhibit the lowest equivalent gate referred flicker noise among any nonplanar devices reported to date.**

***Index Terms*—FINFETs, flicker noise, hole mobility, Hooge parameter, SiGe, $(110)/\langle 110\rangle$ uniaxial strain.**

I. Introduction

FINFETs are an attractive replacement for MOSFETs due to their superior electrostatics compared to their planar counterpart [1]. Strain-engineered FINFETs provide higher drive current along with immunity to short-channel effects [1]. Uniaxial compressive strain combined with 110 channel orientation with SiGe as the channel material is found to give the best hole mobility enhancement in FINFETs [2]. An important figure of merit for analog and RF devices is the low-frequency noise or flicker noise [3] which increases with technology downscaling [4] and is becoming a major concern for analog and RF applications at scaled technology nodes. Thus, it is important to understand the flicker noise characteristics of $SSGOI_{0.25}$ FINFETs, and in this letter, we present, to the best of our knowledge, the first flicker noise characterization of a SiGe FINFET.

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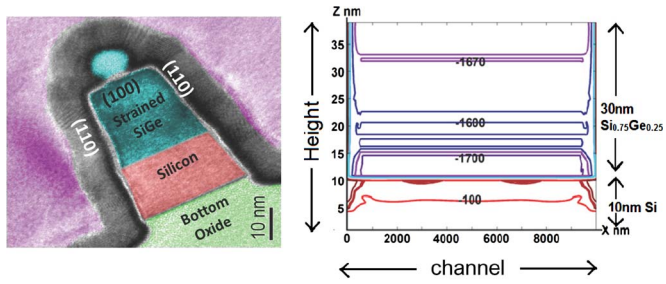

Fig. 1. (a) Cross-sectional TEM micrograph of the SiGe/Si stacked fin under the gate with 30 nm of $Si_{0.75}Ge_{0.25}$ and 10 nm of Si. (b) FEM simulation of 10-μm-long $SSGOI_{0.25}$ pFINFET shows a compressive average sidewall stress of $\sim$1.6 GPa.

II. Flicker Noise Characteristics

A 30-nm-thick biaxial compressively strained $Si_{0.75}Ge_{0.25}$ layer was epitaxially grown on 10-nm-thick (100) SOI wafers which, upon patterning, produced uniaxially strained 20-nm-wide 40-nm-tall fins with $(110)\langle 110\rangle$ channel orientation. Silicon fins were also fabricated for comparison. Gate stack comprising atomic-layer-deposited HfO_2 high-κ dielectric, TiN, and polysilicon gate electrode was deposited followed by nitride spacer formation, source/drain implantation, activation anneal, and silicidation. Fig. 1(a) shows the cross-sectional TEM micrograph of the $SSGOI_{0.25}$ FINFET. Finite-element method (FEM) simulation study on the $SSGOI_{0.25}$ FINFET with a fin length of 10 μm shows that, after strain relaxation through amorphized source–drain regions, an average sidewall stress of -1.6 GPa is retained [see Fig. 1(b)] which corresponds to a 1% compressive strain.

Noise measurements are performed on SOI and $SSGOI_{0.25}$ pFINFETs with gate length and width of 100 nm and 10 μm, respectively. The dc transfer characteristics have been reported in [2]. The measurement setup consists of an SRS 570 low-noise preamplifier and an HP35670A dynamic signal analyzer. All the measurements are done at room temperature and at a constant drain–source bias of -50 mV. The drain current noise is converted to the equivalent gate referred noise (S_{vg}) by normalizing with the transconductance of the device [see Fig. 2(a)]. Over a frequency range of 10–100 Hz and a gate bias ranging from subthreshold to strong inversion, the frequency exponent of the flicker noise characteristics is close to 1, indicating that the traps are uniformly distributed

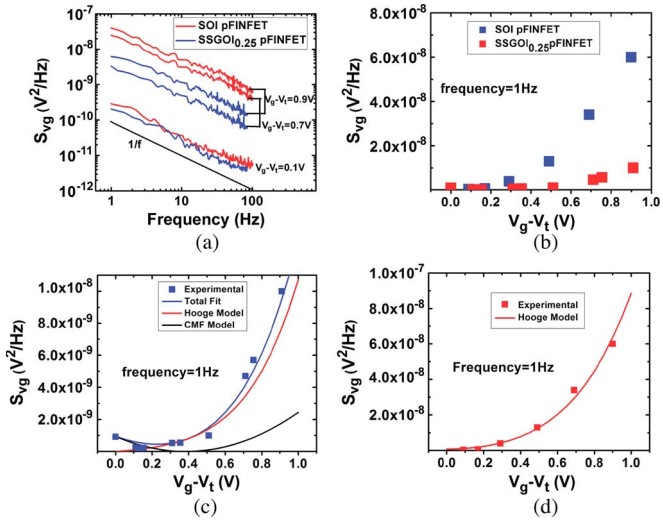

Fig. 2. (a) Gate referred flicker noise for both $SSGOI_{0.25}$ and SOI shows slope of close to 1. (b) Comparison of S_{vg} as a function of gate overdrive voltage shows that $SSGOI_{0.25}$ FINFETs have lower noise levels compared to SOI FINFETs. (c) CMF is dominant in the low-gate-bias range and the Hooge model is dominant in the high-gate-bias range in $SSGOI_{0.25}$ pFINFETs. (d) Hooge model covers the entire gate-bias range in SOI pFINFETs.

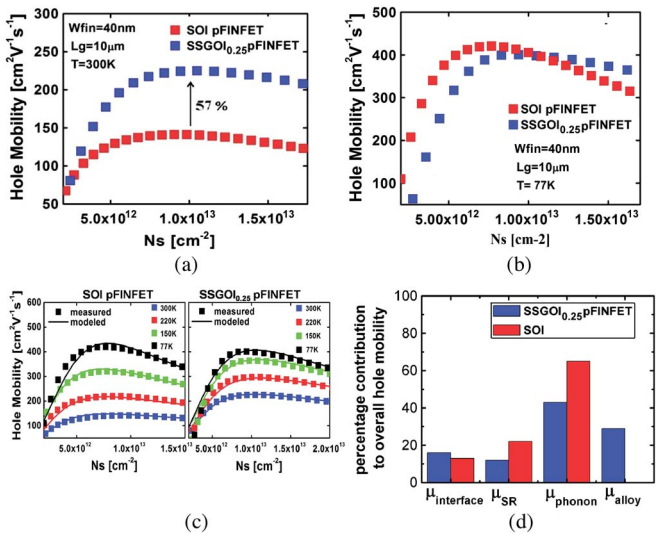

Fig. 3. (a) $SSGOI_{0.25}$ FINFETs exhibit 57% enhancement in hole mobility over SOI at $N_s = 1 \times 10^{13}$ cm^{-2} and $T = 300$ K. (b) At $T = 77$ K, due to the presence of alloy scattering, mobility enhancement in $SSGOI_{0.25}$ is negated. (c) Excellent agreement between the extracted and fitted mobility values is seen in both $SSGOI_{0.25}$ and SOI pFINFETs. (d) At $N_s = 1 \times 10^{13}$ cm^{-2} and $T = 300$ K, the percentage contribution of phonon scattering is smaller in $SSGOI_{0.25}$ than in SOI.

from the oxide–channel interface into the oxide [5]. Fig. 2(b) plots S_{vg} as a function of gate overdrive voltage $(V_g - V_t)$. For a given gate overdrive voltage, the S_{vg} of $SSGOI_{0.25}$ is lower than that of SOI pFINFETs. In order to understand the physical mechanisms that determine the flicker noise performance, the experimentally calculated S_{vg} is modeled using different noise models. In $SSGOI_{0.25}$ pFINFETs under low bias, correlated mobility and number fluctuation (CMF) [6] is dominant, whereas for high bias, the Hooge model becomes dominant [see Fig. 2(c)]. CMF is modeled using the following: $S_{vg} = S_{vfb}[1 - \alpha\mu C_{ox}(V_g - V_t)]^2$, where $S_{vfb} = kTq^2N_{it}/(\Upsilon fWLC_{ox}^2)$, k is the Boltzmann constant, T is the temperature in kelvin, N_{it} is the interface state density per unit volume, W is the width of the FINFET, L is the length of the FINFET, C_{ox} is the capacitance per unit area, and Υ is the attenuation coefficient of the wave function in the oxide. From the WKB theory, $\Upsilon = 4\pi\sqrt{2m_z\varphi_B}/h$, where h is the Planck's constant, m_z is the effective mass in the direction of confinement, and φ_B is the height of the tunneling barrier at the oxide–semiconductor interface. The Hooge mobility fluctuation is modeled as follows: $S_{vg} = (q\alpha_H/WLfC_{ox})(V_g - V_t)[1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2]^2$ [7], where α_H is the Hooge parameter and θ_1 and θ_2 are the mobility attenuation coefficients. For Si FINFETs, the entire gate-bias range is modeled using the Hooge model [see Fig. 2(d)], and CMF does not play a significant role. The calculated Hooge parameter in $SSGOI_{0.25}$ FINFETs is $\sim 10^{-5}$, whereas in Si FINFET, the Hooge parameter is $\sim 10^{-4}$. In the Hooge model, the flicker noise arises from fluctuations in the phonon-limited mobility [8]. For this reason, the Hooge parameter is often treated as a material specific parameter and used as a quality metric of the material [9]. Temperature- and field-dependent mobility study was done to extract the phonon-limited mobility component for further examination, as explained in the next section.

III. Mobility Modeling

Split C–V technique was used to extract the hole mobility. $SSGOI_{0.25}$ exhibits a 57% net enhancement in the hole mobility over SOI FINFETs at sheet carrier density (N_s) of 1×10^{13} cm^{-2} [see Fig. 3(a)] at 300 K. This enhancement is negated at 77 K due to the presence of alloy scattering in $SSGOI_{0.25}$ [see Fig. 3(b)] and also results in a weaker dependence of the hole mobility on N_s. Hole mobility extracted across temperatures (77, 150, 220, and 300 K) was fitted with empirical models which capture the temperature and N_s dependence of different scattering mechanisms. In both SOI and $SSGOI_{0.25}$ FINFETs, bulk coulomb scattering is ignored due to low channel doping levels used, and remote high-k phonon scattering is ignored due to the screening effect by the metal gate [10]. The scattering mechanisms considered for modeling SOI pFINFET mobility data are the following: interface charge scattering [11] $(\mu_{int}\alpha N_s^{-1.6}T^{-1})$, surface roughness scattering [12] $(\mu_{SR} \propto N_s^{-2})$, and phonon scattering [12] $(\mu_{phonon} \propto T^{1.735}Ns^{-0.33})$. For modeling $SSGOI_{0.25}$ pFINFET mobility, the additional mechanism of alloy scattering [13] $(\mu_{alloy} \propto N_s^{-0.33})$ is included. Excellent agreement is seen between the measured and modeled mobility values [see Fig. 3(c)]. Mobility in $SSGOI_{0.25}$ and SOI pFINFETs at 300 K and at $N_s = 1 \times 10^{13}$ cm^{-2} is dominated by phonon scattering, but its percentage contribution to the total mobility is lower in $SSGOI_{0.25}$ compared to SOI pFINFETs [see Fig. 3(d)] thus resulting in the lower value of the Hooge parameter.

Assuming $m_z = 2m_0$ which is the reported value for $(110)/\langle 110\rangle$ biaxially strained $SSGOI_{0.25}$ pMOSFET [14], N_{it} is calculated from S_{vfb} as 2×10^{18} cm^{-3} for $SSGOI_{0.25}$ pFINFETs. The spatial extent of traps into the oxide is calculated to be 1.0 nm [20], and thus, the average interface state density per unit area is found to be 2×10^{11} cm^{-2} which is in reasonable

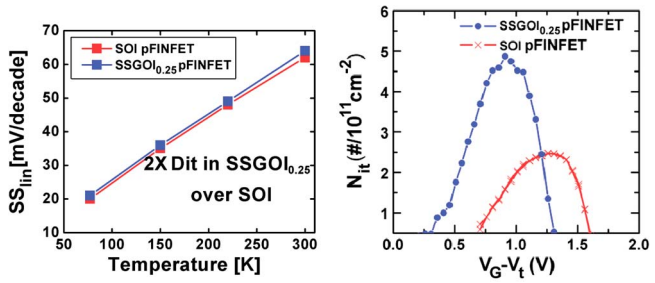

Fig. 4. (a) Subthreshold slope as a function of temperature at $V_{\rm ds} = -50$ mV shows higher interface state density in $\rm SSGOI_{0.25}$ than in SOI. (b) Measured interface state profile via charge pumping measurements.

TABLE I
NOISE BENCHMARK TABLE OF NONPLANAR TRANSISTORS REPORTED TO DATE

	Oxide	EOT (nm)	E=|V_g-V_t|/EOT (V/cm)	S_{vg}*L * W (um^2*V^2/Hz) @10Hz
Si FINFET(this work)	HfO_2	1.3	3×10^6	6.5×10^{-11}
$\rm SSGOI_{0.25}$FINFET (this work)	HfO_2	1.3	3×10^6	6.4×10^{-12}
Si nanowire[15]	SiO_2	4.0	3×10^6	3.34×10^{-11}
InAs nanowire[16]	HfO_2	1.4	3.5×10^6	4.3×10^{-9}
Si FINFET[17]	HfO_2	1.3	5.3×10^6	3×10^{-9}
Si FINFET[18]	HfSiON	1.4	1.5×10^6	1.2×10^{-10}
Si FINFET[19]	SiON	-	2×10^6	1×10^{10}

agreement with the $N_{\rm it}$ value of 5×10^{11} cm^{-2} calculated from the subthreshold slope as a function of temperature [see Fig. 4(a)] and further confirmed from charge pumping measurements [see Fig. 4(b)].

IV. CONCLUSION

Table I summarizes the normalized input referred noise spectral density for different nonplanar transistors as a function of the oxide thickness and vertical electric field. $\rm SSGOI_{0.25}$ pFINFETs exhibit the lowest gate referred flicker noise ($S_{\rm vg} * L * W = 6.4 * 10^{-12}$ um^{2}V^2/Hz, $S_{\rm id}/id^2 * L * W = 4 * 10^{-11}$ um^2/Hz) among any nonplanar devices reported to date. We conclude that this improvement arises due to the following: 1) reduced interface states at the oxide–SiGe interface resulting in lower $S_{\rm vg}$ at lower gate bias and 2) lower value of the Hooge parameter due to improved phonon-limited mobility, thus resulting in lower $S_{\rm vg}$ at higher gate bias.

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