A unified model for insulator selection to form ultra-low resistivity metal-insulator-semiconductor contacts to n-Si, n-Ge, and n-InGaAs

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A unified model for insulator selection to form ultra-low resistivity metal-insulator-semiconductor contacts to n-Si, n-Ge, and n-InGaAs

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A comprehensive, physics-based unified model is developed for study of low resistivity metal-insulator-semiconductor (M-I-S) ohmic contact. Reduction in metal-induced gap state density and Fermi unpinning in semiconductor as a function of insulator thickness is coupled with electron transport including tunnel resistance through the metal-insulator-semiconductor (M-I-S) system to calculate specific contact resistivity at each insulator thickness for n-Si, n-Ge, and n-InGaAs. Low conduction band offset results in $\sim 1 \times 10^{-9}\,\Omega\text{-cm}^2$ contact resistivity with TiO_2 insulator on n-Si, $\sim 7 \times 10^{-9}\,\Omega\text{-cm}^2$ can be achieved using TiO_2 and ZnO on n-Ge, and $\sim 6 \times 10^{-9}\,\Omega\text{-cm}^2$ can be achieved with CdO insulator on n-InGaAs, which meet the sub-22nm CMOS requirements. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4739784]

With the continued scaling of contact dimensions in accordance with Moore's law, the interface resistance between metal and source/drain semiconductor has become a critical area of focus to achieve the required targets for lower external series resistance in a metal-oxide-semiconductor field-effect transistor (MOSFET). Prior studies[1] have shown effective pathways to lower the interface resistance for p-MOSFETs, like the use of narrow bandgap silicon-germanium (SiGe) compounds in source/drain (S/D) regions in silicon channel transistors. In addition, the use of a germanium channel device provides inherent benefit of Fermi-level pinning near the valence band for contacts to p-Ge S/D. Alternative contact architectures are now being sought to improve the interface contact resistance to n-Si (for silicon channel CMOS) and to n-SiGe or n-Ge (for germanium channel CMOS) by reducing the Schottky barrier height (SBH) between metal and n-type S/D semiconductors. The MIS technology to mitigate Fermi level pinning and reduce the contact resistance by inserting interfacial layer between metal and semiconductor was first proposed for Si MOSFETs.[2] Barrier height lowering by means of thin oxides/nitrides was reported for n-Ge with $\rho_C \sim 1 \times 10^{-2}\,\Omega\text{-cm}^2$ (Refs. 3 and 4) was obtained. MIS contact architecture has received intensive focus from academia and industry recently.

Earlier models developed to explain Fermi unpinning by inserting interfacial insulator consider limited aspects. Roy *et al.*[5] considered the effect of tunneling resistance on the achievable minimum contact resistivity but did not account for the effect of metal induced gap state (MIGS) decay quantitatively. The model proposed by Wager and Robertson[6] considered the effect of capacitive division of the metal-semiconductor (M-S) work function difference along with dipole formation between metal/insulator (M-I) and insulator/semiconductor (I-S) interface. However, it did not consider the tunneling transport phenomenon across the M-I-S contact and the effect of insertion of the insulator on the specific contact resistivity.

The goal of this work is to develop a comprehensive, physics based model for quantifying metal-induced gap states in metal-semiconductor interface, identify suitable insulators based on bandgap, dielectric constant, band offset with metal and semiconductor as well as tunneling effective mass and finally, predict the minimum contact resistivity for metal/insulator/n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$ M-I-S contact systems. The quantitative MIGS model is applied in conjunction with electron transport models to calculate current and specific contact resistivity of the M-I-S system.

Fig. 1(a) shows the schematic of energy band structure of a semiconductor in real and imaginary k-space with increasing bandgap. Solution of the Schrodinger's equation for energies in the bandgap thus have complex wave vectors that are spatially decaying.[7] The branch point or the charge neutrality level (CNL) is the energy at which the density of MIGS, D_{MIGS}, as well as the extent of MIGS decay in semiconductor δ is minimum. Fig. 1(b) shows the calculated pinning factor, S as function of semiconductor bandgap. In the inset, the D_{MIGS} and the MIGS penetration depth are also shown as a function of bandgap, which was used to calculate the S factor as discussed by Monch *et al.*[8] For high bandgap semiconductors, the branch point shifts to higher *Im(k)*, leading to rapid decay of MIGS inside the semiconductor, resulting in reduced D_{MIGS} and MIGS depth. The occupancy of MIGS in the bandgap of the semiconductor by charge transfer from metal depends on the extent of metal wavefunction penetration. Inserting a thin insulator between metal and semiconductor attenuates the metal electron wavefunction in the insulator prior to penetrating in the semiconductor. This would result in fewer charges available to drive E_F towards E_{CNL} or, in other words, the exponential reduction in MIGS density as given by[8]

$$D_{MIGS}(t) = D_{MIGS0} \times e^{-2\beta t}, \tag{1}$$

where t is the thickness of the insulator, D_{MIGS0} is the MIGS density at zero insulator thickness or, in other words, for the

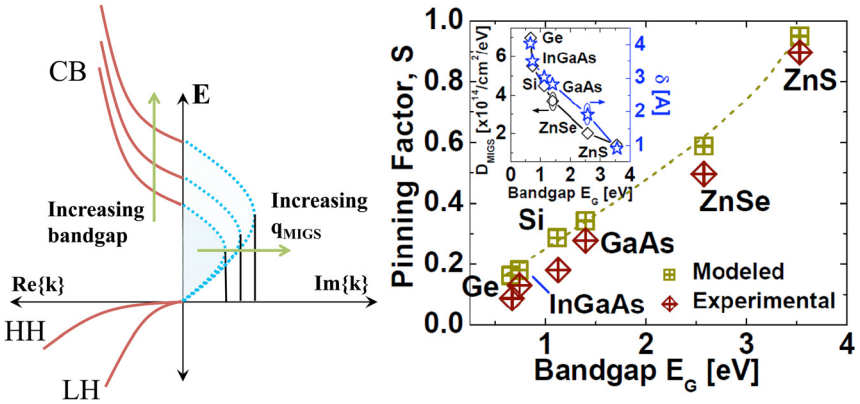

FIG. 1. (a) Schematic of bandstructure with energy in real and imaginary wavevector k domain for increasing bandgap, (b) experimental and calculated pinning factor S vs. semiconductor bandgap for important semiconductors, inset shows D_{MIGS} and MIGS penetration depth δ as function of bandgap. Reducing D_{MIGS} and δ lead to high S factor for large bandgap semiconductors.

metal-semiconductor junction case, β is the rate of decay of the MIGS with increasing thickness and is proportional to the bandgap of the interfacial insulator.

The reduced $D_{MIGS}(t)$ is used to calculate the pinning factor, S as given by

$$S = \frac{1}{1 + \frac{q^2 D_{MIGS}(t)(t+\delta)}{\epsilon_{ins}}}, \tag{2}$$

where δ is the thickness of the interfacial dipole formed for M-S junction case without any interfacial insulator and ϵ_{ins} is the dielectric constant of the insulator. The S factor with the insulator will be higher than that for the metal-semiconductor case, due to the reduction of D_{MIGS}, thereby, resulting in Fermi level unpinning. The effective metal workfunction with respect to vacuum can be calculated from the S factor as

$$\Phi_{Meff} = S\Phi_M + (1 - S)\Phi_{CNL}, \tag{3}$$

where Φ_M is the workfunction of the metal with respect to vacuum and Φ_{CNL} is the energy difference between CNL and vacuum for the semiconductor. The effective SBH between metal and semiconductor with insulator at the interface is given as the difference of the semiconductor workfunction, electron affinity, and the equilibrium surface potential corresponding to the band bending within the semiconductor,

$$\phi_{Bn} = \Phi_S - \chi_S - \psi_S, \tag{4}$$

where the band bending can be written as[6]

$$\psi_S = -\frac{C_I}{C_I + C_S}\Phi_{Meff} - \frac{C_{iS}}{C_{iS} + C_{iI}}\Delta_{IS}, \tag{5}$$

where C_I and C_S are the insulator and semiconductor capacitance densities, respectively, and C_{iI} and C_{iS} are insulator-semiconductor dipole capacitance densities for the insulator and semiconductor, respectively. Equation (5) signifies the capacitive division of the metal-semiconductor work function difference across a series combination of the insulator and semiconductor capacitance densities as well as the division of the insulator-semiconductor dipole voltage across a series combination of the insulator and semiconductor dipole capacitance densities. These capacitance densities are specified by

$$C_I = \frac{\epsilon_I}{t}, \quad C_{iI} = \frac{\epsilon_{\infty I}}{d_{iI}}, \quad C_{iS} = \frac{\epsilon_{\infty S}}{d_{iS}}, \tag{6}$$

where ϵ_I is the insulator dielectric constant, while $\epsilon_{\infty I}$ ($\epsilon_{\infty S}$) and d_{iI} (d_{iS}) are the high-frequency dielectric constant and dipole layer thickness, respectively, of the insulator (semiconductor). d_{iI} was assumed equal to d_{iS} for sake of simplicity. For an n-type semiconductor,[9]

$$C_S(\psi_S) = q\sqrt{\frac{\epsilon_S N_D}{2k_B T}}\left|\frac{e^{\frac{q\psi_S}{k_B T}} - 1 - \left(\frac{n_i}{N_D}\right)^2 e^{\frac{-q\psi_S}{k_B T}}}{\sqrt{e^{\frac{q\psi_S}{k_B T}} - \frac{q\psi_S}{k_B T} - 1 + \left(\frac{n_i}{N_D}\right)^2\left[e^{\frac{-q\psi_S}{k_B T}} - 1\right]}}\right|, \tag{7}$$

where q is the electronic charge, ϵ_S is the semiconductor low-frequency dielectric constant, N_D is the net donor doping density, and n_i is the semiconductor intrinsic carrier concentration. Δ_{IS} is the insulator-semiconductor dipole voltage corresponding to the charge neutrality misalignment, which drops across the insulator-semiconductor interface and is given by

$$\Delta_{IS} = (1 - S_{IS})[\Phi_{CNL,S} - \Phi_{CNL,I}], \tag{8}$$

where S_{IS} is the pinning factor for the I-S interface.

Finally, the calculated Schottky barrier height was used to obtain the total resistivity of the M-I-S contact using either thermionic field emission (TFE) for low-doped semiconductors or field emission (FE) for moderate and high doped semiconductors.[10]

The criteria for selecting the insulator depends on the specific application of the M-I-S system. Since our aim is to employ the M-I-S configuration for source/drain contacts in a MOSFET, an insulator that provides minimum specific contact resistivity for an optimal insulator thickness is desirable. For this purpose, it is essential that the insulator should have minimum conduction band offset with metal and semiconductor, in order to reduce tunnel resistance. The dielectric constant of the insulator should be high, ensuring faster unpinning of the Fermi level with increasing insulator thickness. The bandgap of the insulator should be high, which ensures faster unpinning and that the metal is not pinned at the CNL of the insulator. Since this condition conflicts with the high dielectric constant case, an insulator with lower bandgap but CNL close to conduction band can be chosen.

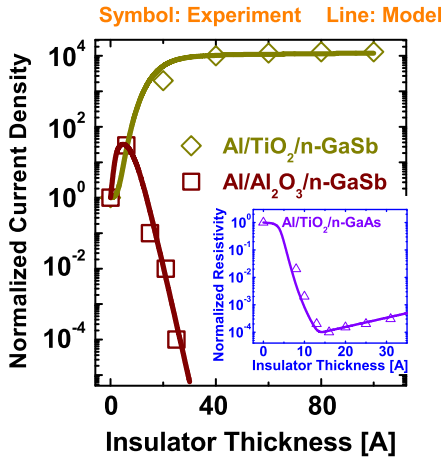

FIG. 2. Experimental and modeled current density ratio for n-GaSb (Ref. 11) as a function of insulator thickness showing excellent agreement between the two. Inset shows experimental and modeled normalized contact resistivity versus insulator thickness for n-GaAs (Ref. 12).

Using the model described above, we study the experimental data on Fermi unpinning by insertion of interfacial insulator between metal and n-GaSb (Ref. 11) and n-GaAs (Ref. 12) semiconductors. Fig. 2 shows the experimental and modeled values for the ratio of the current density with the TiO_2 and Al_2O_3 as insulator to that of the Al-n-GaSb Schottky junction case. Inset shows the experimental and modeled specific contact resistivity ratio for Al-TiO_2-n-GaAs system. Parameters used in the calculations such as Richardson's constant, initial barrier height, conduction band offset between Al/Insulator and insulator/semiconductor have been used as measured or extracted from the experiments from the given references.

Excellent agreement is obtained between the experimental and modeled results as a function of insulator thickness for GaSb and GaAs semiconductors. The physical effects considered so far allow us to reproduce the experimental characteristics with respect to insulator thickness. For Al_2O_3/GaSb case, the depinning effect leads to the initial increase in current density, however the high conduction band offset (CBO) of Al_2O_3 with GaSb (2.4 eV) limits the transport as the thickness of insulator increases, thereby increasing the tunneling resistance of the contact. The optimal thickness was extracted as 1 nm for Al_2O_3. The low CBO (0-0.2 eV) of TiO_2 on GaSb ensures that no excessive tunneling resistance is introduced by increasing TiO_2 thickness up to 7.5 nm, while the depinning effect increases current density by four orders approximately.

Similarly for TiO_2/GaAs system, the specific contact resistivity reduces by four orders of magnitude with increasing TiO_2 thickness upto 1.5 nm, and then gradually increases owing to small CBO (0.1 eV) with GaAs.

The excellent agreement shown above between experimental and modeled results for Al_2O_3 and TiO_2 insulators on n-GaSb and n-GaAs prove the validity of the phenomenological model for Fermi level unpinning.

Using the model developed above, we study different insulators for the purpose of Fermi unpinning in M-I-S structures on n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$ and compute the range of contact resistivity that can be achieved as a function of insulator thickness. Aluminum with a low workfunction of 4.06 eV has been chosen for calculations, since we are investigating contact resistivity for n-type semiconductors.

The choice of insulators was governed by low CBO between Al/insulator and insulator-semiconductor interface and low tunneling effective mass as the main parameters to obtain low contact resistivity along with high bandgap and high dielectric permittivity to achieve faster Fermi unpinning. We selected La_2O_3, ZnS, ZnSe, $SrTiO_3$, ZnO, Ta_2O_5, GeO_2, and TiO_2 for n-Si and n-Ge based on high insulator bandgap and high dielectric constants. In addition, CdO and SnO_2 were selected for n-$In_{0.53}Ga_{0.47}As$ due to high electron affinity compared to Si or Ge. For all simulations, a heavily doped n-Si with doping density of $2 \times 10^{20}/cm^3$, n-type Ge with a doping density of $2 \times 10^{19}/cm^3$ and n-$In_{0.53}Ga_{0.47}As$ with $10^{19}/cm^3$ doping are used. Even though the CNL in InGaAs is 0.2eV below the conduction band edge, poor dopant activation limits the minimum achievable resistivity mandating the need to study Fermi unpinning in InGaAs. The simulation parameters used for different insulators are reported in Table I. $\Delta 1$ and $\Delta 2$ are the CBO between metal-insulator and insulator-semiconductor, respectively. For each insulator thickness, the specific contact resistivity is calculated taking into account the Fermi unpinning leading to reduced SBH and increased tunneling resistance through the insulator. The point of crossover between these two factors provides the optimum insulator thickness for minimum contact resistivity.

TABLE I. Table showing parameters like bandgap, S factor, dielectric constant, tunneling effective mass, electron affinity, and conduction band offset[a] at aluminum/insulator and insulator/semiconductor interface for the selected insulators on Si, Ge, and InGaAs.

Insulator	S	E_{Gap} (eV)	χ (eV)	m* (m_0)	ϵ (ϵ_0)	$\Delta 1$(Al) (eV)	$\Delta 2$(Si) (eV)	$\Delta 2$(Ge) (eV)	$\Delta 2$(InGaAs) (eV)
TiO_2	0.18	3.05	3.05	0.3	80	0.065	0	−0.26	0.51
$SrTiO_3$	0.28	3.3	3.9	0.55	300	0.4	0	0.344	0.4
ZnO	0.52	3.37	4.35	0.27	9	0	0.3	0	0.1
Ta_2O_5	0.4	4.4	3.96	0.3	25	0.38	0.28	0.38	0.95
La_2O_3	0.53	6	1.75	0.26	30	2.3	2.3	2.56	2.93
ZnS	0.91	3.72	3.9	0.367	8.9	0.8	1	0.85	0.8
ZnSe	0.6	2.68	4.09	0.19	8.976	0.4	0.03	1.33	0.4
GeO_2	0.94	6	2.24	0.7	5.8	0.6	—	0.8	—
CdO	0.32	2.16	4.5	0.21	18.1	0	—	—	0
SnO_2	0.54	3.5	4.5	0.273	14	−0.25	—	—	0

[a]Parameters are calculated from Refs. 5 and 13.

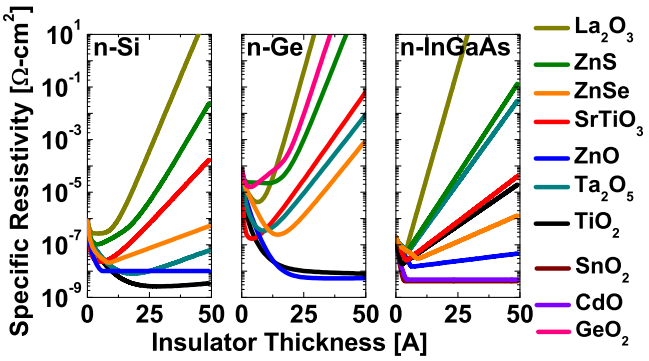

FIG. 3. Calculated specific contact resistivity as a function of insulator thickness for Al/insulator/n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$ with La_2O_3, ZnS, ZnSe, ZnO, TiO_2, Ta_2O_5, $SrTiO_3$, GeO_2, CdO, and SnO_2 as interfacial insulators.

Fig. 3 shows the calculated contact resistivity as a function of insulator thickness for the above mentioned insulators on n-Si. Insulators with high dielectric constant and bandgap such as La_2O_3, ZnS, ZnSe, $SrTiO_3$, and Ta_2O_5, result in faster MIGS decay rate, thereby rapidly unpinning the Fermi level. Minimum resistivity of $10^{-8}\,\Omega$-cm^2 is achieved after which the tunnel resistance increases with increasing insulator thickness due to significant conduction band offset with Al. The minimum resistivity can be obtained with TiO_2 as insulator due to very small CBO $\sim$ 70 meV. Specific contact resistivity as low as $10^{-9}\,\Omega$-cm^2 can be achieved with Al as metal, which is five times lower than contact resistivity of state-of-the-art NiSi/n-Si at same doping.[14]

Similarly, for n-Ge, insulators with significant CBO with Al like La_2O_3, ZnS, ZnSe, GeO_2, $SrTiO_3$, and Ta_2O_5, the specific resistivity increases at $T_{ins} \sim 0.5$ nm and 1 nm, respectively, due to increased tunnel resistance. On the other hand, for ZnO and TiO_2, there is no barrier to the conduction band electrons, and increasing the oxide thickness does not cause a significant increase in the specific contact resistivity as shown in figure. At T_{ins}=1.5 nm, the contact resistivity reduces by four orders of magnitude to a minimum of $10^{-8}\,\Omega$-cm^2 and remains constant with increasing insulator thickness due to zero CBO.

InGaAs, owing to its high electron affinity of 4.5eV, has significant CBO with above insulators, therefore, the minimum contact resistivity is limited to $2 \times 10^{-8}\,\Omega$-cm^2. High electron affinity insulators like CdO and SnO_2 were investigated, resulting in zero CBO with Al and InGaAs. Very low contact resistivity of $6 \times 10^{-9}\,\Omega$-cm^2 can be achieved with CdO as insulator on heavily doped n-$In_{0.53}Ga_{0.47}As$.

Fig. 4 summarizes the minimum achievable specific contact resistivity for the chosen insulators on n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$.

Finally, it is important to note that these results are subject to conditions and assumptions of an ideal interface quality between insulator and semiconductor. Additionally, care needs to be taken to prevent oxidation of Al metal by oxygen in the insulator, this would result in dipole formation shifting the metal workfunction depending on oxygen areal density

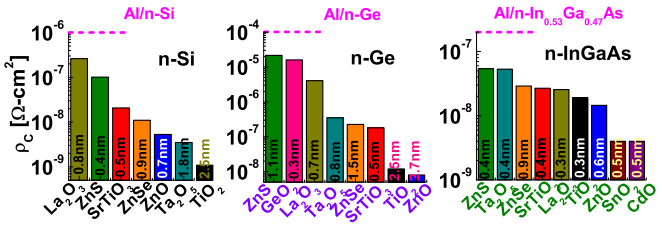

FIG. 4. Summary of minimum specific contact resistivity along with optimal insulator thickness using La_2O_3, ZnS, ZnSe, ZnO, TiO_2, GeO_2, Ta_2O_5, and $SrTiO_3$ insulators on heavily doped n-Si and n-Ge. ZnO and TiO_2 are ideal candidates providing low conduction band offset and high dielectric constant on n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$.

difference between oxidized Al and deposited insulator.[15] A low D_{IT} interface between insulator and semiconductor having interface state density less than $10^{12}/\text{cm}^2$ was assumed. Since current transport through the M-I-S contact is significantly affected by conduction band offset between Al/insulator and insulator/semiconductor, experimental verification needs to be done in order to accurately extract the band offsets.

In conclusion, MIGS-based modeling using a comprehensive, physics-based model in conjunction with electron tunneling model is used to elucidate Fermi level unpinning for low contact resistivity ohmic contacts for n-Si, n-Ge, and n-$In_{0.53}Ga_{0.47}As$ semiconductors. Criteria for insulator selection to achieve minimum specific contact resistivity for ohmic contact formation are discussed. For a n-Si, a 2.5 nm TiO_2 insulator was found to provide the lowest contact resistance of $\sim 10^{-9}\,\Omega$-cm^2. For a n-Ge, a 2.7 nm ZnO film was found to provide the lowest contact resistivity of $\sim 7 \times 10^{-9}\,\Omega$-cm^2. For InGaAs, 0.5 nm CdO was found to provide the lowest contact resistivity of $\sim 6 \times 10^{-9}\,\Omega$-cm^2. Deviations from ideal interfaces could result in higher contact resistivity than what is predicted in this work. However, these low values of resistivity put the M-I-S system in compatibility with integration with mainstream CMOS for source/drain applications.

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