

Benchmarking of Novel Contact Architectures on Silicon and Germanium

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Novel contact architectures to *n*-Silicon (***n*-Si**) and to *n*-Germanium (***n*-Ge**) were benchmarked for the first time against the state-of-the-art contact architecture to ***n*-Si**. It was found that although the recently reported contact architectures to ***n*-Ge** exhibit markedly improved performance, more work must be done to match state-of-the-art NiSi/***n*-Si** contact architecture in terms of current-carrying capability.

With the continued scaling of contact length in accordance with Moore's law, the interface resistance between metal and semiconductor has become a critical area of focus to achieve the required targets for lower external series resistance (Fig. 1, Fig. 2). Prior studies have shown effective pathways to lower the interface resistance for *p*-MOSFETs, like the use of narrow bandgap Silicon-Germanium (**SiGe**) compounds in Source/Drain (***S/D***) regions in silicon channel transistors. In addition, the use of a Germanium channel device provides inherent benefit of Fermi-level pinning near the valence band for contacts to ***p*-Ge *S/D***. Alternative contact architectures are now being sought to improve the interface contact resistance to ***n*-Si** (for Silicon channel CMOS) and to ***n*-Ge** (for Germanium channel CMOS) by reducing the Schottky Barrier Height (**SBH**) between metal and *n*-type *S/D* semiconductors. In this work, a metric which is based on current density (***J***) at given semiconductor doping density (***N_D***) was found to be most suitable for benchmarking contact architectures of widely varying maturities.

Metal-Insulator-Semiconductor (**MIS**) contact architecture, in contrast to current Metal-Semiconductor (**MS**) architecture, has been proposed to reduce **SBH** by unpinning the Fermi level [1-2]. There is a concern, however, that the insertion of a high bandgap oxide results in large tunnel resistance and would offset the positive effect of Fermi level unpinning. It is therefore necessary to benchmark the current-carrying capability of the **MIS** contact architectures on both ***n*-Si** and ***n*-Ge** with respect to state-of-the-art solution. Since ***J*** depends exponentially on ***N_D***, we propose to use ***J*** versus ***N_D*** as a way to benchmark different **MIS** contact architectures. The reference NiSi/***n*-Si** and PtSi/***n*-Si** current density data was obtained from [3], and ***J*** vs. ***N_D*** data was fitted to an analytical model [4]. A **SBH** of 0.55eV provided best fit (Fig. 4), consistent with numerical **QM** analysis done on the same data set [5]. It is also consistent with values extracted on nanoscale contacts for NiPtSi/***n*-Si** contact architecture with heavily doped *S/D* semiconductor ($\approx 3 \times 10^{20} \text{ cm}^{-3}$) [6].

In one study, a TaN/LaO_x/***n*-Si** (**MIS**) contact stack [2] is benchmarked against the NiSi/***n*-Si** reference system in Fig. 5. The TaN/LaO_x/***n*-Si** contact stack provides a very promising result. The benefit demonstrated at low ***N_D***, however, needs to be demonstrated at ***N_D*** $\approx 3 \times 10^{20} \text{ cm}^{-3}$. Various contact architectures to ***n*-Ge** are also benchmarked using ***J*** vs. ***N_D*** plot in Fig. 6. Data was taken from [1, 7-10]. When an insulator is inserted between the metal and ***n*-Ge**, ***J*** is attenuated due to the insulator energy barrier. For example see TiO₂/***n*-Ge**, AlO_x/***n*-Ge**, MgO/***n*-Ge** data points which are lower than the reference line. This leads us to conclude that the **MIS** contact architecture on ***n*-Ge** currently underperforms state-of-the-art NiSi/***n*-Si** system.

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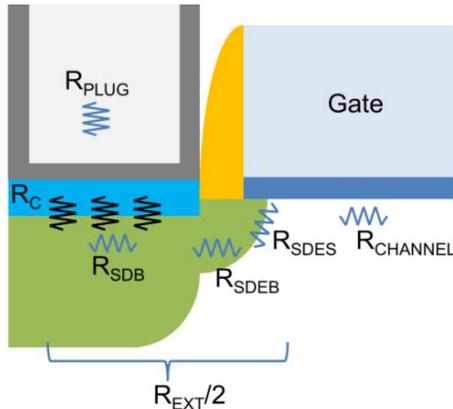


Fig. 1 Schematic showing different resistance components in a MOSFET. Interface contact resistance (R_C) is one of the biggest challenges facing CMOS performance and power scaling due to contact length scaling in accordance with Moore's law (See Fig. 2).

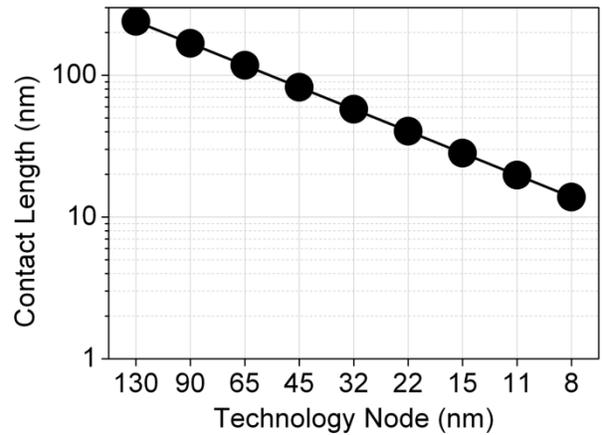


Fig. 2 Trend of contact length as function of CMOS technology node. The contact length shrinks from node-to-node following the scaling of contacted gate pitch in accordance with Moore's law.

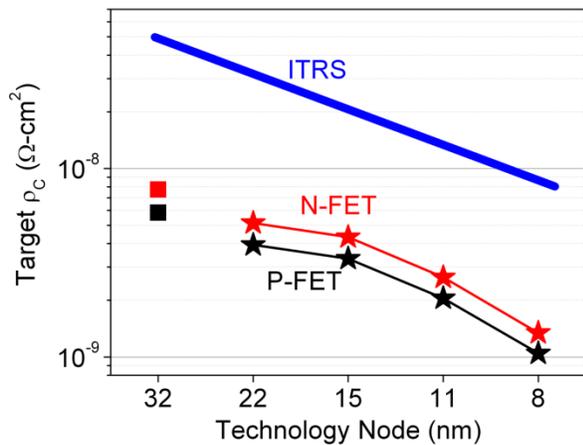


Fig. 3 Specific contact resistivity requirements for different CMOS nodes. Symbols are estimated values in this work.

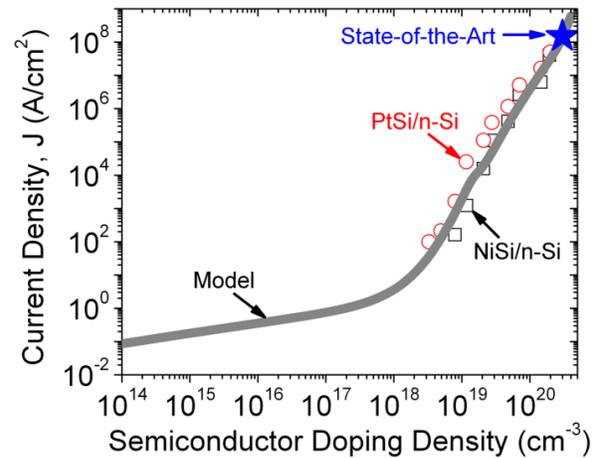


Fig. 4 Current density at 100mV forward bias through NiSi/*n*-Si and PtSi/*n*-Si contact architectures. Analytical model [4] fits the data [3] very well.

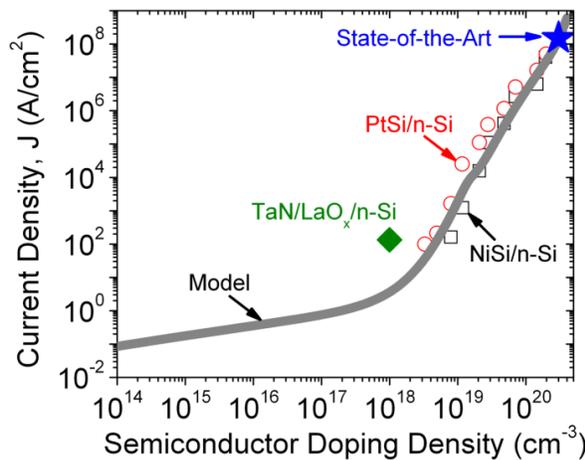


Fig. 5 Benchmarking of TaN/LaO_x/*n*-Si contact architecture [2] versus NiSi/*n*-Si reference.

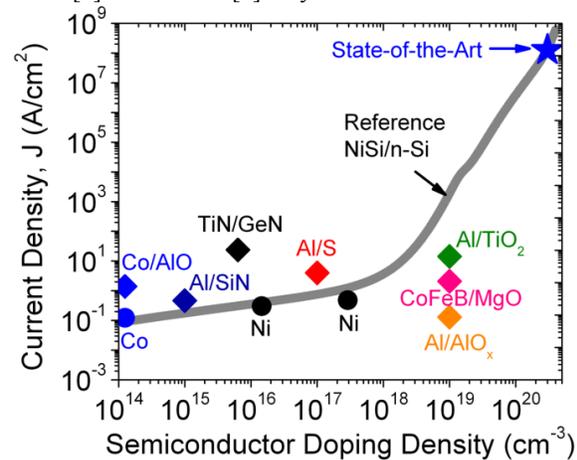


Fig. 6 Benchmarking of various contact architectures on *n*-Germanium [1, 7-10] versus NiSi/*n*-Si reference.

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