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Electron Transport in Multigate In_xGa_{1-x} As Nanowire FETs: From Diffusive to Ballistic Regimes at Room Temperature

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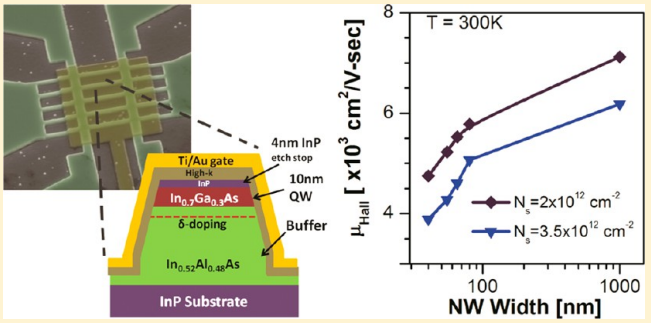
Supporting Information

ABSTRACT: The III−V semiconductors such as $In_xGa_{1-x}As$ (x = 0.53−0.70) have attracted significant interest in the context of low power digital complementary metal-oxide-semiconductor (CMOS) technology due to their superior transport properties. However, top-down patterning of III−V semiconductor thin films into strongly confined quasi-one-dimensional (1D) nanowire geometries can potentially degrade the transport properties. To date, few reports exist regarding transport measurement in multigate nanowire structures. In this work, we report a novel methodology for characterizing electron transport in III−V multigate nanowire field effect transistors (NWFETs). We demonstrate multigate NWFETs integrated with probe electrodes in Hall Bridge geometry to enable four-point measurements of both longitudinal and transverse resistance. This allows for the first time accurate extraction of Hall mobility and its dependence on carrier concentration in III−V NWFETs. Furthermore, it is shown that by implementing parallel arrays of nanowires, it is possible to enhance the signal-to-noise ratio of the measurement, enabling more reliable measurement of Hall voltage (carrier concentration) and, hence, mobility. We characterize the mobility for various nanowire widths down to 40 nm and observe a monotonic reduction in mobility compared to planar devices. Despite this reduction, III−V NWFET mobility is shown to outperform state-of-the-art strained silicon NWFETs. Finally, we demonstrate evidence of room -temperature ballistic transport, a desirable property in the context of short channel transistors, in strongly confined III−V nanowire junctions using magneto-transport measurements in a nanoscale Hall-cross structure.



KEYWORDS: *Field effect transistor, Hall effect, Hall cross, multigate FET, III−V, nanowire FET CMOS, scattering, electrical transport, diffusive transport, ballistic transport*

Power constrained scaling of complementary metal oxide semiconductor (CMOS) technology places several stringent requirements on the performance metrics of the underlying device, such as drive-current, leakage current, on-to-off state current ratio, subthreshold slope, drain-induced barrier lowering, which have to be satisfied simultaneously.[1,2] A key requirement however, is to reduce dynamic power dissipation. This can be achieved by scaling down the supply voltage (V_{dd}) because that power dissipation is proportional to the square of V_{dd}. At reduced supply voltages, however, traditional silicon CMOS is limited by reduced drive currents. In this context, III−V material systems are being actively researched because they afford competitive drive currents at lower supply voltages.[3−5] This advantage stems primarily from the reduced effective mass in low band gap III−V materials, which results in higher mobility.

In order to take advantage of this high mobility while maintaining a high I_{ON}/I_{OFF} ratio, multigate architectures have been introduced to achieve better electrostatic integrity in highly scaled transistors.[6,7] However, confining III−V materials to nanowire (NW) like structures, either by top-down patterning or bottom-up growth, can result in additional scattering mechanisms that are detrimental to electron transport. Figure 1 shows a schematic illustration of the different extrinsic scattering mechanisms that can arise in such structures. Among the various factors that influence the mobility, the dominant mechanism in such structures is likely the scattering from the side walls, and in recent years, there has been significant interest in measuring and modeling these various scattering mechanisms.[8,9] It is therefore crucial to understand whether the advantage of good electrostatic control in nanowire structures will come at the expense of reduced mobility, negating the benefits of using high mobility channel materials.

Despite recent demonstrations of high-performance NW based multigate devices including FETs and inverters,[10,11] there is a lack of quantitative understanding of the true carrier concentration and mobility in such confined structures. Field effect based mobility estimates have been reported for III−V NW and planar devices;[9,12] however, this technique does not

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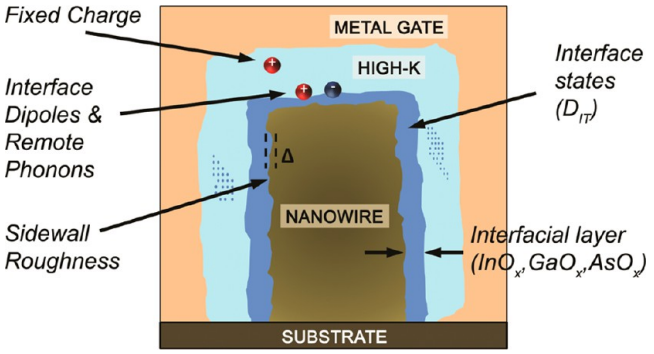

Figure 1. Schematic representation of various extrinsic scattering mechanisms that affect transport in multigate NWFET structures on III–V substrates.

discriminate between the true mobile charge and contributions from charge occupying and emptying the interface trap states (D_{IT}). This inability to distinguish between the two types of charge typically results in an overestimation of channel charge leading to significant error in the estimated mobility. These shortcomings may be partially addressed by using the two FET method, as employed by Gunawan et al. in ref 13. Quantitatively accurate measurements of the true mobile charge concentration, however, may only be obtained through the use of Hall effect measurements as a result of the fact that charge residing in interface traps does not respond to the applied transverse magnetic field.[14,15] Although this technique allows for accurate estimation of the true mobile charge concentration, reliable measurement of the Hall voltage remains challenging in the case of NWs due to their prohibitive geometry. These challenges have become apparent in several recent studies on Hall mobility in NW geometries for various semiconductors.[16−18] Storm et al.[16] measure the Hall mobility in a single InP core−shell NW while simultaneously mapping the spatial distribution of carriers along the NW using cathodoluminescence. The dependence on the gate field (carrier concentration), however, was not studied in this case. Bloomers et al.[17] measure the Hall effect mobility for a surface inversion layer in InAs NWs and were able to vary the carrier concentration by applying a gate voltage through a SiO_2 back gate. In both these studies, however, accurate measurement depends critically on the highly accurate lithographic placement of directly opposing Hall probe electrodes, which makes it prohibitive to study very small NWs with sub-100 nm diameter. By realizing offset probes fabricated using angled contact deposition scheme DeGrave et al.[18] were able to address this shortcoming. Although this technique can be extended to ultrathin NW like geometries, the need to contact the side walls with metal electrodes as well as the requirement for a thick insulator layer on top of the NW prohibits the integration of scaled dielectric layers that is required to study technologically relevant semiconductor multigate NWFET architectures.

In this work, we present a methodology that overcomes the above-mentioned difficulties using a novel test structure design. In this test structure, long channel multigate NWFETs are fabricated using NW arrays while simultaneously integrating Hall probe electrodes that extend between the individual NWs. The final structure forms a Hall bridge with two pairs of opposing Hall probes contacting each NW. Figure 2a shows a false color scanning electron micrograph of the completed device for a NW width of 40 nm. We start with a 10 nm thick

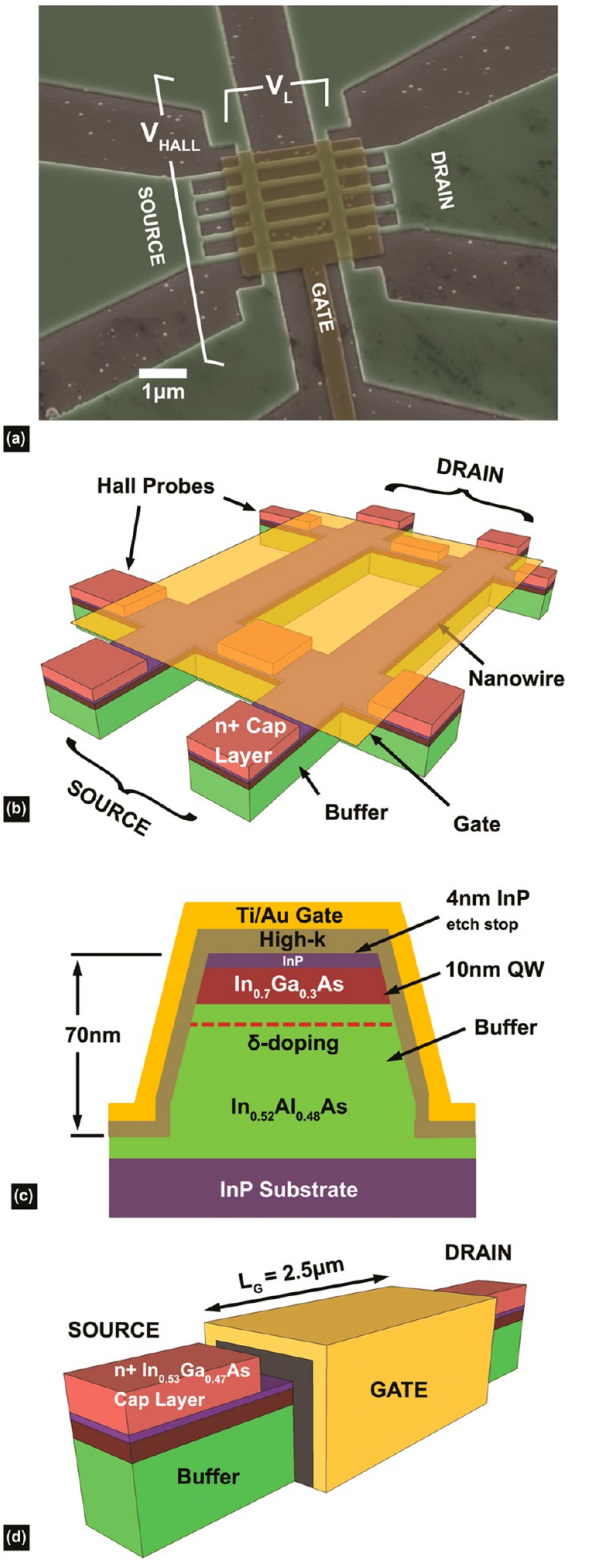

Figure 2. (a) SEM micrograph of multigate, $In_{0.7}Ga_{0.3}As$ NWFET with an array of five NWs of width 40 nm. Also seen are the additional probe electrodes integrated to form a Hall bridge structure. Hall voltage (V_{HALL}, also referred to as V_H) and longitudinal (V_L) voltage are measured as shown. (b) Schematic of the device showing two representative NWs and the structure of the probe underneath the gate. The heavily doped n+ cap layer is also retained on the probe electrode in the regions between the NWs. (c) Schematic cross-section of the NW showing the layer structure of the substrate and (d) perspective view along a NW in the array.

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$In_{0.7}Ga_{0.3}As$ quantum well (QW) channel grown by molecular beam epitaxy (MBE) on semi-insulating InP substrate. A 4 nm thick InP etch stop layer and 20 nm thick heavily doped n-type $In_{0.53}Ga_{0.47}As$ layer are grown on top of the quantum well to facilitate ohmic contacts to the metal electrodes. The n+ cap layer is first recessed, using a wet etch comprising citric acid and H_2O_2, in order to define the channel region. The etch mask is created by opening windows, using e-beam lithography, in diluted ZEP 520A resist to define the recess etch openings over the regions where nanowires will subsequently be patterned. The spacing between consecutive NWs in the array is kept at 500 nm. Accounting for the 50 nm undercut from each side resulting from the wet etch, we leave behind 400 nm of heavily doped cap layer on the Hall probes in the regions between the NWs as seen in Figure 2b.We retain the cap layer in these regions in order to maintain low resistance on the probes. Subsequently the entire structure comprising of the source/drain electrodes, NW array, and Hall probe electrodes is patterned using e-beam lithography followed by dry etching in a chlorine (Cl) based plasma. This is followed by atomic layer deposition (ALD) of 1 nm Al_2O_3 and 3 nm HfO_2 high-k dielectric stack followed by Ti/Au gate metal electrodes, patterned using evaporation and lift-off process. The cross section of the NW is shown schematically in Figure 2c. Finally, a second metal stack comprising of Ti/Au is deposited on the n + cap using lift-off to form the source/drain pads. Figure 2d provides a three-dimensional perspective view of the gated nanowire region.

We fabricate devices with various NW widths starting from 1 μm (plate type geometry) down to 40 nm in order to create to a 1D confined geometry. The gate lengths for all the test structures are kept constant at 2.5 μm while maintaining a source to drain separation of 4 μm and Hall probe separation of 1.5 μm. The quality and morphology of the side walls of the top-down etched structures is of utmost importance as this directly impacts the transport properties through the scattering mechanisms delineated earlier in Figure 1. We analyze the cross−section of the etched NWs through transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) as shown in Figure 3. The side wall shows a smooth etch profile without any visible damage to the NW. However, we see that a thin (∼1 nm) indium rich native oxide layer is left behind after etching. This layer is etched subsequently using a dilute sulfuric acid treatment prior to deposition of high-k dielectric. The resulting interface has good electrical properties as evidenced by NWFET characteristics shown in Figure 4. The measured transfer characteristics for the long channel array device with 40 nm NW width shows a subthreshold slope of 85 mV/dec. Close to zero drain-induced barrier lowering (DIBL) indicates good electrical isolation between source and drain pads for the $In_{0.7}Ga_{0.3}As$ quantum well structure, aided by the presence of InAlAs barrier layer. Further, the output characteristics show good saturation with a peak drive current of around 250 μA/μm.

After ensuring good FET transfer characteristics for the test structure, we perform gated Hall measurements. The Hall measurements are performed in a Lakeshore TTP6 cryogenic probe station equipped with a superconducting magnet that can generate magnetic fields up to 2.5T. The magnetic field is oriented perpendicular to the substrate for all the measurements carried out in this study. We point out here that since the test structures are FETs constructed in a Hall bridge geometry, it is possible to change carrier concentration in a well-

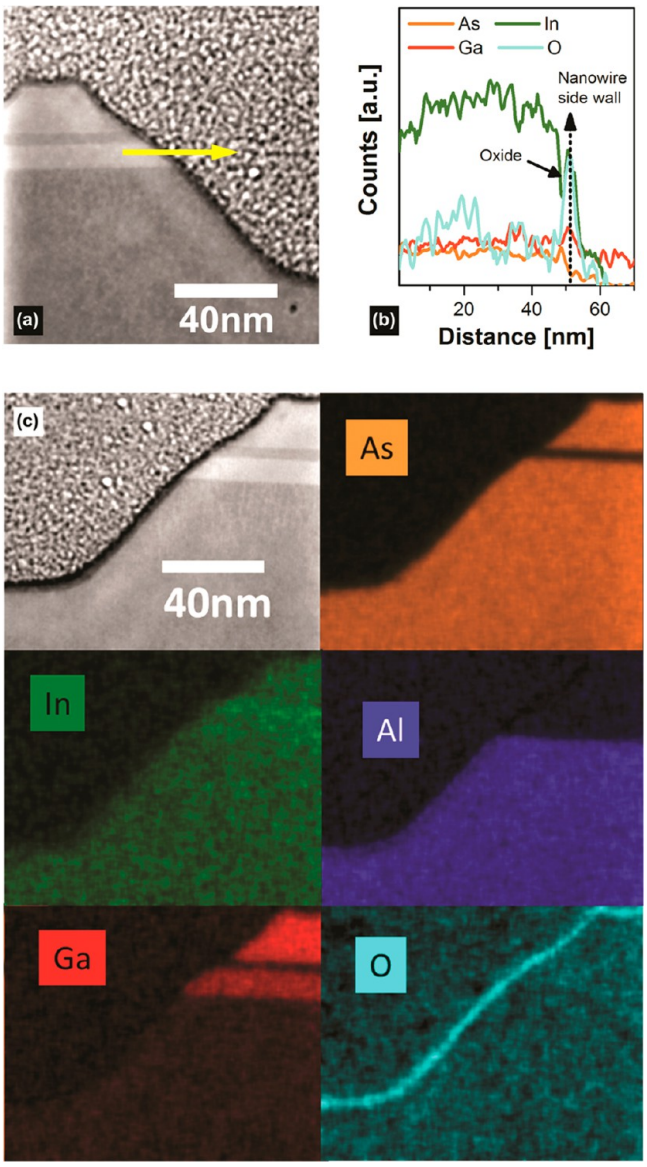

Figure 3. Characterization of the top down patterned nanowire subsequent to plasma etching: (a) STEM image indicating location of EELS line scan and (b) results of EELS line scan showing possible formation of indium oxide interfacial layer. (c) EELS elemental map of NW cross-section confirming that top-down etch yields high quality, defect-free NW structure, while also highlighting the formation of native oxide layer on side walls.

controlled fashion using gate modulation. The gate voltage (V_{gs}) is varied from −0.5 to 1 V in steps of 50 mV, while applying a fixed source to drain bias (V_{ds}) of 50 mV. The Hall voltage (V_H) is then recorded at magnetic field values of ±0.5 and ±0.8T for each gate bias, and the measurements are then repeated after reversing the polarity of V_{ds}. Thus the Hall voltage from each pair of probes is written as

$$V_H = \frac{(V_{H1} + V_{H2})}{2}$$

where

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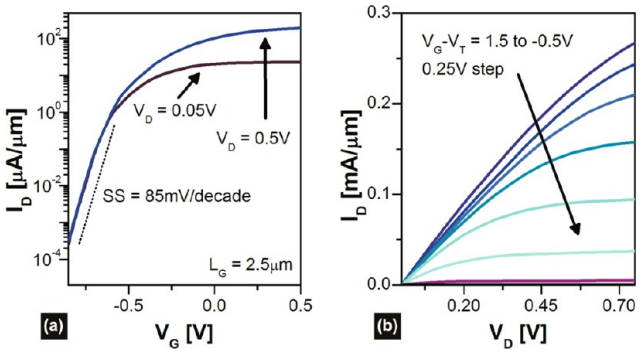

Figure 4. (a) Transfer characteristics (I_D–V_G) of the multigate NWFET based Hall structure with NW width of 40 nm showing good subthreshold behavior. (b) Output characteristics (I_D–V_D) of the same device.

$$V_{H1} = \frac{1}{2}\left[\frac{V_T(+B_1) - V_T(-B_1)}{2} + \frac{V_T(+B_2) - V_T(-B_2)}{2}\right] \quad \text{at} \quad V_{ds} > 0$$

$$V_{H2} = \frac{1}{2}\left[\frac{V_T(+B_1) - V_T(-B_1)}{2} + \frac{V_T(+B_2) - V_T(-B_2)}{2}\right] \quad \text{at} \quad V_{ds} < 0$$

This entire set of measurements is then repeated using the second pair of Hall probes. The results are thus averaged over the set of 16 measurements to yield each data point in order to ensure reliable estimates as well as rule out measurement artifacts arising from geometrical asymmetries such as unintentional offsets between Hall probes.

The measurements are performed using a Keithley 4200 semiconductor characterization system with five source measure units (SMU). Two SMUs are configured as voltage sources, connected to the gate and the drain, respectively, while the source terminal is grounded. These SMUs determine the bias conditions for the FET while the three remaining SMUs are configured as nanovoltmeters to measure the Hall and longitudinal voltages, respectively. The gate voltage dependence, as shown in Figure 5a, shows a roll off with increasing carrier density (gate electric field) in the channel. More importantly, as summarized in Figure 5b, our results show that the mobility reduces monotonically as the NW dimensions are scaled down, indicating that scattering increases as a result of confinement.

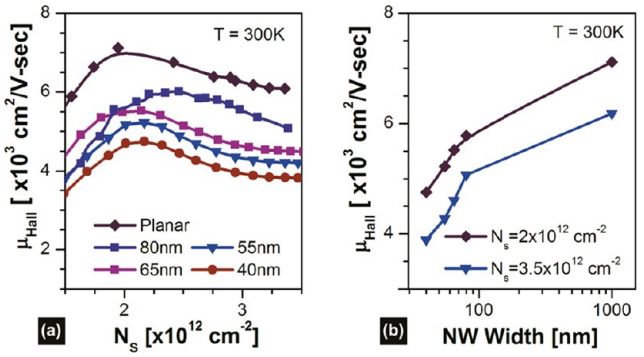

Figure 5. Experimentally measured Hall electron mobility for multigate NWFET of Figure 2 as a function of carrier concentration for different NW widths. (b) Mobility shows a monotonic roll-off with reducing NW dimensions. Peak mobility is observed at a carrier concentration of 2 × 10^{12} cm^{-2} for all NW widths.

Devices with nanoscale channels are particularly challenging in the context of Hall measurements due to the small currents involved, which results in low values of Hall voltage for practically accessible magnetic field strengths. We show here that by increasing the number of NWs in parallel, it is possible to generate larger Hall voltages as the contribution from each NW will add in series. Because the Hall voltage is measured using a high impedance voltmeter, current does not flow perpendicular to the NWs. Thus, resistive voltage drops along the Hall probe are ruled out. The total Hall voltage may then be written as the addition of individual Hall voltages produced from each NW. This is in turn a function of the current (which in turn depends on gate bias) and the magnetic field. For a uniform array of NWs, assuming that the dimensions for each NW are the same, the average Hall voltage per NW maybe expressed as

$$V_H = \frac{1}{N}\sum_{i=\langle N\rangle} V_{Hi}$$

where N is the number of NWs in parallel. Next, in order to measure longitudinal resistance the magnetic field is turned off. The SMUs configured as high impedance voltmeters are now connected to a pair of probes spaced along the NW. The resulting structure then forms a parallel resistor network so that the total longitudinal resistance for each NW may be expressed, in units of ohm/square, as

$$\frac{1}{R_{SH}} = \frac{1}{N}\frac{L}{W_{NW}}\sum_{i=\langle N\rangle}\frac{1}{R_i}$$

where the effective width is taken to be the active perimeter of the NW which includes the top width and side walls, that is, $W_{NW} = W_{Top} + 2H_{SW}$. It should be noted that here L refers to the distance between the hall probes. For a given Hall voltage, the sheet carrier density may then be evaluated in units of cm^{-2} as

$$n_S = \frac{IB}{qV_H}$$

ultimately yielding the average mobility for an individual NW in units of $cm^2/V{\cdot}sec$ as

$$\mu = \frac{1}{qR_{SH}n_S}$$

The mobility trends observed in Figure 5a,b for the NW geometries are estimated using the above procedure and clearly depict a mobility roll-off with reducing NW width.

In order to understand the validity of the above method, we simulate the entire structure using a finite element three-dimensional (3D) numerical device simulator, Sentaurus TCAD.[19] Three-dimensional drift diffusion simulations are performed while incorporating a density gradient approximation model to capture the quantization effects. The simulations are first calibrated to the measured I_D–V_G characteristics of Figure 4. We subsequently add the magnetic field dependence in the simulation using the built-in drift-diffusion-based model for current densities that is augmented by magnetic-field-dependent terms corresponding to the Lorentz force on the motion of the carriers.[19] Figure 6a shows the potential profile in the structure with an applied magnetic field of 0.4T. In order to

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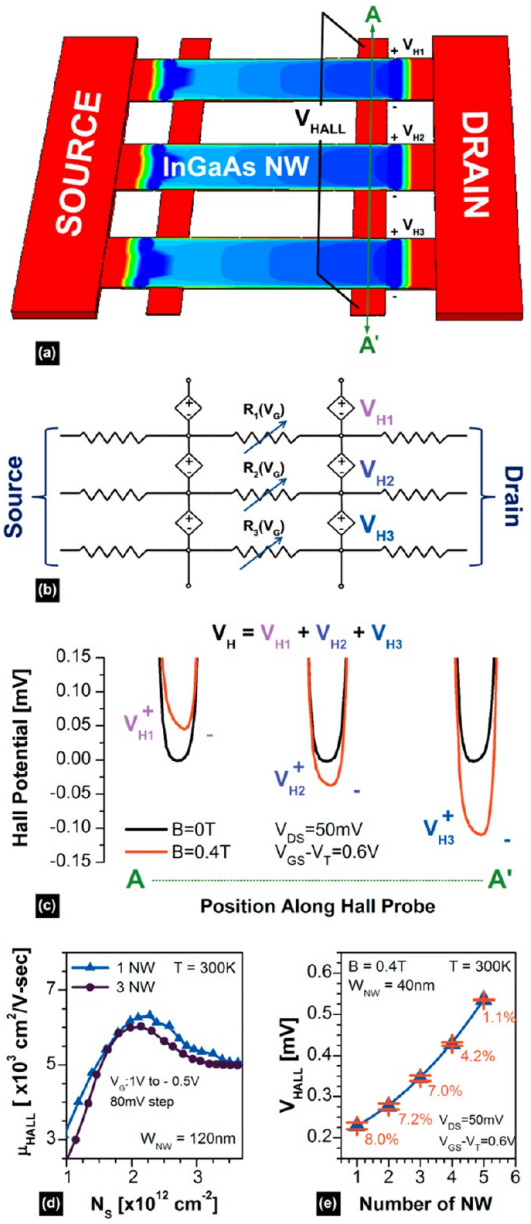

Figure 6. Improving measurement accuracy: (a) simulated electrostatic potential through the NW array. (b) Equivalent circuit model based interpretation for the array and (c) simulated Hall potential profile plotted as a function of position along the Hall probe. The results show that each NW contributes a small Hall potential to the total V_H, which is measured across the device. (d) Plot of measured results for Hall mobility as a function of carrier concentration showing excellent agreement between single NW and NW array device. These results confirm the equivalent circuit based interpretation of panel b. (e) Simulated Hall voltage as a function of NW number showing an increase in measured Hall voltage as number of NWs increases. Because of the averaging effect of the array, the error of the measured Hall voltage reduces as number of NWs increases. This error is less than 1% when the number of NWs is increased beyond 5.

allow a convenient interpretation of the observed potential and charge distribution, we construct an equivalent circuit model as shown in Figure 6b. The Hall voltage produced by each NW is represented as a gate voltage dependent voltage source since the carrier concentration (Hall voltage) is controlled by the gate voltage, and the longitudinal resistance of each NW is represented by a corresponding voltage dependent resistor. Figure 6c shows that the Hall potentials generated from each NW add in series, resulting in a larger V_H across the entire structure.

In addition to the numerical validation of our technique, we test the accuracy experimentally by comparing the mobility between single NW and multi-NW devices as shown in Figure 6d. We compare the results for a single NW and array device at a NW width of 120 nm so that reliable measurements of Hall voltage may be obtained even for a single NW device. The results agree closely thus validating the equivalent circuit model based interpretation. Finally, as shown in Figure 6e, we compare the error between the expected total Hall voltage and that calculated by summing the values from individual NWs. We note that, as the number of NWs is increased, the percentage error in the estimated Hall voltage reduces and the accuracy of mobility extraction increases. The experimental structures presented in this study implement NW arrays with five NWs in parallel for which the estimated error is of the order of 1%. Further, we compare the results of our mobility extraction with published results on similar structures measured using the field effect technique (split CV measurements), shown in Figure 2 of the Supporting Information. Additionally, Figure 3 of the Supporting Information shows close agreement between the field-effect mobility extracted independently from Sentaurus TCAD device simulations calibrated to the measured FET transfer characteristics of Figure 4. The excellent agreement between the results from different methods, extracted independently of each other, further validates the technique presented in this work for gated Hall measurement in NWs.

An important question however, is the value of mobility that can be expected at smaller NW widths close to or below 10 nm that is of significant technological interest. Simulation studies for silicon NWs[20,21] show that the additional scattering present in thin NWs can be effectively modeled by potential fluctuations resulting from surface roughness. This type of scattering is a temperature-independent phenomenon. Experimental evidence for such surface roughness based scattering has also been observed in ballistic InAs NWFETs.[22] Figure 7a shows the results of ungated ($V_G = 0$) Hall measurements for our top-down patterned NW devices. We are able to perform such measurements as the devices used in this study operate in the depletion mode with the channel normally on without applying a gate bias. The reduction in mobility resulting from reducing the NW width is extracted by Mathiessen's rule using the mobility of the planar structure as the reference. Thus, we write $1/\mu_{SW} = 1/\mu_{Planar} - 1/\mu_{NW}$ where, μ_{SW} refers to the side wall roughness limited mobility. Figure 7b shows clearly that the scattering limited mobility in our case also exhibits temperature independence. We note that similar mobility trends have also been observed for vapor-transport grown InGaAs NWs[23] measured using the field effect technique, which however suffers from drawbacks highlighted before.

In light of these observations, it is clear that the mobility degradation trends observed in this work can be attributed to surface roughness-induced scattering resulting from the side walls. In order to quantify the impact of this scattering, we assume an exponentially correlated roughness and calculate the associated scattering rate using the approach in ref 22. The matrix element (overlap integral) however is estimated using the model in ref 20 which accounts for the dependence of wave function spread and effective electric field on the NW size. Further details may be found in the Supporting Information of

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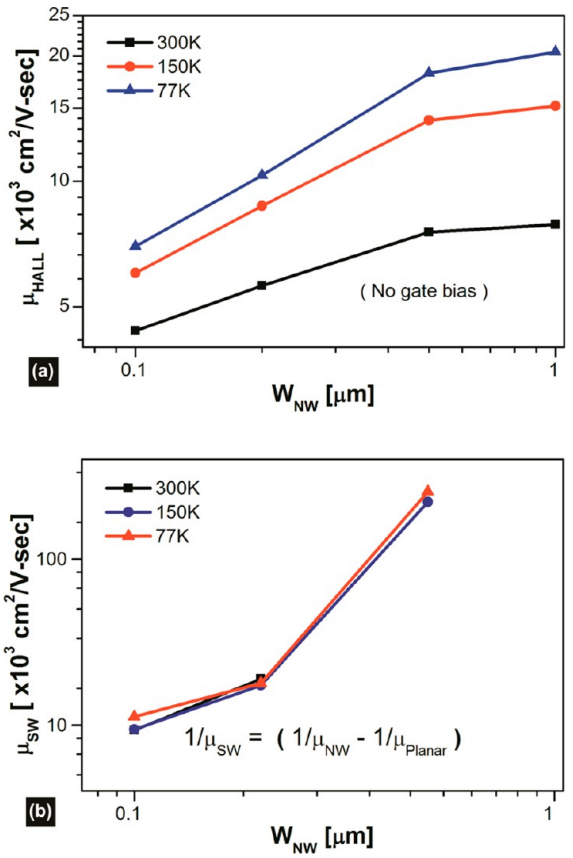

Figure 7. (a) Temperature-dependent, ungated Hall measurements showing mobility degradation as the InGaAs quantum well is patterned into NWs with width reducing from 1 μm (planar) down to 100 nm. (b) The additional scattering extracted using Mathiessen's rule. This component is found to be independent of temperature clearly indicating that the scattering arises from roughness due to the side walls.

this paper. Because the top surface is capped with the InP layer, it is reasonable to assume that the scattering contribution from this MBE grown interface remains constant with NW width while that from the side walls scales commensurately. Figure 8

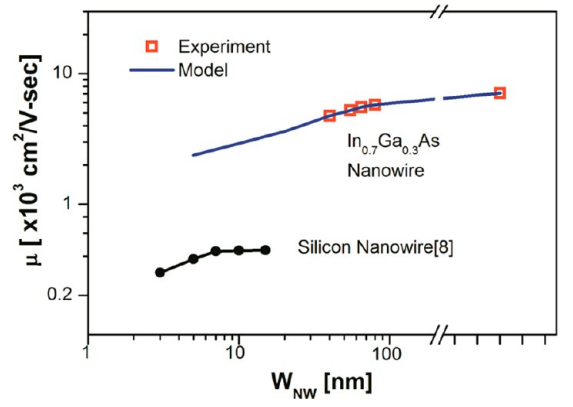

Figure 8. Projection of mobility for 10 nm NW width. The side-wall roughness scattering model is calibrated to the measured data. The gated Hall measurement results clearly indicate a mobility roll-off with decreasing nanowire width. Comparison of mobility between InGaAs and silicon NWs indicates over 10× higher mobility for InGaAs at a NW width of 10 nm.

projects the mobility values for NWs at 10 nm width after calibrating the model to the measured results. We note that these values are significantly higher compared to what is projected for silicon NW transistors with similar dimensions.[8]

In the context of low power digital CMOS technology at scaled gate lengths however, it is important to investigate if ballistic transport is achievable at room temperature in such top down patterned III−V NWs. For very short channel lengths, it is expected that the carriers will travel across the transistor channel with little or no scattering, which is conducive to higher drive currents at low supply voltages.[24] Ideally in a fully ballistic channel, the longitudinal resistance would vanish to zero. Such effects have been observed in two-dimensional electron gases in the seminal works published on the quantum and fractional quantum Hall effects.[25,26] These effects however, are observed only in the presence of strong magnetic fields. Zero longitudinal resistance has been demonstrated, however, in a NW type of structure by Picciotto et al.[27] The authors create confined nanowire type geometry through a cleaved edge overgrowth technique, while simultaneously connecting to the planar two-dimensional electron gas (2-DEG). In order to realize contacts, probes are defined by depleting the planar 2-DEG in selected regions using gate electrodes, enabling the demonstration of zero longitudinal resistance through a four-point measurement. However it should be noted that all the above measurements are performed at very low (typically mK) temperatures. Despite these experimental demonstrations of ballistic transport, little direct evidence exists for observing such phenomena at room temperature. At room-temperature, phonon scattering dominates transport, significantly reducing the mobility, and tends to quench any observable effects. Scattering free transport at room temperature may perhaps be accessible with more exotic materials such as topological insulators,[28] which are actively under investigation.

In the context of semiconductor NWFET structures, ballistic transport has been demonstrated through quantized conductance measurements[22,29] where conductance plateaus are observed using a traditional two probe configuration. These results have been observed at significantly higher temperatures of up to 190 K for NWs with diameters smaller than 25 nm.[22] Here, the authors show that at 120 K, as expected for short channel lengths of 60 nm, significant fraction of carriers participating in the transport are ballistic with the corresponding carrier mean free path (λ) of 170 nm. For NWs demonstrated in this work, after accounting for the reduction in mobility with NW width, we project that for a width of 10 nm the mobility is close to 3000 cm^2/V·sec at room temperature. This corresponds to a mean free path of λ = 60 nm, calculated as $\lambda = \upsilon_F\tau$, where we assume υ_F to be the Fermi velocity and τ is the lifetime estimated from the mobility. Thus at room temperature, it may be possible to observe ballistic transport only over very short length scales.

In order to investigate ballistic transport in our top-down patterned NWs, we construct a nanoscale Hall cross structure as shown schematically in Figure 9a. This structure allows a four point resistance measurement. However, instead of measuring traditional longitudinal four point resistance we measure the so-called bend resistance[30,31] in these structures as a function of both magnetic field and temperature. The bend resistance is defined as $R_B = V_{21}/I_{34}$ as shown in Figure 9a. If the transport in the junction is predominantly diffusive, the electrons undergo scattering within the junction and the voltages measured between probe 1 and 2 simply correspond to

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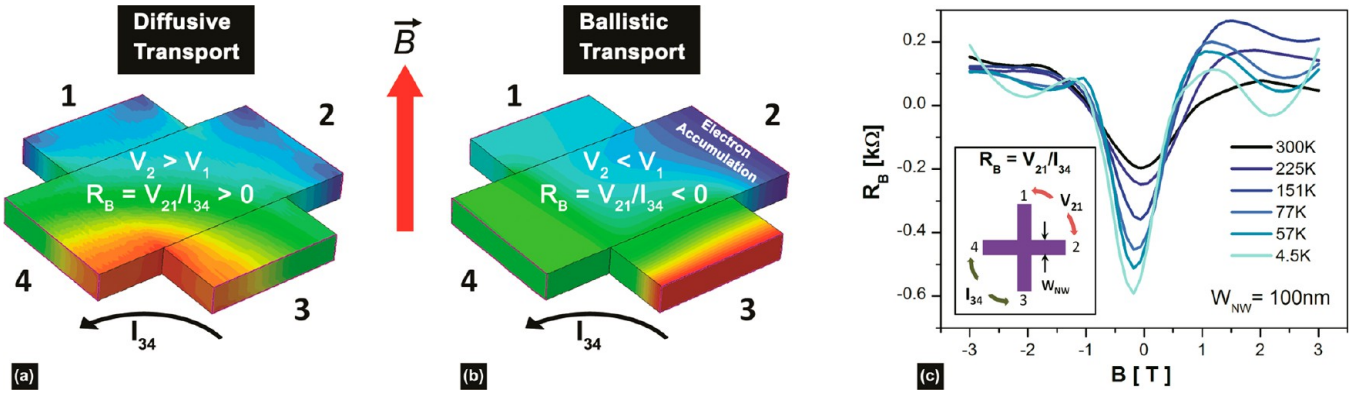

Figure 9. (a) Simulated potential distribution profile for a Hall cross structure in the diffusive regime. As current flows from contact 3 to 4, a positive bend resistance is measured. (b) Potential distribution in the ballistic regime. Electrons from contact 4 travel past the junction without scattering and start accumulating in contact 2 reversing the polarity of V_{21}, thus giving rise to negative bend resistance. (c) Measured bend resistance as a function of magnetic field and temperature for $In_{0.7}Ga_{0.3}As$ NW-based Hall cross structure. Negative bend resistance is observed even at room temperature confirming ballistic transport at room temperature in this structure.

the resistive drop as current flows diffusively from probe 3 to 4, implying that $V_{21} > 0$. In the case of ballistic transport, as seen in Figure 9b, electrons leaving terminal 4 do not scatter within the junction. This allows them to conserve momentum, travel past probe 3, and accumulate in probe 2. A negative potential then builds up in probe 2 relative to probe 1 thus reversing the polarity of V_{21}. By definition, R_B is negative thus giving rise to negative bend resistance. In the presence of a magnetic field, the electrons are forced to curl back into contacts 3 or 1, thus restoring a positive value for V_{21}. In such a configuration, ballistic transport may be observed more easily than in a longitudinal resistance measurement as the behavior of the carriers is probed over a very small length scale. Ultimately, it should be noted that negative bend resistance provides a clear signature for ballistic transport through the nanowire junction.

Figure 9c shows the experimental results for our NW-based Hall cross structure. The device consists of a junction of two perpendicularly oriented NWs each of width of 100 nm which is comparable to the mean free path at the smallest NW width. A current of 100 nA is forced from probe 3 to 4 while measuring the voltage difference between probes 2 and 1. As seen the resistance shows a negative peak at zero magnetic field and diminishes as the magnetic field is ramped in either direction. Further, we note that the magnitude of the peak reduces with increasing temperature due to the onset of phonon scattering which pushes the carriers into the diffusive regime. Most interestingly, we observe that negative bend resistance is present up to room temperature clearly indicating that a significant fraction of the carriers still exhibit ballistic behavior at room temperature. We conclude that despite the significant deterioration resulting from side-wall roughness scattering in these NWs, the mobility is still significantly high so that a large fraction of electrons participating in transport are predominantly ballistic over short lengths at room temperature. These results indicate that III−V NWs are likely to behave as ballistic channels over short lengths that will allow high drive currents in short channel NWFETs even at reduced supply voltages.

In conclusion, we demonstrate a novel technique for accurate quantitative estimation of charge and mobility in III−V semiconductor nanowire based multigate transistor architectures. We utilize gated Hall measurements to accurately measure mobility as a function of gate bias modulated carrier concentration for $In_{0.7}Ga_{0.3}As$ NWFETs with widths as small as 40 nm. Although the method is demonstrated for the specific example of InGaAs Trigate NWFETs, we believe that it can be extended to other NWFET architectures and materials. The present investigation shows that reducing the nanowire width results in mobility degradation due to scattering from the side wall roughness. After careful calibration of scattering models to measured experimental data, we are able to extend the results to smaller nanowire dimensions and show that for ultranarrow NW dimensions close to 10 nm the expected mobility is approximately 3000 $cm^2/V{\cdot}sec$, significantly better than state of the art silicon devices. Finally, we demonstrate direct observation of room-temperature ballistic transport despite the detrimental impact of side wall scattering for the NW structures in this work. These results indicate that III−V semiconductor based ballistic NWFETs may provide a viable path to low power CMOS logic technology at nanoscale channel lengths of 14 nm or smaller.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Additional information and figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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