Impact of fin width scaling on carrier transport in III-V FinFETs

Arun V. Thathachary[1], L. Liu[1] and S.Datta[1]
[1]Pennsylvania State University-PA-16801,U.S.A

Introduction: Power constrained scaling mandates that devices for future nodes beyond 14nm will need to maintain high drive currents at low supply voltages. In this regard, III-V FinFETs have attracted much interest due to their superior transport properties [1-2]. However in order to maintain electrostatic integrity, multi-gate architectures such as the FinFET will be implemented simultaneously. As shown in figure 1, patterning of III-V substrates into narrow Fin structures can have an adverse impact on channel mobility due to additional scattering mechanisms coming from side wall roughness. Further the potentially high interface state density at the III-V sidewall – High –k interface could lead to further degradation in channel mobility. In this work we quantify the mobility degradation through hall measurements on long channel FinFETs realized on $In_{0.7}Ga_{0.3}As$ quantum well substrates. Further, we extract the percentage degradation arising from side wall roughness and project the expected mobility down to 10nm Fin widths.

Device fabrication: Devices are realized on MBE grown substrates from IQE Inc. First 20nmTi/50nmAu is realized for the source/drain and Hall probe pads using lift – off. Then the heavily doped cap layer is recessed in the active region of the device (over the Fin). This is followed by lithography and a BCl_3/Ar dry etch with the resist mask to isolate the individual devices along with the Fin. This is followed by Atomic Layer Deposition of 1nmAl_2O_3 and 3.5nm HfO_2, followed by annealing at 350C in forming gas ambient. Finally the gate electrode is patterned by lift-off of 20nmTi/50nmAu. Figure 2a shows the device cross-section under the gate stack. An Atomic Force Microscope scan of the final device realized is shown in figure 2b. Figure 2c shows the configuration of the device for Hall measurements.

Results: Figure 3 shows the IdVg and output characteristics for the lowest fin width device (W_{fin} = 100nm) measured using a Keithley 4200 SMU. Hall measurements were then performed in a Quantum design Physical Property Measurement System (PPMS) by wire bonding the devices. A magnetic field of $\pm$ 0.5T is used and possible geometrical asymmetry is averaged out by measuring for all configurations of the Hall probes as shown in figure 2c. The measured mobility for V_G = 0V, at different temperatures are shown in figure 4a. It should be noted that the mobility monotonically reduces with the fin width. When the additional scattering is extracted simply using Mathiessen's rule, it is seen to have negligible temperature dependence as shown in figure 4b. Thus it is reasonable to assume that the degradation is caused mainly by the side wall roughness. Similar trends have been reported for InSb electron waveguides [3], at very low temperatures (2K) but only down to waveguide widths of 500nm.

Modeling this added sidewall roughness scattering using a scattering rate dependence $1/\tau \propto |\varepsilon_{avg}|^2$ on the lateral electric field perpendicular to the sidewall (similar to surface roughness scattering model discussed in [4]) we fit the experimental data for different fin widths at 77K, 150K and 300K as shown in figure 5. It is seen that the degradation is exacerbated with reducing fin width as a greater percentage of carriers are susceptible to scattering from the sidewall. Extending the model we see that high mobility (~3000cm^2/V-sec) is retained down to 10nm fin width, significantly higher still compared to bulk silicon CMOS.

Further insight into the mechanism is provided by figure 6a. The sidewall roughness limited mobility is proportional to a carrier density – weighted, average of the lateral electric field coming from the side walls. At a fixed carrier density, reducing fin width results in larger average lateral electric field perpendicular to the sidewalls, resulting in mobility degradation. This is seen more clearly in figure 6(b) (iv-ii), which shows the spatial variation of the lateral electric field and the normalized carrier density along the fin width. However as we continue to scale below 10nm fin width volume inversion (Figure 6b(i)) caused by strong quantization, is eventually expected to provide further enhancement in the mobility.

Conclusions: In conclusion this work highlights the importance of side wall scattering as the primary mechanism resulting in reduced mobility when scaling fin width for III-V FinFETs. By quantitative modeling of un-gated Hall mobility obtained from long channel FinFETs we project that the mobility for fin widths down to 10nm is still appreciably high. Despite significant reduction in mobility, III-V QW channels will show superior transport properties compared to state-of-the-art Silicon devices at highly scaled dimensions.

[1] L. Liu et. al., *Proc. Int. Electron Devices Meeting*, 2011 [2] JJ Gu et. al., *Proc. Int. Electron Devices Meeting* 2012 [3] A.M. Gilbertson et. al., *Phys. Rev. B*, 075304, 2011 [4] D.K. Ferry et. al., Transport in Nanostructures, *Cambridge university Press*.

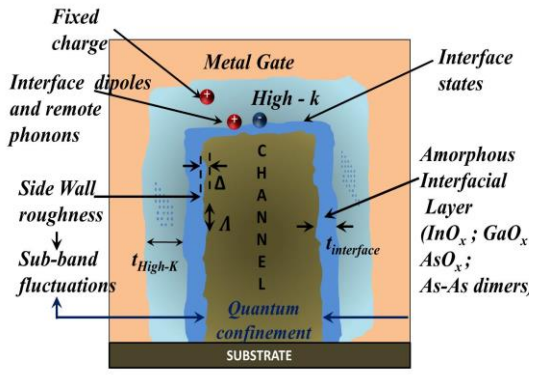
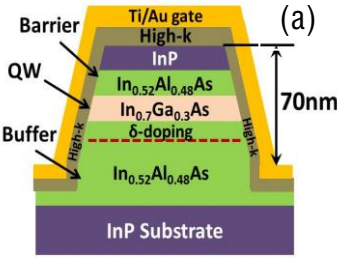
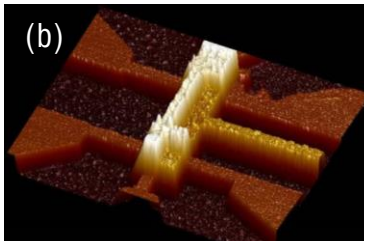


Fig.1 Sources of mobility degradation in III-V FinFETs. Scaling from Planar to Multi-gate architectures introduces additional scattering from side-wall roughness and interface states.





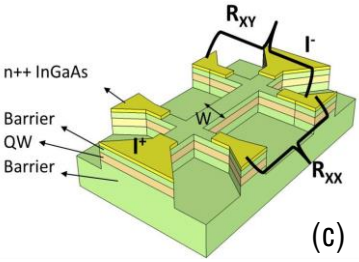


Fig.2 (a) Device cross-section under the gate region showing 10 nm Quantum well $In_{0.7}Ga_{0.3}As$ channel (b) AFM image of fabricated long channel FinFET with integrated Hall voltage probes. (c) Schematic of the configuration for hall measurements.

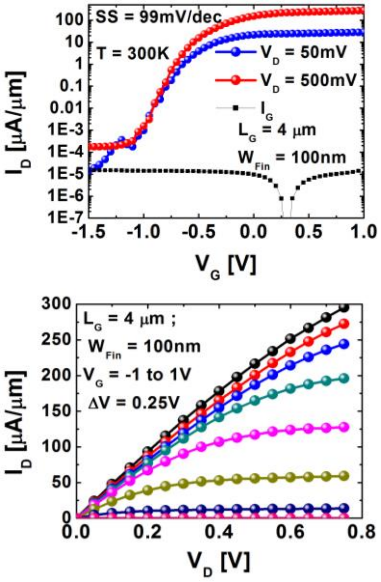


Fig.3 IdVg and output characteristics of physically realized long channel FinFET with 100nm fin width.

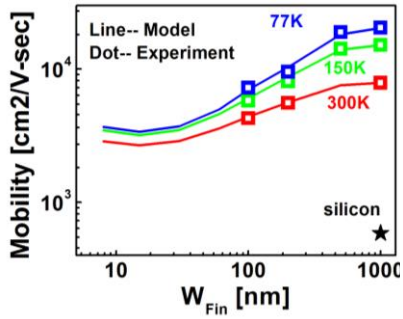
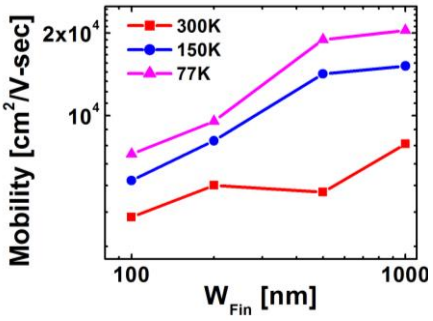


Fig.5 Experimental Hall mobility fitted using a side wall roughness scattering model. Projected mobility for 10nm III-V FinFET is much larger than silicon.



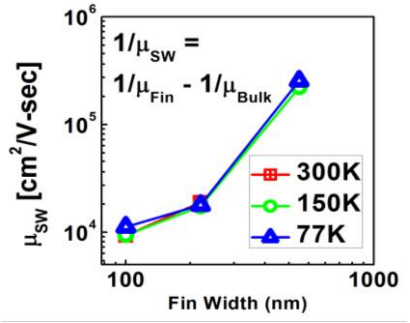
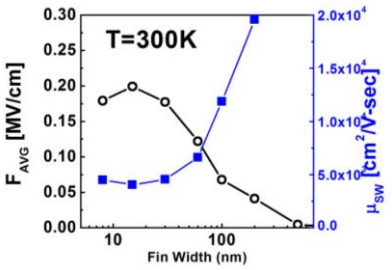


Fig.4 (a) Measured Hall mobility (V_G = 0) for different fin width down to 100nm as a function of temperature (b) Contribution to scattering from side wall extracted using Mathiessen's rule showing that the residual scattering component is temperature independent.



$$\mu_{SW} = e\tau_{sw}/m^* \qquad (a)$$

$$1/\tau_{sr} = \frac{|F_{avg}|^2 e^2 m^*}{2\pi\hbar^3} \times \int_0^{2\pi} d\theta \frac{\pi\Delta^2 L^2}{(1+q^2L^2/2)^{3/2}}(1-\cos\theta)\left|\frac{\Gamma(q)}{\varepsilon(q)}\right|^2$$

$$, where,\ q = 2k\sin(\theta/2)$$

$$F_{avg}(W_{FIN}) = \iint_{W_{FIN},H_{FIN}} dydz\phi^*(y,z)\frac{\partial\varphi(y,z)}{\partial y}\phi(y,z)$$

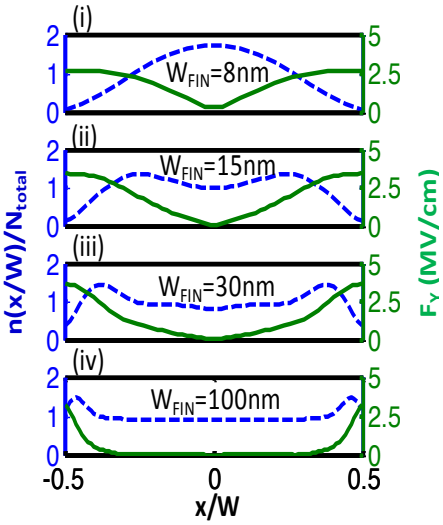


Fig.6 (a) Plot of average lateral electric field and side wall limited mobility for various fin widths. (b) Spatially averaged electric field and normalized carrier density along the fin width showing volume inversion below 10nm.