Enhancement Mode Strained (1.3%) Germanium Quantum Well FinFET (W_{fin}=20nm) with High Mobility (μ_{Hole}=700 cm^2/Vs), Low EOT (~0.7nm) on Bulk Silicon Substrate

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[1]The Pennsylvania State University
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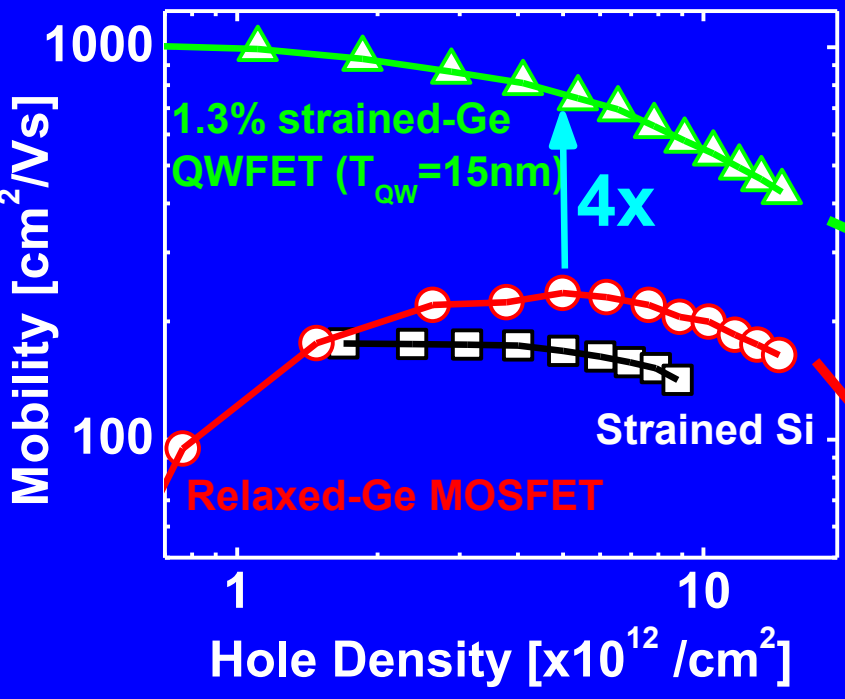
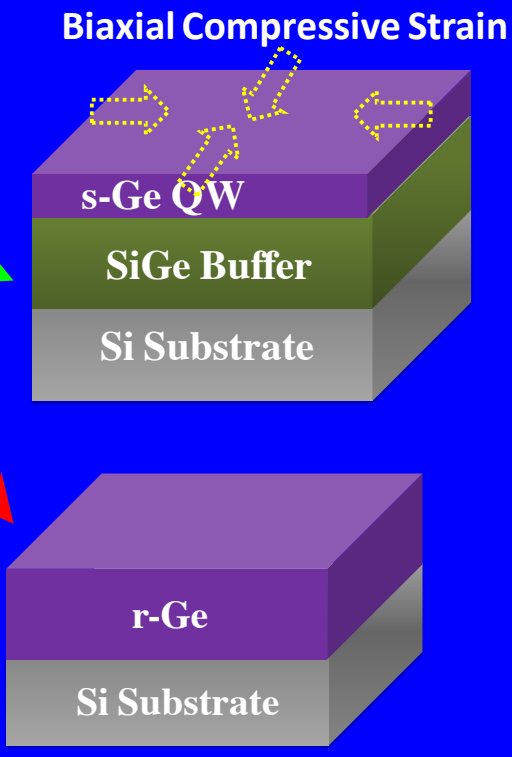
[4]Taiwan Semiconductor Manufacturing Company

Outline

- High Mobility Strained Germanium (s-Ge) QW
- Novel Tri-layer Dielectric Integration on Ge
- s-Ge QW on silicon Buffer Design and Growth
- s-Ge QW FinFET Fabrication and Characterization
- Benchmarking

Strain-Enhanced Mobility





*R. Pillarisetty, Nature 2011

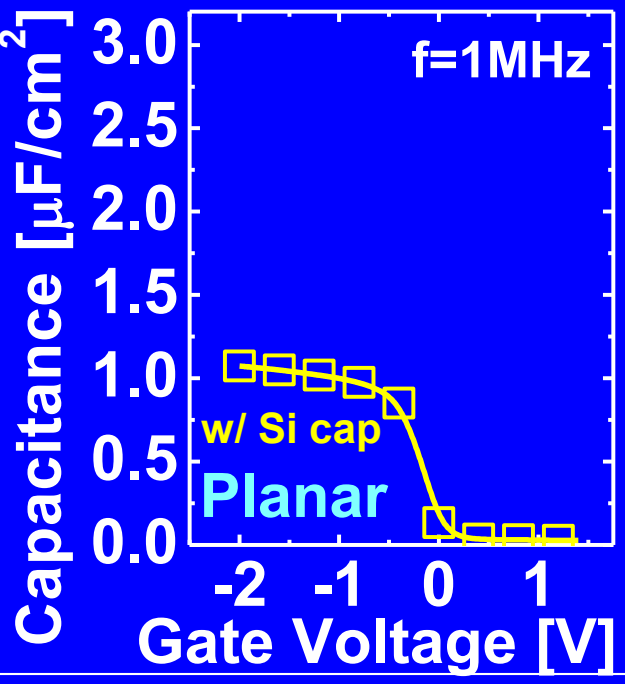
➢ 4x higher hole mobility for s-Ge QWFET compared to r-Ge MOSFET

Si cap vs. GeOx IL

Cap Layer

✓ 10A Si

▪ Limits EOT Scaling



Ge QW/10A Si cap/5A Al_2O_3/22A HfO_2

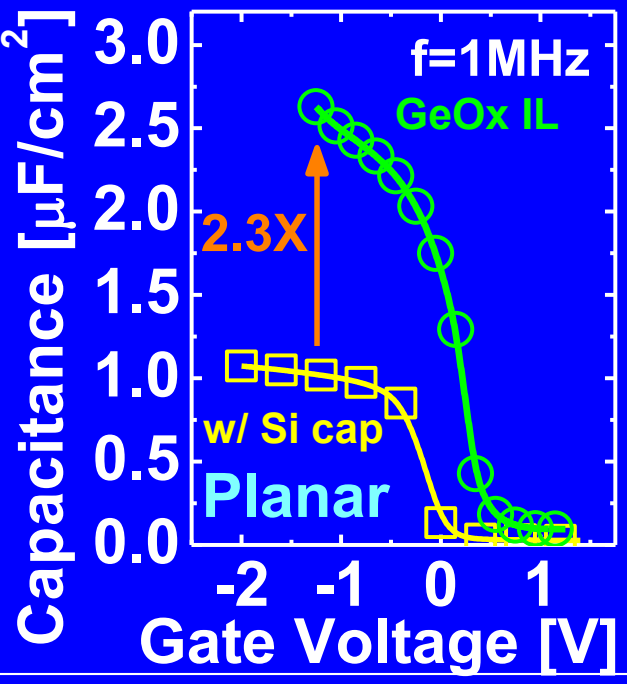
➢ Si cap passivation limits EOT scaling

Si cap vs. GeOx IL

Cap Layer

✓ 10A Si
- Limits EOT Scaling

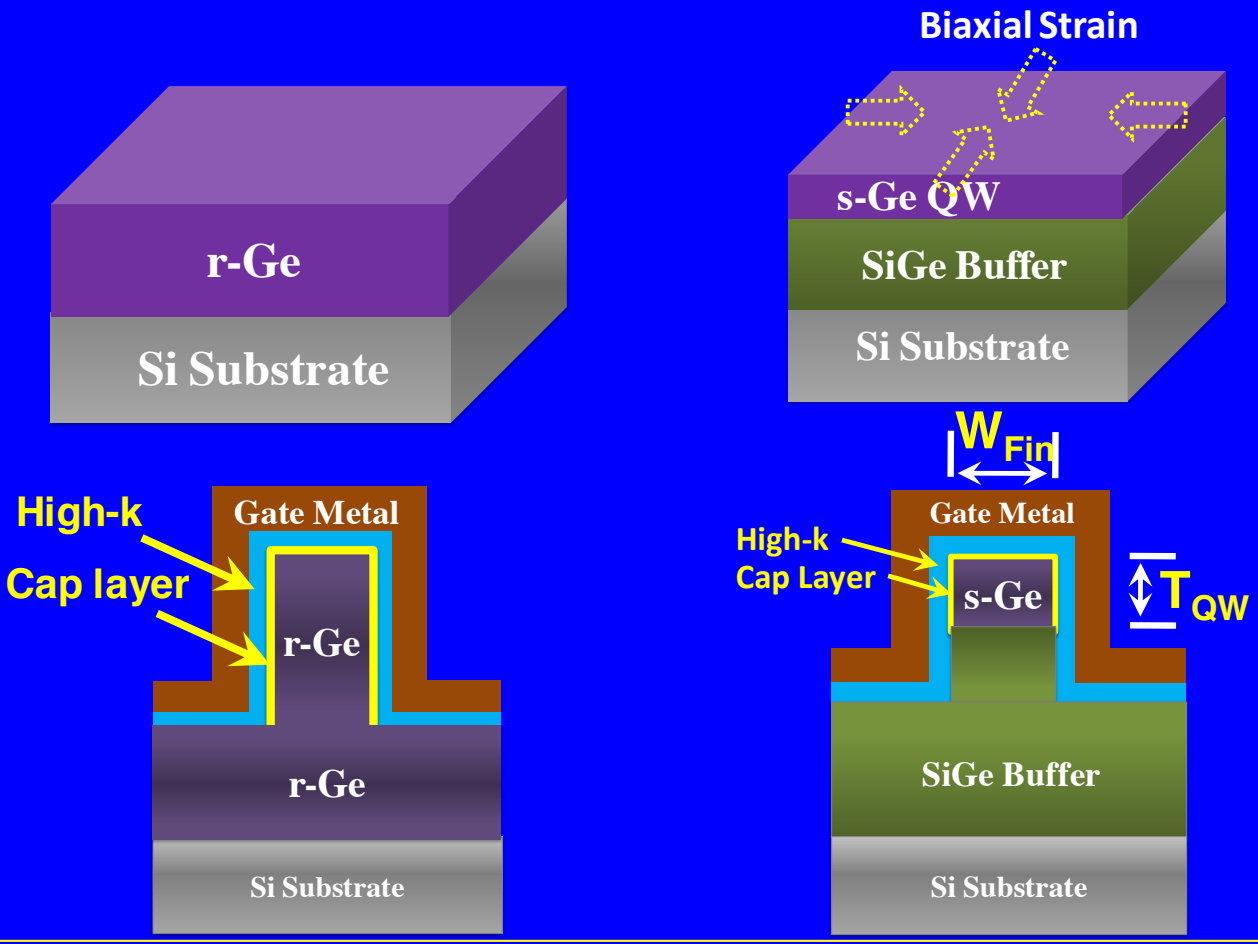
✓ 6A GeOx
- Low EOT, low D_{IT} achieved



Ge QW/6A GeOx IL/5A Al_2O_3/22A HfO_2

- GeOx IL passivation instead of Si cap realized
- Low EOT of 0.83nm obtained on Ge QW

Bulk FinFET vs. QW FinFET



➢ Both W_{fin} and T_{QW} determine strain in Ge QW

S-Ge QW FinFET Highlights

Channel Strain

❑ Asymmetric Uniaxial strain;

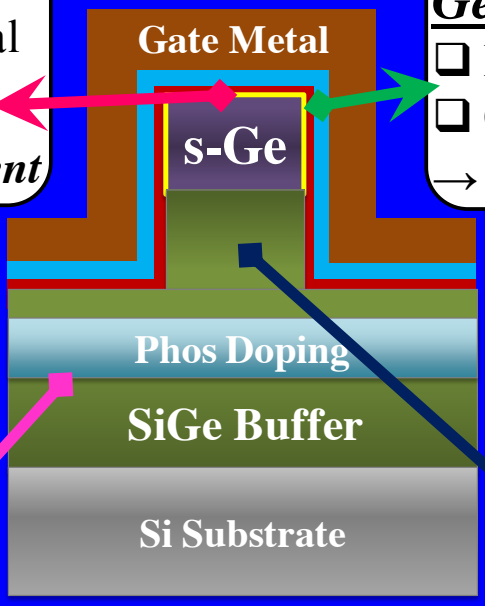
→ μ_{Hole} *Enhancement*

Ge-Passivation

❑ In-situ H-Plasma clean

❑ Controlled sub-nm GeO_x;

→ *Low* D_{IT} *Ultrathin EOT*



SiGe Buffer Optimization

❑ Retrograde Phos Doping;

→ *Eliminate parallel channel*

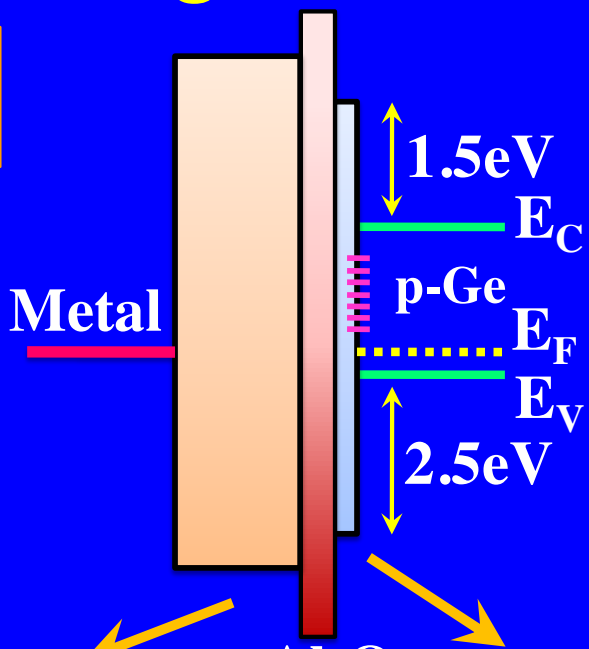
Scaled FinFET

❑ 20nm Fin Width;

→ *E-Mode Operation*

Tri-Layer High-κ Gate Stack

GOAL:
Sub-1 nm (EOT)

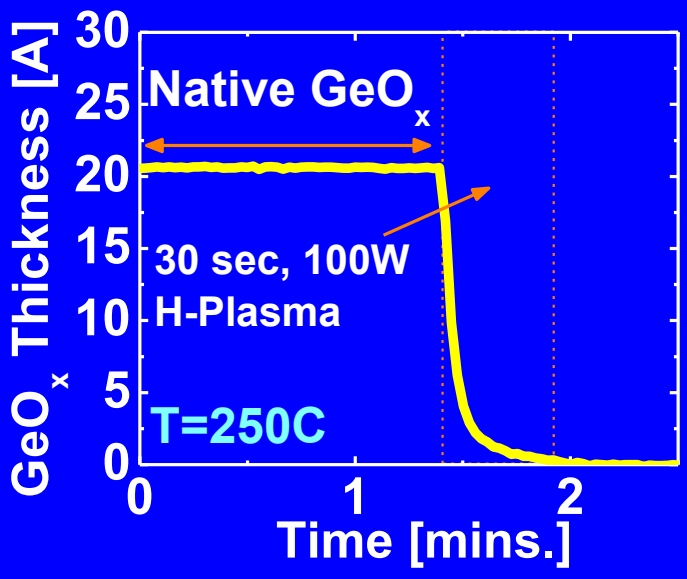


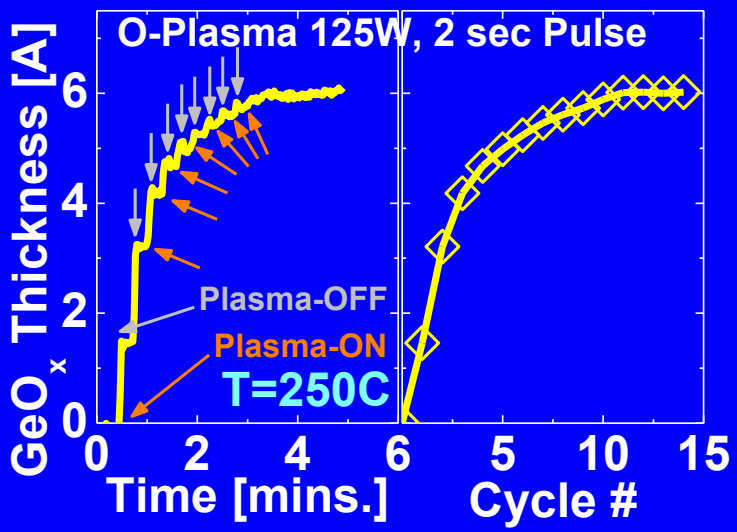
HfO_2
- Reduce gate leakage

Al_2O_3
- Prevent HfO_2-GeO_x intermixing

GeO_x
- Reduce D_{IT}
- Low temperature process prevent Si-Ge interdiffusion

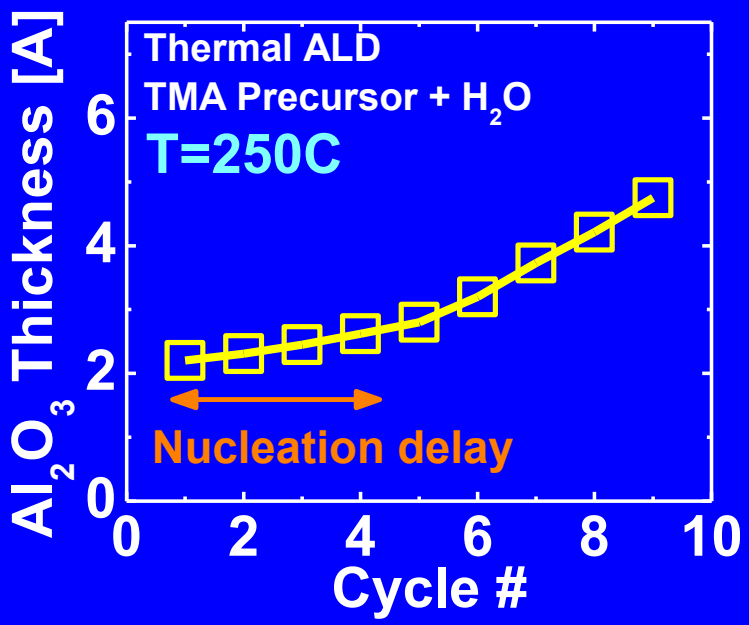
Tri-Layer Process Flow

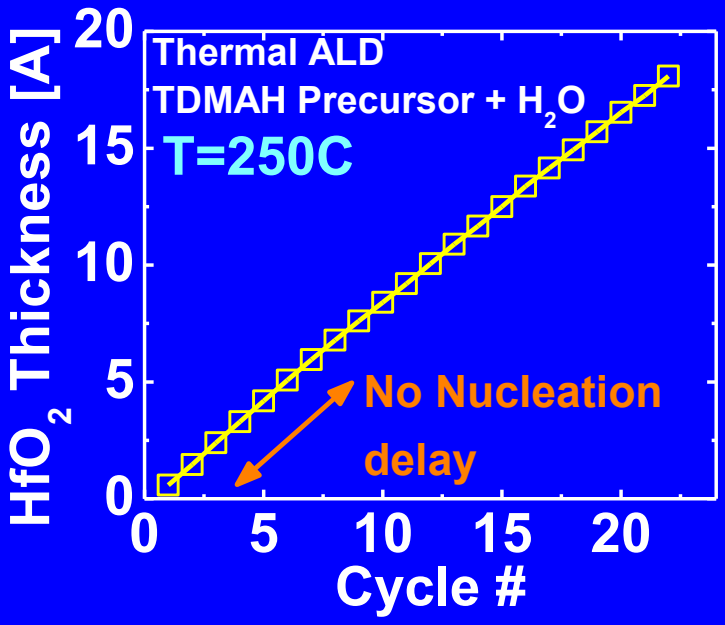




- Removal of native GeO_x with low power H-Plasma etch
- High quality, uniform GeO_x IL formed using low power O-Plasma pulse

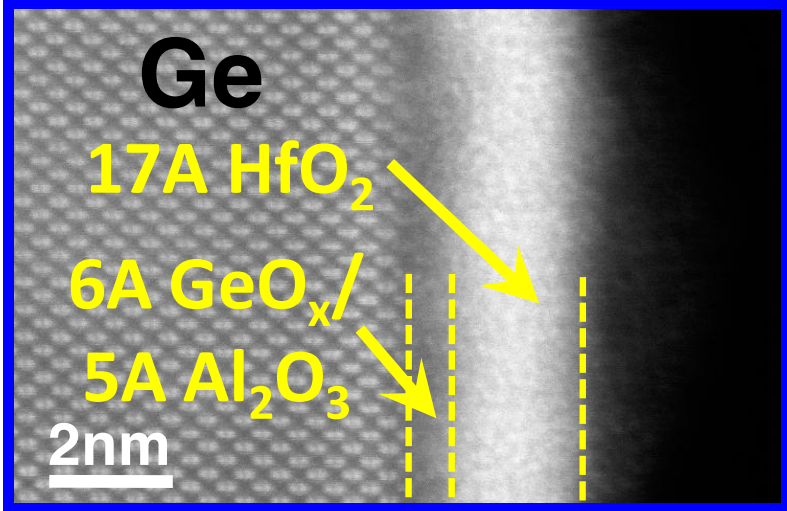
Tri-Layer Process Flow

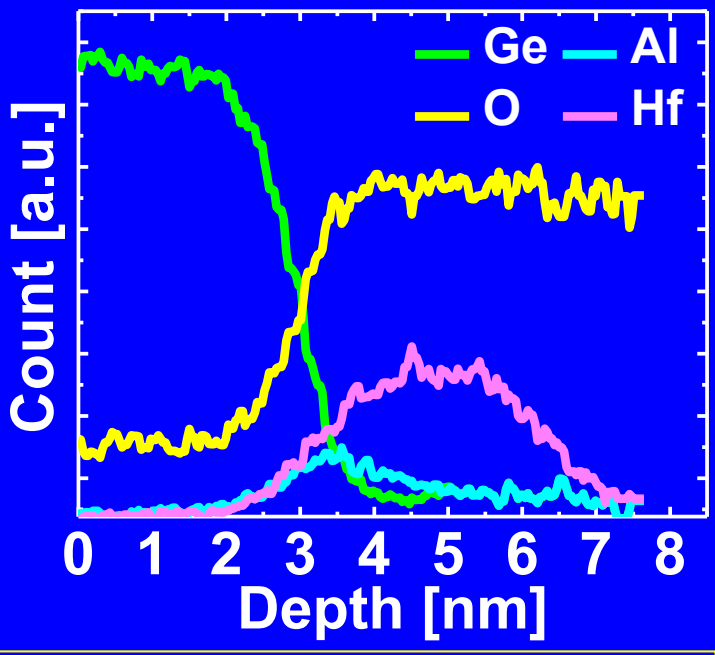




➢ Ultrathin Al_2O_3 cap layer and HfO_2 high-κ deposited using Thermal ALD

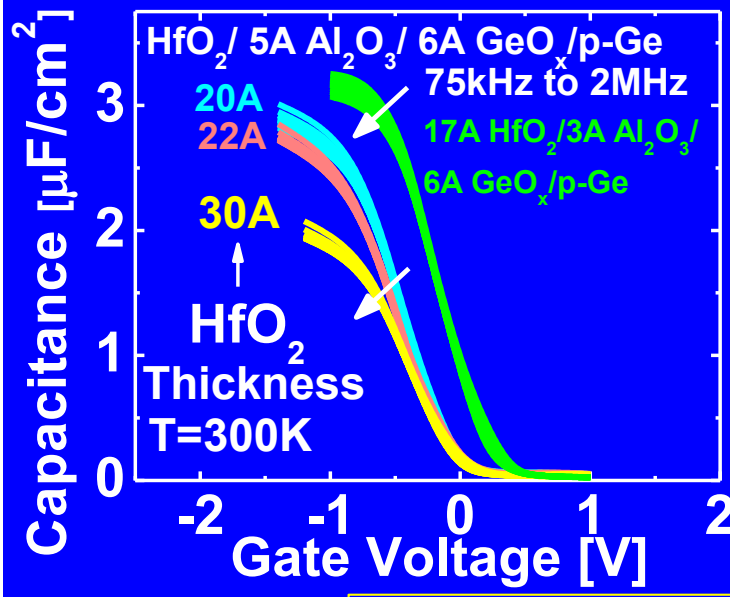
Tri-Layer High-κ: In-situ GeO_x Passivation

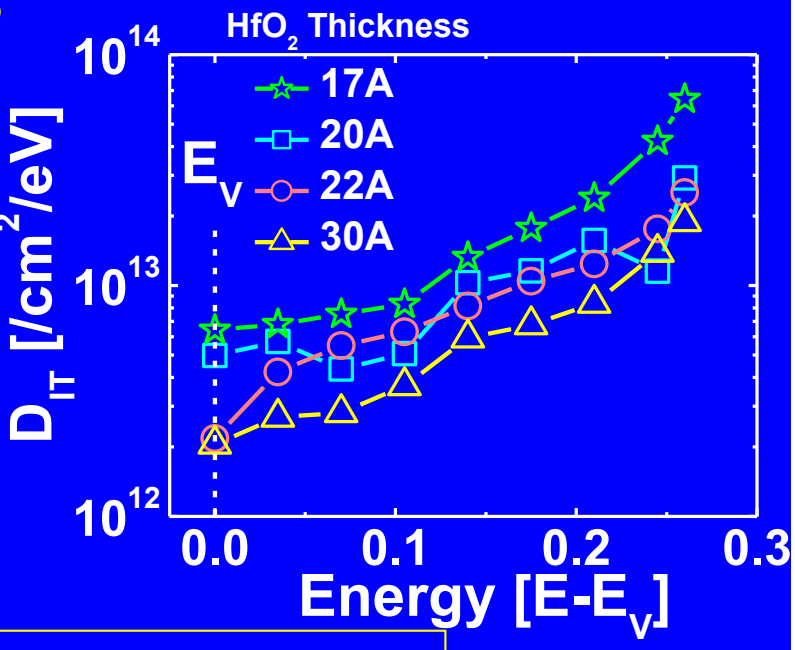




- In-situ plasma clean and GeO_x IL realized for enhanced surface passivation
- Low power plasma reduces surface roughness

Tri-Layer High-κ/Ge C-V Characteristics

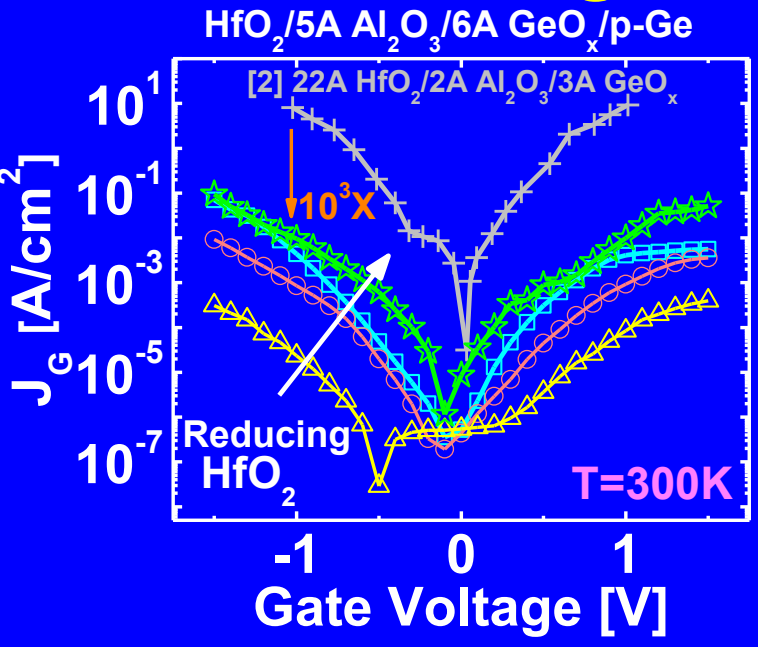


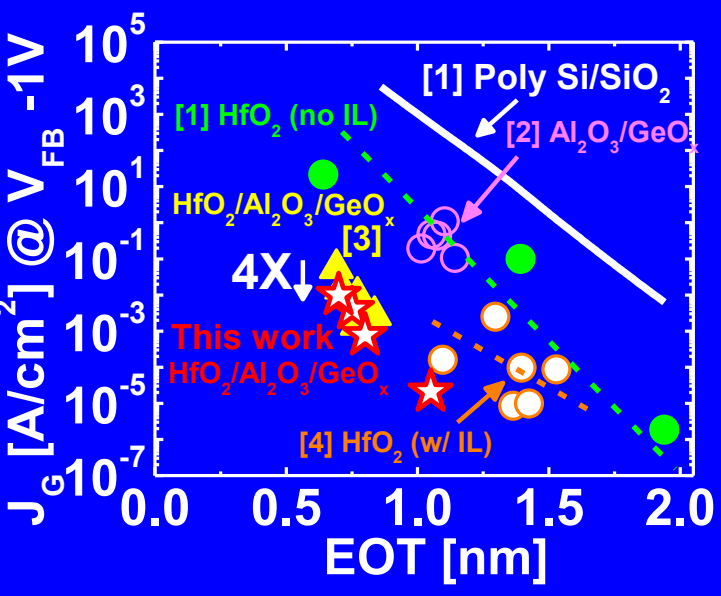


HfO_2/5A Al_2O_3/6A GeO_x/p-Ge

- EOT of ~0.72nm achieved
- Band-edge D_{IT} from low 10^{12} to 10^{13} /cm²/eV in midgap observed

Gate Leakage Reduction

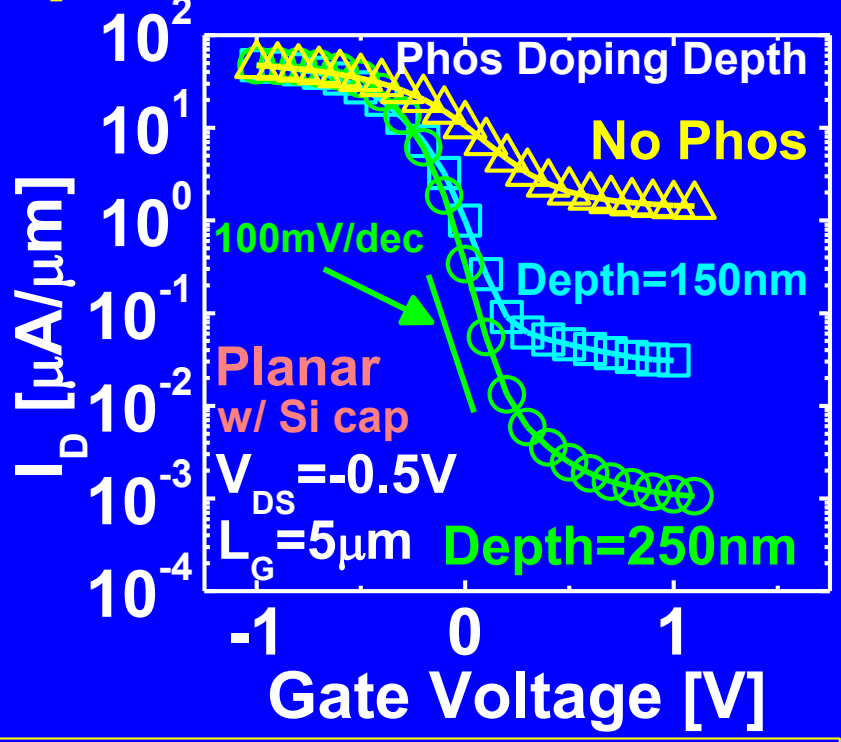




➢ **Low gate leakage of 10^{-2} A/cm² ($V_G=V_{FB}$-1V) obtained at 0.72nm EOT with Tri-layer gate stack**

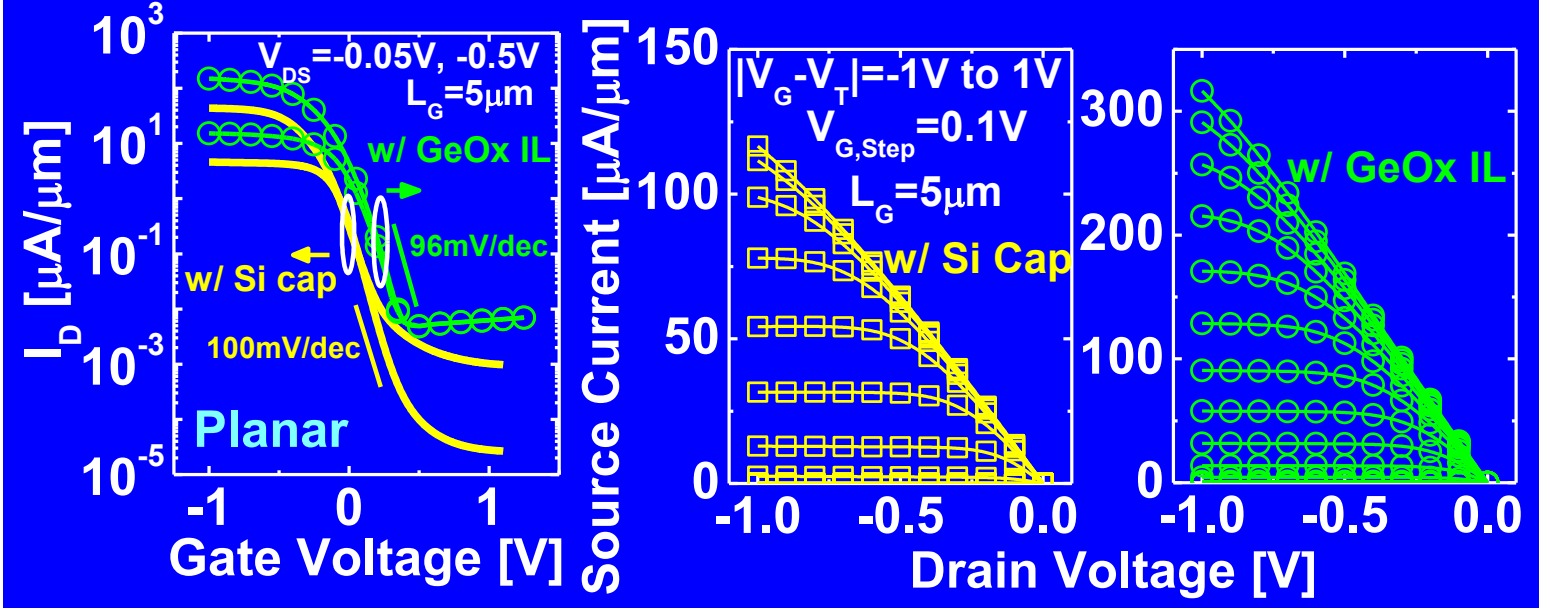
[1] C. Choi et al., EDL 2004 [2] R. Zhang et al., IEDM 2011
[3] R. Zhang et al., IEDM 2013 [4] R. Xie et al., IEDM 2008

s-Ge QW on Silicon: SiGe Buffer Optimization



➢ 10^3X I_{OFF} reduction with deeper Phos doping in SiGe buffer with no degradation in I_{ON}

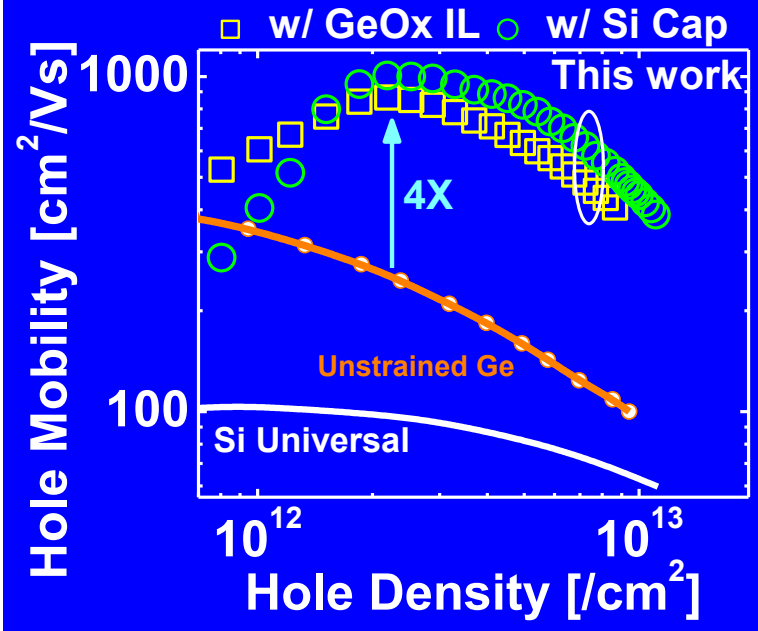
QW MOSFET with Tri-layer High-k

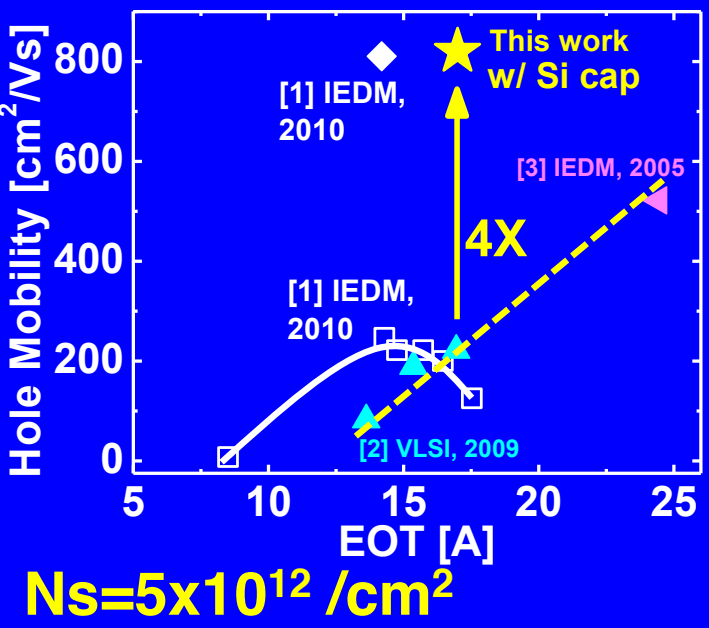


Ge QW/Si Cap or GeO_x IL/5A Al_2O_3/22A HfO_2

- 2X higher I_{ON} (V_{DS}=-0.5V) with 96 mV/dec subthreshold slope obtained with Tri-layer high-κ

Drift Mobility



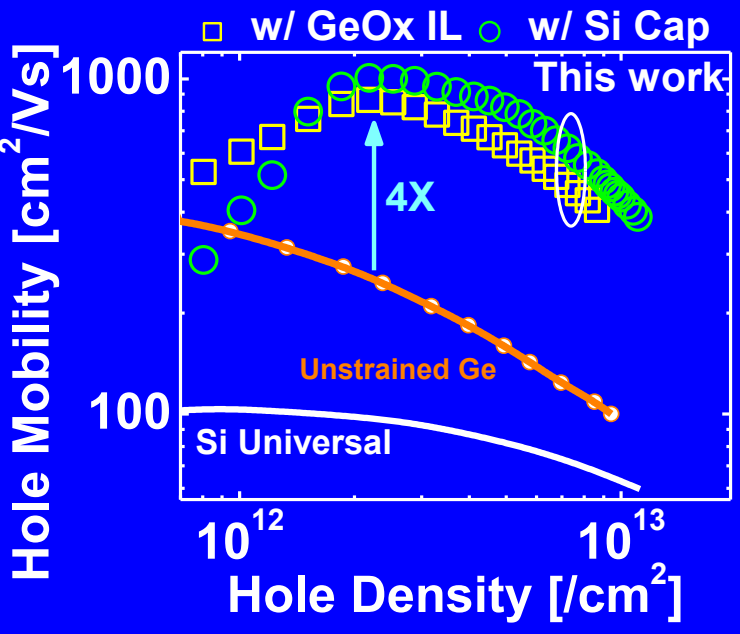


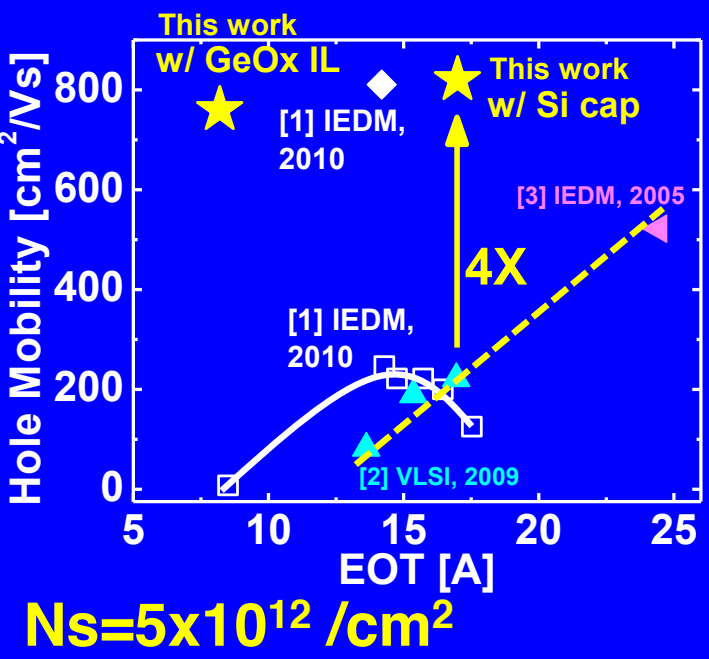
$N_s = 5 \times 10^{12}$ /cm²

➢4X higher hole mobility compared to r-Ge achieved

[1] R. Pillarisetty et al., IEDM 2010 [2] J. Mitard et al., VLSI 2009
[3] O. Weber et al., IEDM 2005

Drift Mobility





Ns=5x10¹² /cm²

- **Highest hole mobility at lowest EOT achieved with GeO_x IL**

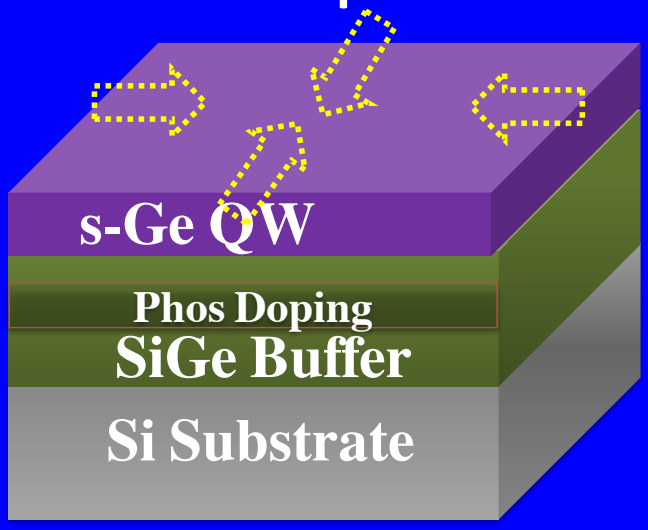
[1] R. Pillarisetty et al., IEDM 2010 [2] J. Mitard et al., VLSI 2009
[3] O. Weber et al., IEDM 2005

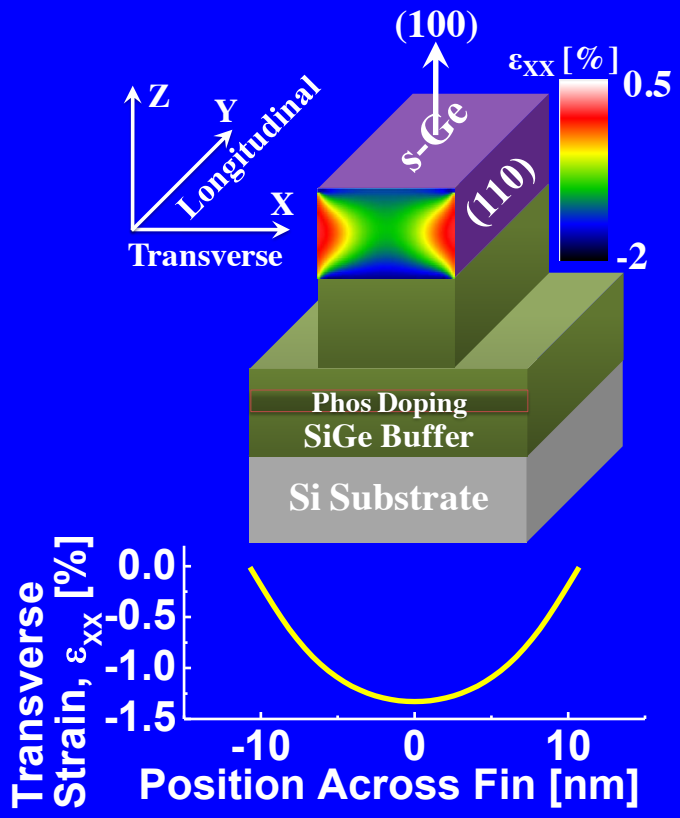
Outline

Integrate s-Ge QW and Tri-layer high-κ in a FinFET

Asymmetric Strained FinFET

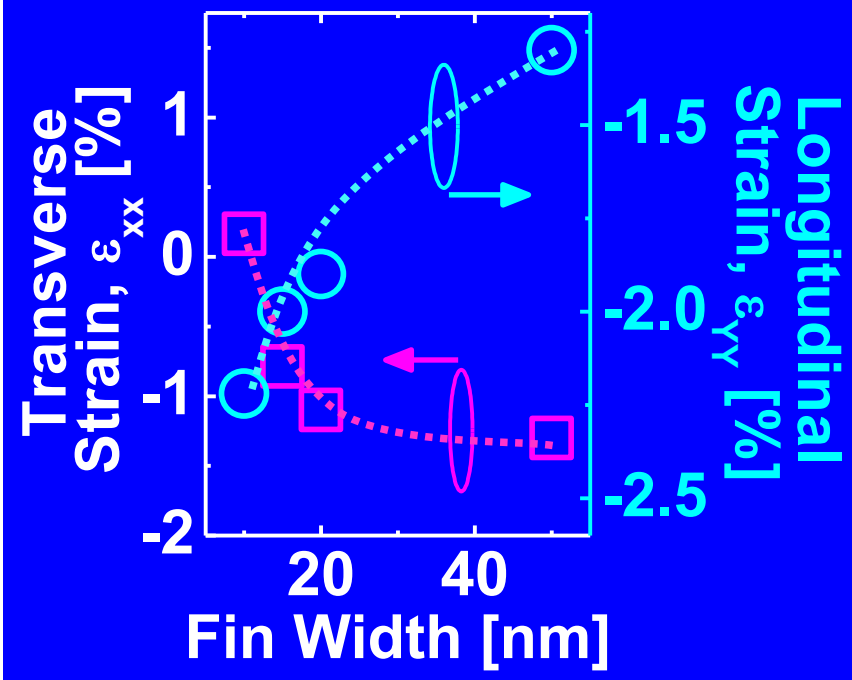
Biaxial Compressive Strain

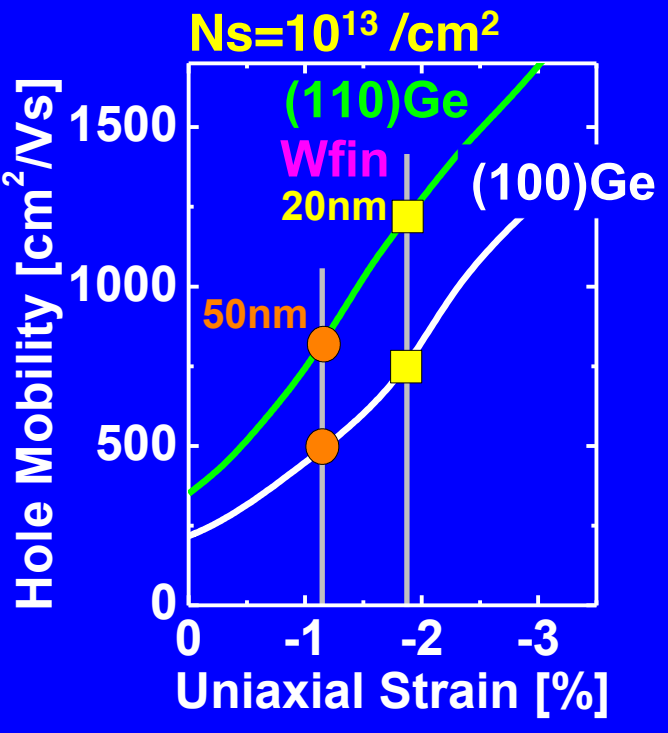




➢ Strain relaxation near sidewall results in net uniaxial strain along the channel direction

Fin Mobility



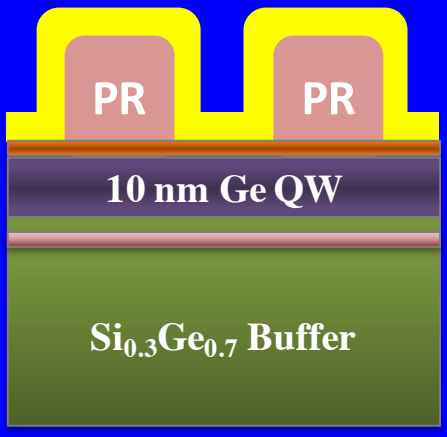


* M. Chu et al., Annu. Rev. Mater. Res. 2009

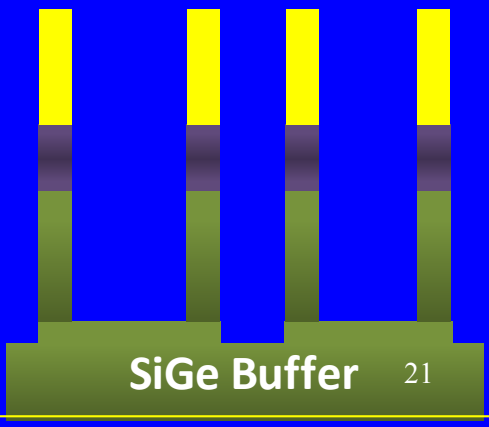
➢ **Mobility enhancement due to increasing uniaxial compressive strain with reducing W_{fin}**

FinFET Fabrication Flow

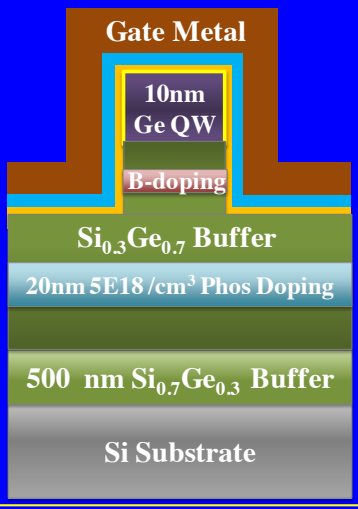
Fin Pattern +
Hardmask Deposition



Dry RIE Etch

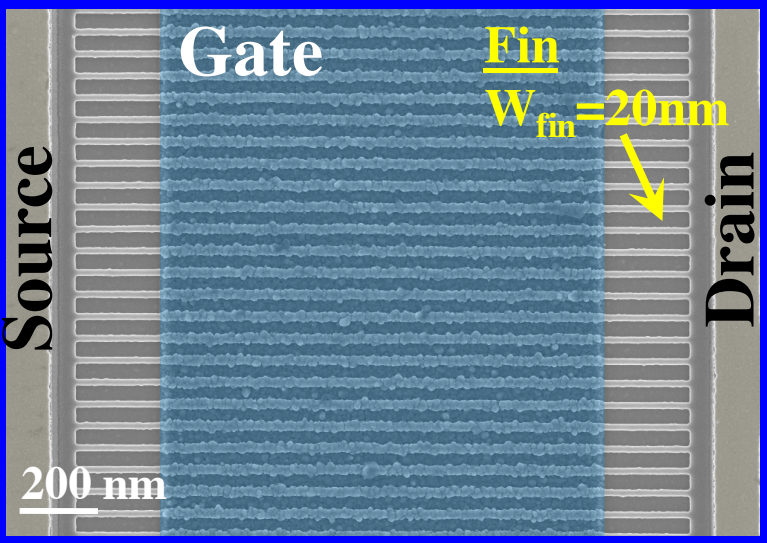


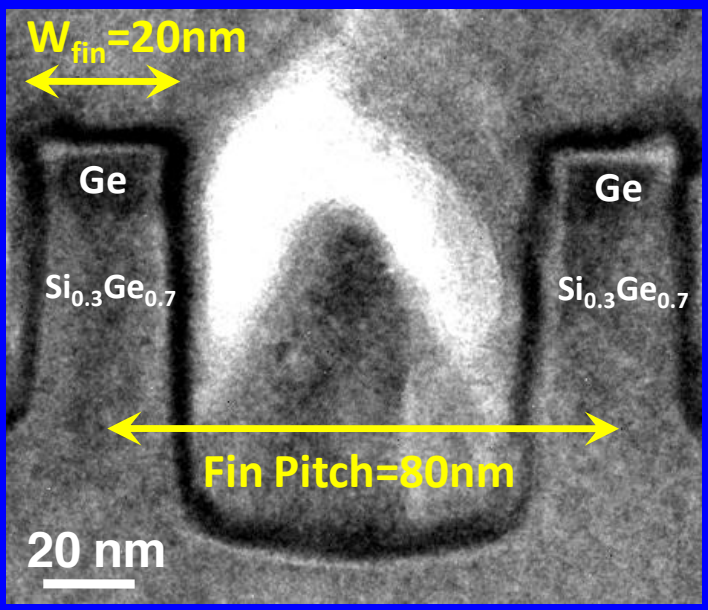
Tri-Layer High-k +
Gate Patterning



➢ FinFET fabrication using Sidewall Image Transfer (SIT)

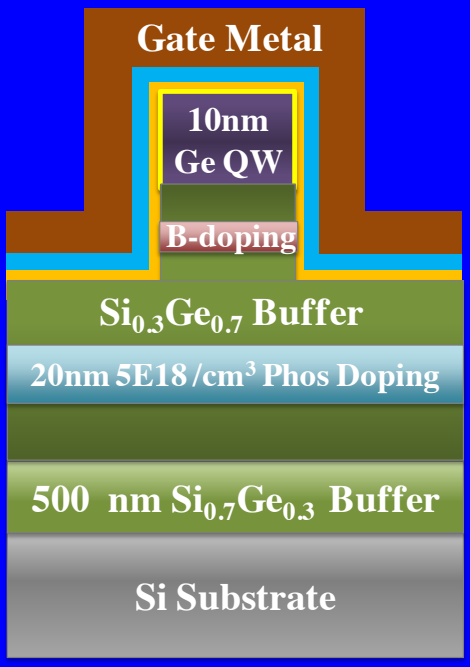
FinFET Fabrication : SEM

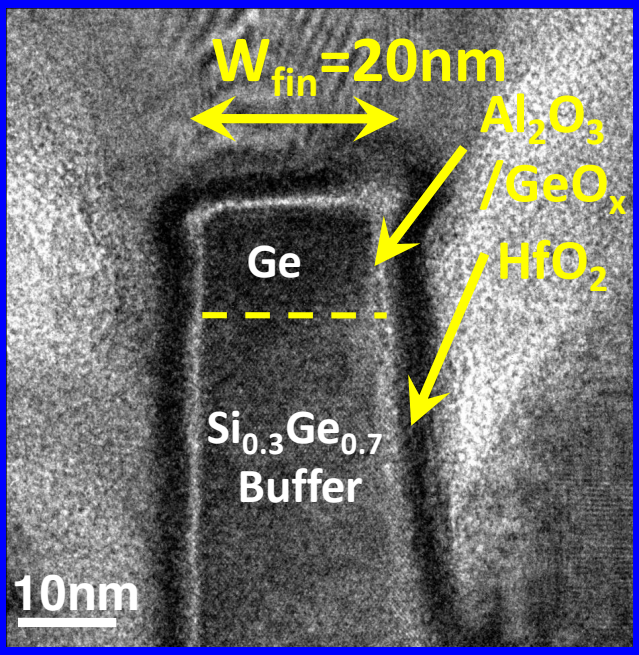




- W_{fin}=20nm; Fin pitch = 80nm; Tri-layer high-κ realized on s-Ge QW with SIT process

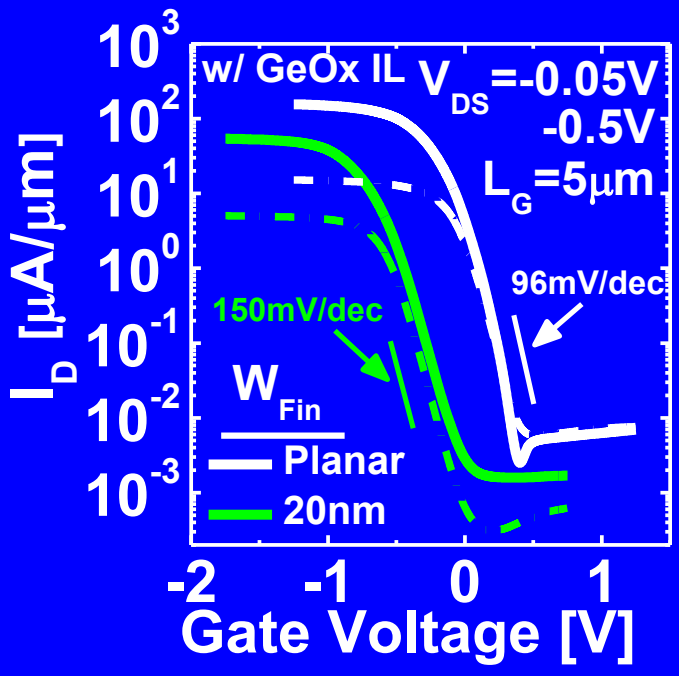
FinFET Fabrication : TEM

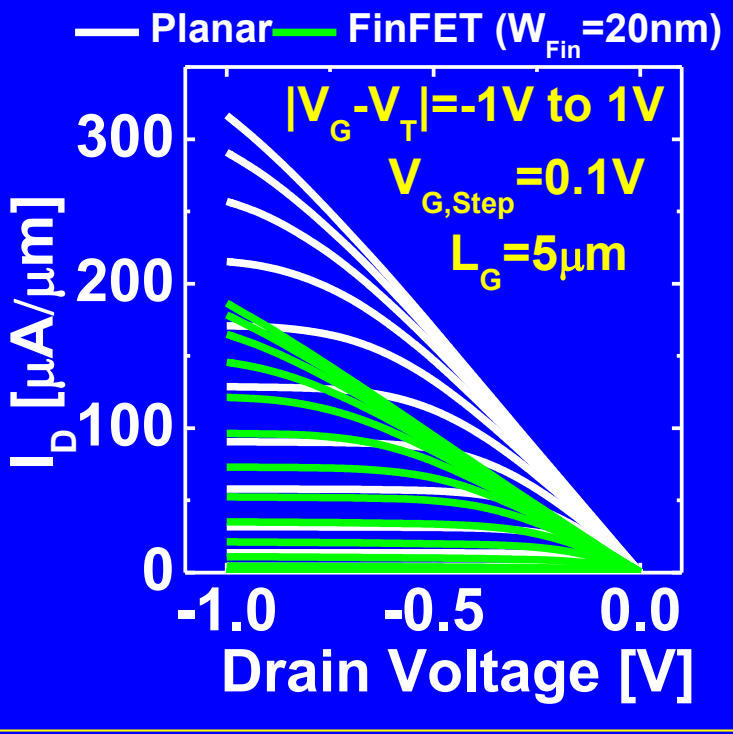




➢ Vertical fin sidewall profile achieved for W_{fin}=20nm QW FinFET

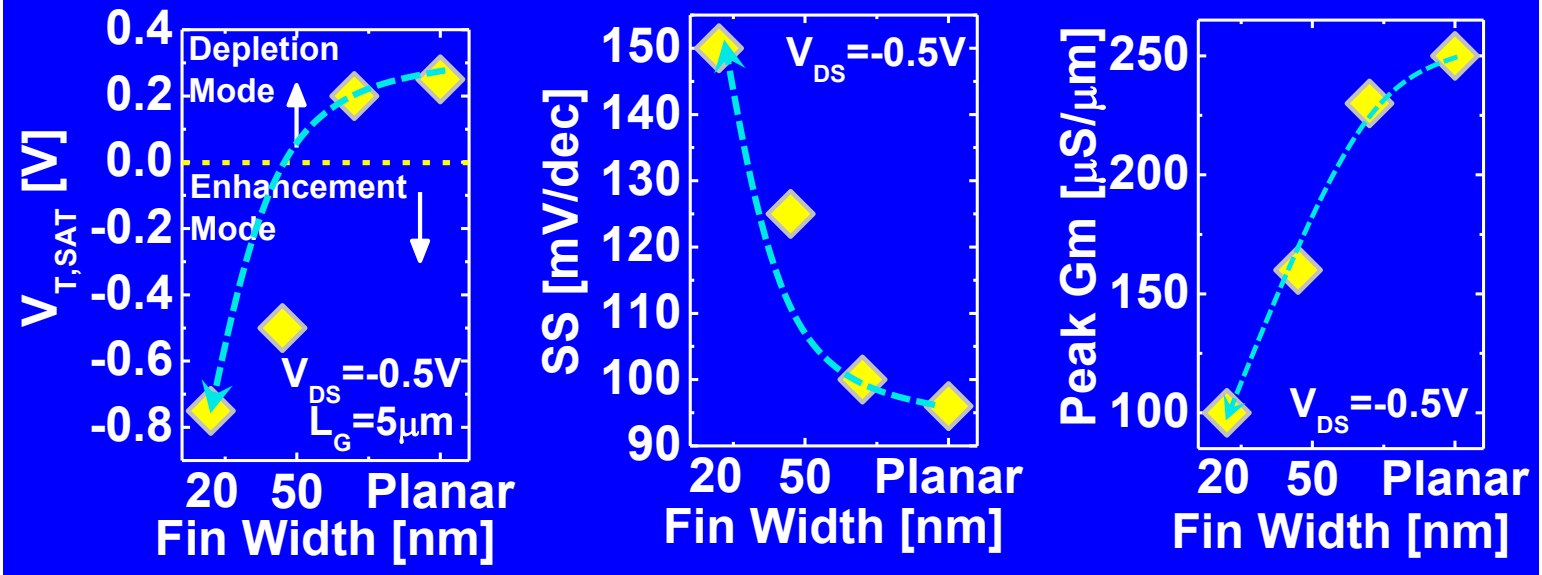
Long Channel FinFET Performance





➢ E-Mode (V_T=-0.75V); I_{ON}/I_{OFF}~10^4; SS=150mV/dec for W_{fin}=20nm FinFET with Tri-layer high-κ obtained

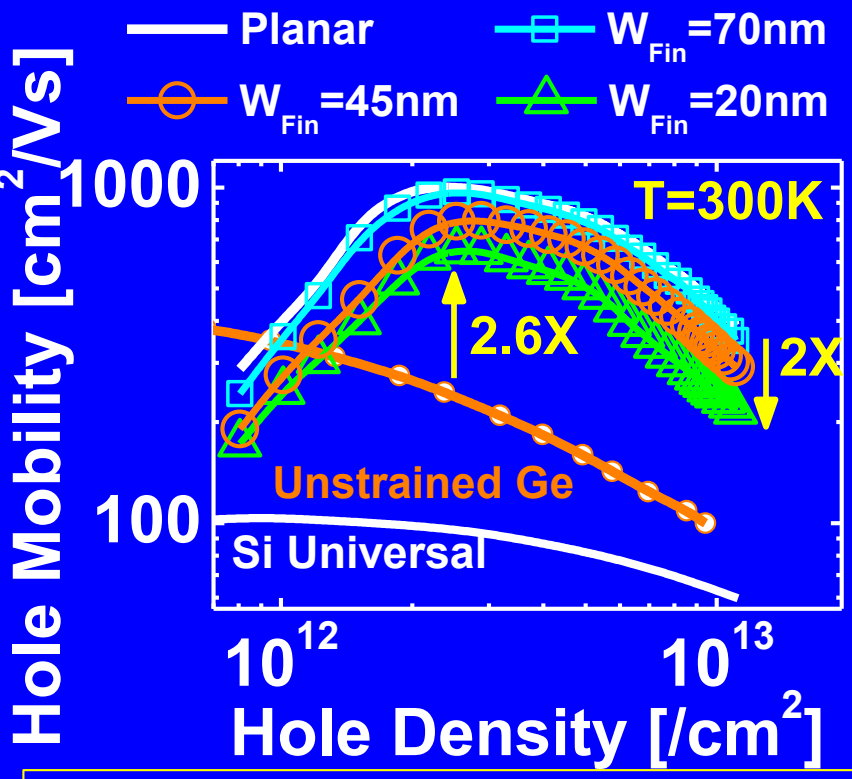
E-Mode QW FinFET Operation

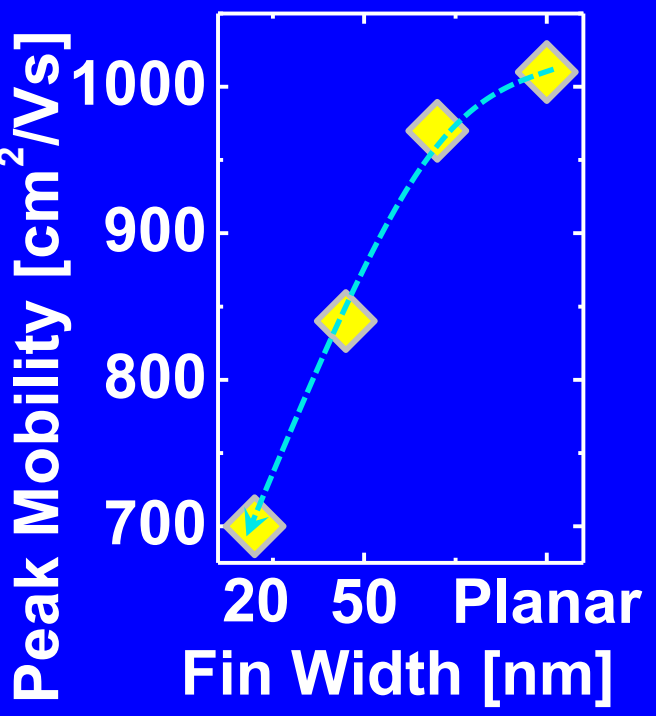


W_{fin}=20nm; L_G=5μm; 10 fins/μm

- E-Mode operation for W_{fin}=45nm and 20nm
- Degradation in SS (36%) and peak Gm (60%) with reducing W_{fin}

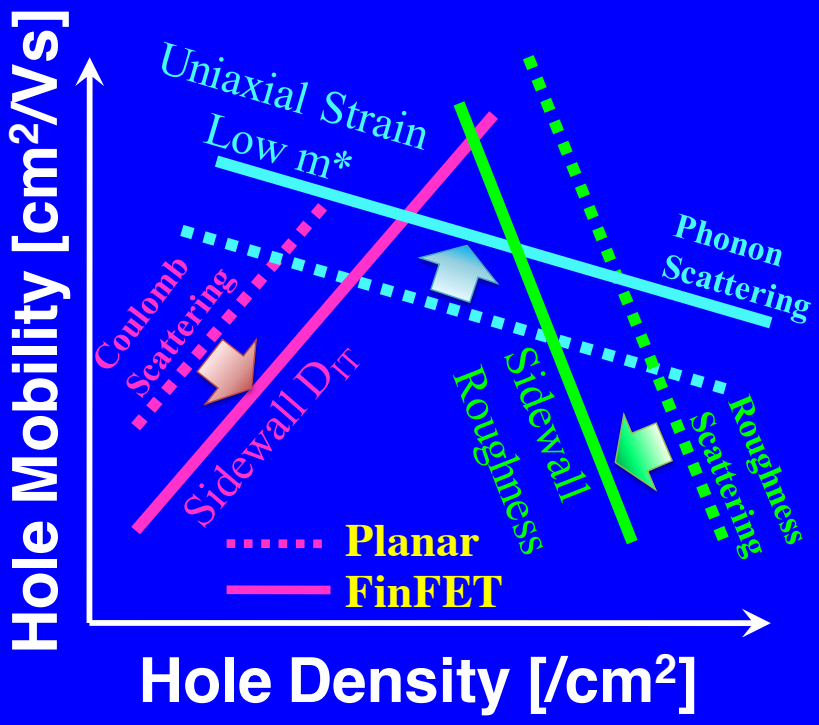
Fin Mobility





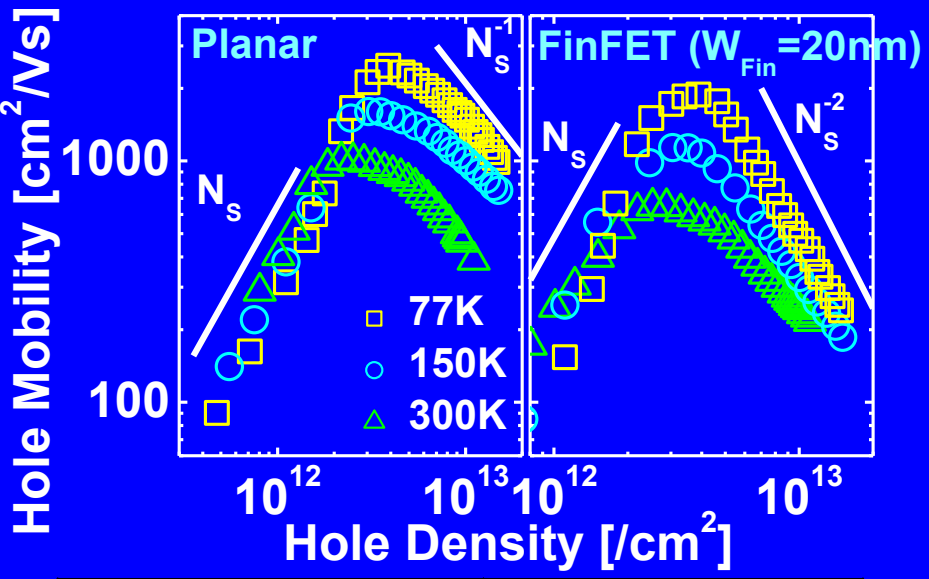
- 2.6X higher μ_{Peak} obtained with s-Ge QW FinFET (W_{fin}=20nm) compared to unstrained-Ge

FinFET Hole Transport Highlights



➢ Reducing sidewall D_{IT} and sidewall roughness key to achieving higher fin mobility

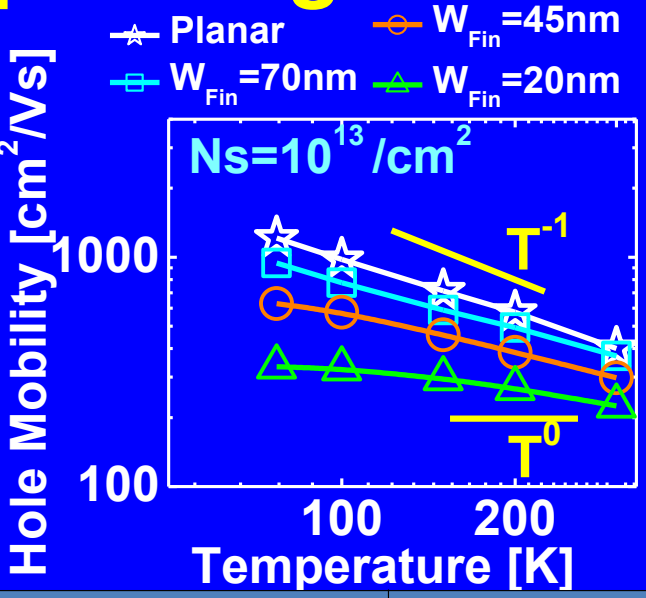
Transport Degradation



Scattering Mechanism	*Ns and T Dependence*
Acoustic Phonon	$Ns^{-1/3}$ T
Sidewall Roughness	Ns^{-2} T^0
Remote Charge Scattering	$Ns^{3/2}$ T^0

➢ **Strong Ns dependence for FinFET at 77K indicates sidewall roughness scattering**

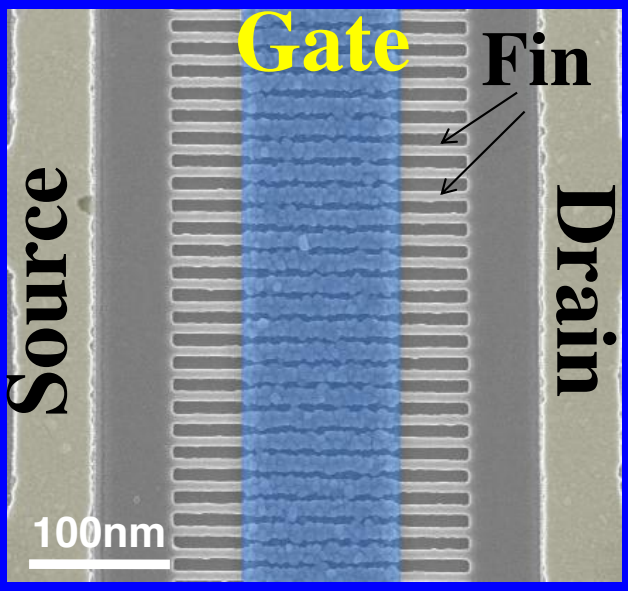
Transport Degradation

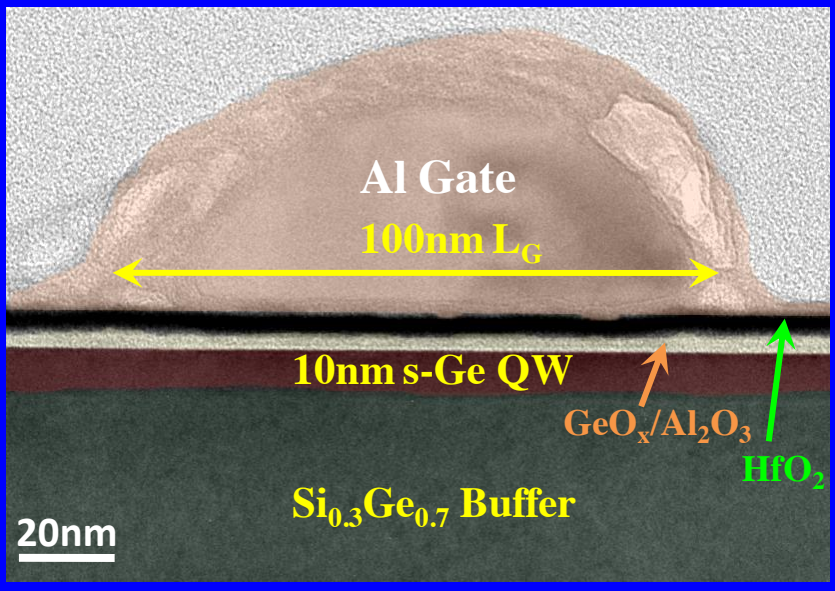


Scattering Mechanism	*Ns and T Dependence*
Acoustic Phonon	$Ns^{-1/3}$ T
Sidewall Roughness	Ns^{-2} T^0
Remote Charge Scattering	$Ns^{3/2}$ T^0

➢ Reduced temperature dependence of mobility for FinFET is indicative of sidewall roughness

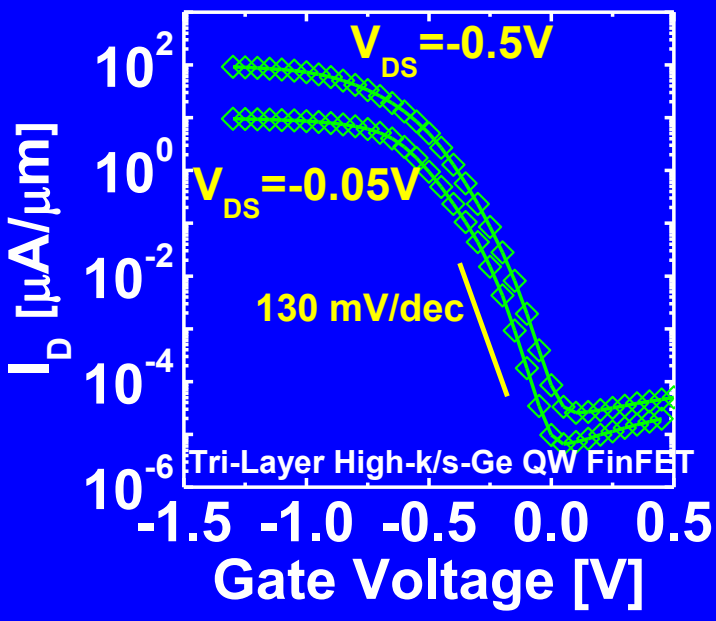
Short Channel Ge QW FinFET

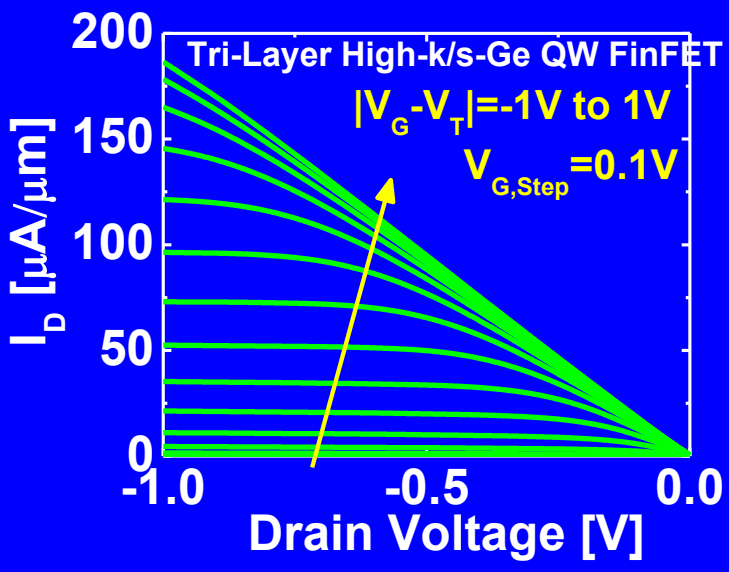




➢ Short channel FinFET with gate length of 100nm and Tri-layer high-κ fabricated using SIT

Short Channel FinFET Performance

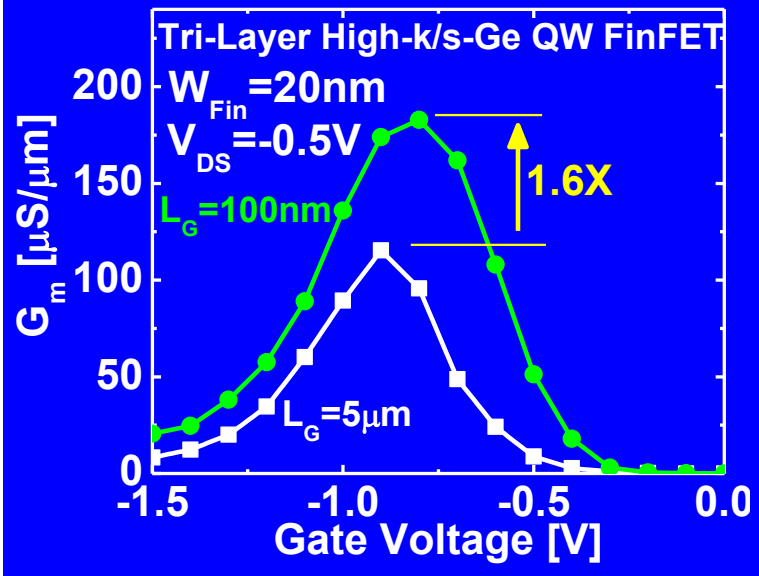


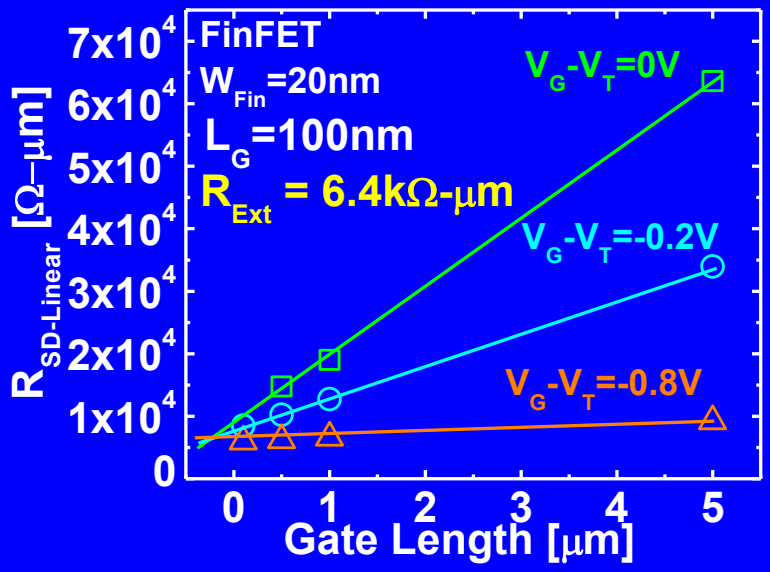


W_{fin}=20nm; L_G=100nm; 10 fins/μm

- **E-Mode L_G=100nm QW FinFET (W_{fin}=20nm) with with I_{ON}=90μA/μm (V_G-V_T=-0.5V) and SS=130 mV/dec**

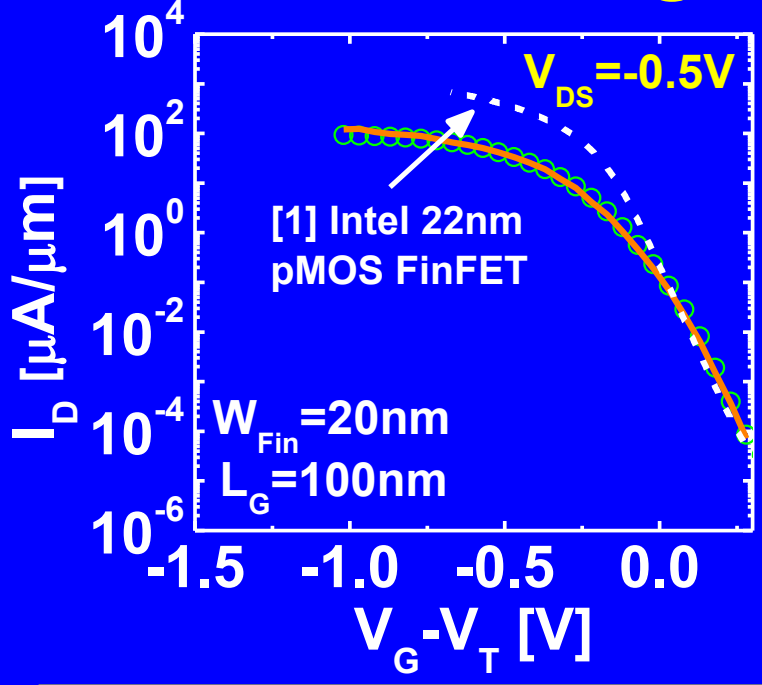
Transconductance





- Peak G_m enhancement of 1.6X observed for L_g=100nm QW FinFET
- High R_{access}=6.4kΩ-μm limits short channel performance

Benchmarking



$$R_{channel} = R_{Total} - R_{ext}$$

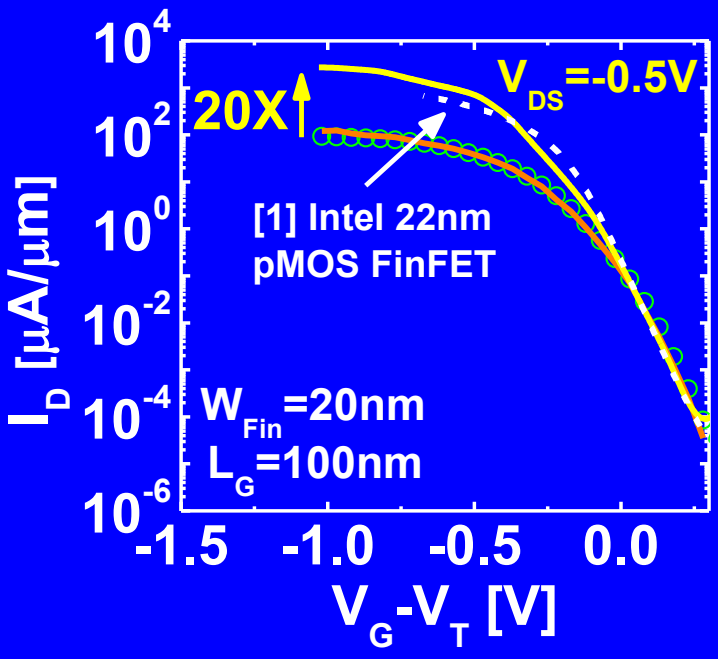
$$\frac{I_D}{W} = Q_{ixo}(V_G) \times \langle v_{inj} \rangle$$

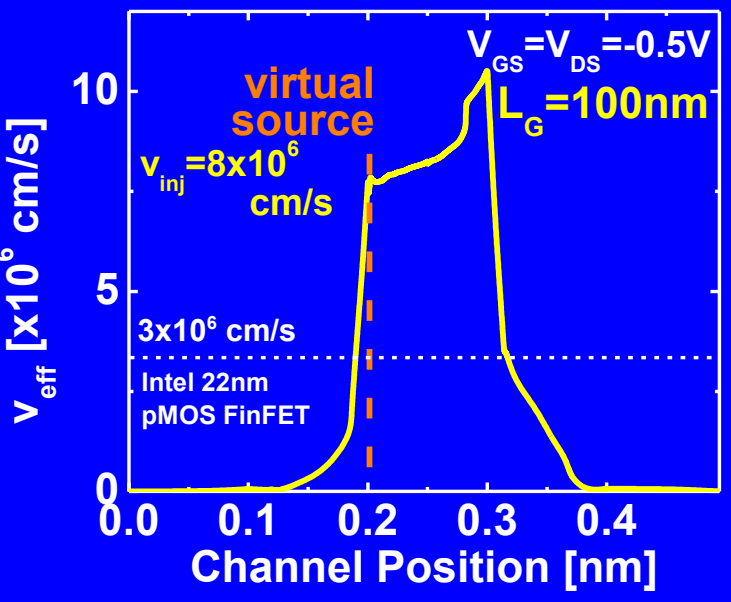
$$\frac{1}{\langle v_{inj} \rangle} = \frac{1}{\mu_{Eff} V_D / L} + \frac{1}{v_{sat}}$$

➢ 3D simulation model calibration to experiment performed using self-consistent Poisson-Schrodinger solver for QW FinFET

[1] C. Auth et al., VLSI 2012

Performance Projection





R_{ext} = 6.4 kΩ-μm -> 200 Ω-μm

- v_{inj} estimated at 8x10^6 cm/s for s-Ge QW short channel FinFET at L_G=100nm

[1] C. Auth et al., VLSI 2012

Conclusion

- Asymmetric uniaxial strain along fin (1.8%) results in high hole mobility in s-Ge QW FinFET

- In-situ H-plasma clean and Tri-layer High-k gate stack developed: Low leakage (10^{-2} A/cm^2), low D_{IT} at ultrathin EOT (0.72nm) obtained

- Mobility of 770 cm^2/Vs at 0.83nm EOT achieved with s-Ge QW MOSFETs

- E-Mode 1.3% s-Ge QW FinFET with W_{fin}=20nm and μ_{Hole}=700 cm^2/Vs (2.6X over r-Ge) achieved with Tri-layer high-k

- s-Ge QW FinFET shows 8x10^6 cm/s v_{inj} (simulation) with lower R_{access}

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