Enhancement Mode Strained (1.3%) Germanium Quantum Well FinFET (W_{Fin}=20nm) with High Mobility (μ_{Hole}=700 cm^2/Vs), Low EOT (~0.7nm) on Bulk Silicon Substrate

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Abstract

Compressively strained Ge (s-Ge) quantum well (QW) FinFETs with $Si_{0.3}Ge_{0.7}$ buffer are fabricated on 300mm bulk Si substrate with 20nm W_{Fin} and 80nm fin pitch using sidewall image transfer (SIT) patterning process. We demonstrate (a) in-situ process flow for a tri-layer high-κ dielectric $HfO_2/Al_2O_3/GeO_x$ gate stack achieving ultrathin EOT of 0.7nm with low D_{IT} and low gate leakage; (b) 1.3% s-Ge FinFETs with Phosphorus doped $Si_{0.3}Ge_{0.7}$ buffer on bulk Si substrate exhibiting peak μ_h=700 cm^2/Vs, μ_h=220 cm^2/Vs at 10^{13} /cm^2 hole density. The s-Ge FinFETs achieve the highest $\mu*C_{max}$ of $3.1x10^{-4}$ F/Vs resulting in 5x higher I_{ON} over unstrained Ge FinFETs.

Introduction

Ge pMOSFETs on bulk silicon substrate are a promising solution for improving the p-channel FET performance [1]. It is imperative to optimize the relaxed SiGe buffer counter doping with Phosphorus to achieve reliable isolation, maximize the uniaxial compressive strain in extremely scaled s-Ge fin to enhance μ_h, incorporate a gate stack with low EOT and D_{IT}, and mitigate the sidewall roughness to prevent μ_h reduction. In this work, we investigate the optimum depth of location of the buffer Phos doping, tri-layer optimization of an ultrathin EOT gate stack without Si interlayer (IL) (Fig. 1), residual uniaxial strain retention in scaled fins of a s-Ge QW heterostructure (Fig. 2), and temperature dependent μ_h characterization in s-Ge fins to quantify the effective mobility degradation. We experimentally evaluate enhancement mode, scaled s-Ge QW FinFETs with W_{Fin}=20nm and 80nm fin pitch to demonstrate record $\mu*C_{max}$ product of $3.1x10^{-4}$ F/Vs which is 2X higher than best reported till date.

Tri-layer Gate Stack

The tri-layer gate stack design and fabrication is shown in Fig. 3. GeOx is used to ensure low D_{IT} at high-κ/Ge interface, Al_2O_3 cap layer mitigates HfO_2-GeOx intermixing while HfO_2 alleviates gate leakage. The oxide layer thicknesses have been systematically optimized using in-situ spectroscopic ellipsometry (Fig. 4) to enable ultimate EOT scaling whilst preserving functionality of each layer as confirmed using TEM and EDX (Fig. 5). Direct correlation of the Al_2O_3 and HfO_2 thicknesses was established with the MOS capacitor C-V characteristics (Fig. 6). Excellent C-V response with ultrathin EOT of 0.72nm exhibiting the lowest gate leakage (Fig. 7, 8) was obtained with 17A HfO_2/5A Al_2O_3/6A GeO_x/p-Ge gate stack. The D_{IT} analysis of these gate stacks (Fig. 9, 10) exhibited 4X better interface quality with thicker Al_2O_3 indicating more stable GeOx. Further, bulk trap density was reduced with Al_2O_3 thickness preventing HfO_2-GeOx intermixing (Fig. 11).

s-Ge FinFETs

Fig. 12 shows the schematic of s-Ge QW heterostructure on 300mm bulk Si substrate along with the fabrication process for scaled FinFETs with scaled and tight fin pitch using SIT process. Optimization of chlorine-based dry etch resulted in vertical fin sidewall profile with W_{Fin}=20nm and fin pitch of 80nm as seen under high resolution cross section TEM (Fig. 13)

Phos Doped Buffer Design

s-Ge QW MOSFETs with Phos doping placed at 150nm and 250nm depth in the $Si_{0.3}Ge_{0.7}$ buffer were characterized to identify the optimum depth of buffer counter doping. Four

orders of magnitude lower I_{OFF} was obtained for 250nm deep Phos doping compared to no Phos in buffer, with no degradation in I_{ON} (Fig. 14). This indicated effective counter doping of acceptor defects in relaxed $Si_{0.3}Ge_{0.7}$ buffer that otherwise result in parallel conduction and affect device isolation.

Si cap vs. GeO_x passivation

The incorporation of an ultrathin Si interlayer to passivate high-κ/Ge interface results in high EOT and is further incompatible with 3D FinFET manufacturing process flow. Hence, the tri-layer gate stack with GeO_x passivation after Si cap removal was deposited on s-Ge QW MOSFET and FinFET (Fig. 15). 2X higher I_{ON} was obtained with tri-layer gate stack at V_{DS}=-0.5V, L_G=5μm compared to with Si cap on s-Ge QW MOSFET. This can be attributed to 2.3X higher capacitance as measured using split-CV along with excellent modulation from accumulation to depletion. Hence, Si cap removal and tri-layer dielectric with GeOx passivation was key in realizing low EOT with low D_{IT} on s-Ge QW.

E-Mode s-Ge QW FinFET

Excellent transfer characteristics with $I_{ON}/I_{OFF}=2x10^4$ were observed on s-Ge QW FinFETs with W_{Fin}=70nm, 45nm and 20nm fabricated with SIT process after Si cap removal and deposition of tri-layer gate stack (Fig. 16(a)) showing advantage of Phos doping in buffer in addition to ultrathin EOT gate stack on high mobility s-Ge channel. The combined effect of confinement due to quantization from QW and fin patterning resulted in enhancement mode operation for W_{Fin}=45nm and 20nm s-Ge QW FinFETs (Fig. 16(b)). Experimental effective hole mobility (μ_{eff}) for s-Ge QW MOSFETs and FinFETs extracted from split-CV is summarized in Fig. 17. Highest peak μ_{eff} of 700 cm^2/Vs obtained for s-Ge FinFET with W_{Fin}=20nm shows 2.6X improvement compared to unstrained Ge [2] which is attributed to the residual asymmetric uniaxial strain in the fin as a result of patterning. In addition, 2X degradation in μ_{eff} at $N_s=10^{13}$ $/cm^2$ from planar to W_{fin}=20nm indicated increased scattering in FinFET compared to planar which was investigated using temperature dependent measurements.

Sidewall Scattering

Temperature dependent transfer characteristics for s-Ge QW FinFET with W_{Fin}=20nm showed higher modulation with temperature in the subthreshold region compared to s-Ge QW MOSFET for the same gate stack (Fig. 17, 18). Low subthreshold slope of 96 mV/dec for planar MOSFET indicates low D_{IT} at the high-κ/Ge top surface. In contrast, a degraded subthreshold slope of 150 mV/dec for s-Ge FinFET is indicative of higher D_{IT} response from the high-κ/Ge interface at the sidewall due to higher density of dangling bonds as a result of fin etch. Temperature dependent hole mobility as a function of hole density for planar MOSFET (Fig. 19) revealed Ns^{-1} dependence at 300K and 77K, which is characteristic of phonon scattering limited mobility. For s-Ge QW FinFETs, a much stronger Ns^{-2} dependence and temperature independent mobility with varying fin width (Fig. 20) revealed sidewall roughness as the dominant scattering mechanism. Optimization of fin etch to reduce the sidewall roughness is key to achieving even higher hole mobility in s-Ge QW FinFET.

Benchmarking and Conclusions

In conclusion, optimized tri-layer high-κ gate stack exhibiting ultrathin EOT=0.72nm and low gate leakage on Ge was developed. Uniaxially s-Ge QW FinFETs with W_{Fin}=20nm was demonstrated with high μ_{Peak}=700 cm^2/Vs and 220 cm^2/Vs at 10^{13} $/cm^2$ with ultrathin EOT (Fig. 21). The high mobility s-Ge channel FinFET in conjunction with scaled gate stack resulted in the highest $\mu*C_{max}$ product of $3.1x10^{-4}$ F/Vs (Table I) among high performance Ge FinFETs. The aforementioned enhancements in transport and gate stack resulted in 5X higher I_{ON} (Fig. 23) for s-Ge QW FinFET indicating promise for future alternate channel p-FinFET device technology.

Acknowledgement

This work was supported by the Pennsylvania State University Materials Research Institute Materials Characterization and Nanofabrication Laboratories and the National Science Foundation Cooperative Agreement No. ECS-0335765.

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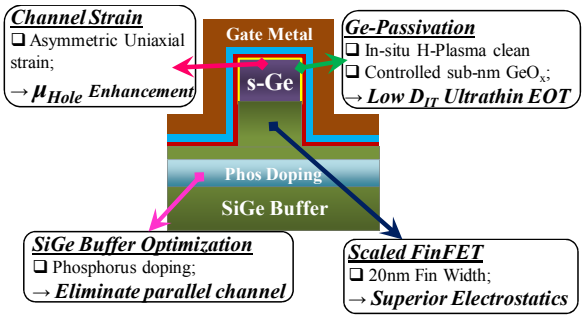

Fig. 1: (a) Schematic showing device parameters critically optimized and enhanced for high performance p-channel 1.3% compressively strained Ge QW FinFET grown on $Si_{0.3}Ge_{0.7}$ buffer on 300mm bulk Si substrate.

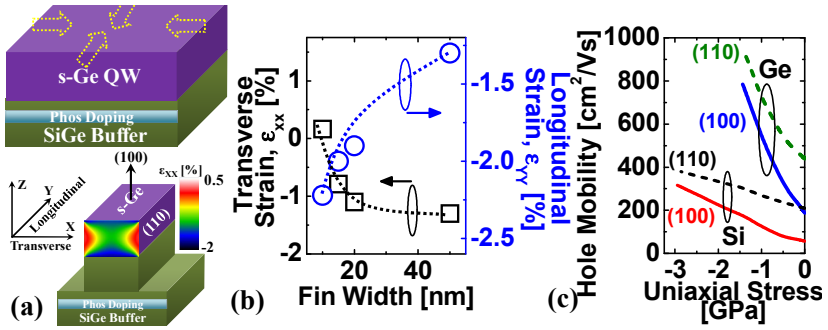

Fig. 2: Simulated transverse strain (ε_{xx}) profile for W_{Fin}=20nm Ge QW FinFET; color scale is in % strain, (b) Simulated transverse and longitudinal strain in channel as a function of fin width, (c) simulated hole effective mobility as function of uniaxial stress in channel for (100) and (110) orientated Ge and Si substrate.

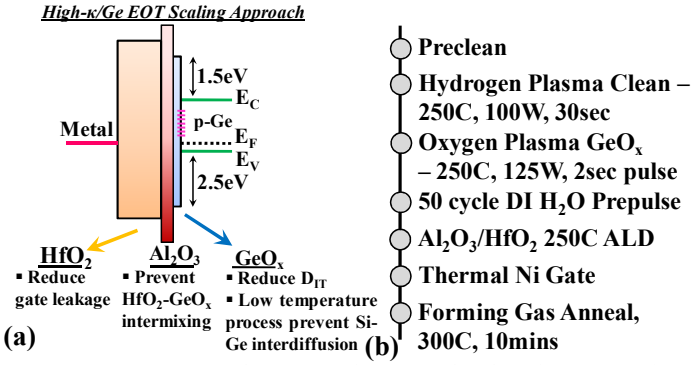

Fig. 3: (a) Schematic showing band alignment for $HfO_2/Al_2O_3/GeOx/p\text{-}Ge$ gate stack, (b) MOS capacitor fabrication flow

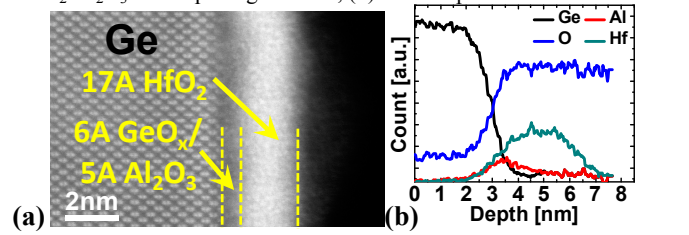

Fig. 5: (a) High resolution cross-section TEM of $HfO_2/Al_2O_3/GeO_x/Ge$ gate stack, (b) EDX line scan across the Ge gate stack

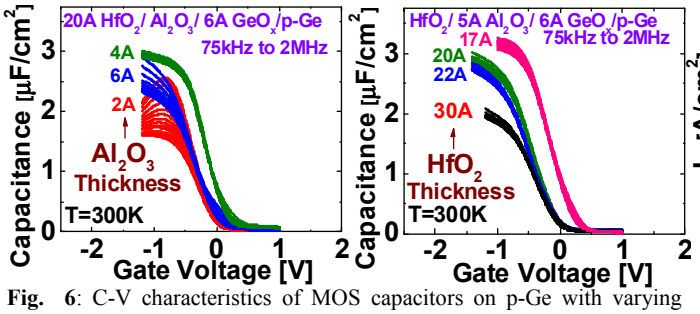

Fig. 6: C-V characteristics of MOS capacitors on p-Ge with varying Al_2O_3 cap layer thickness and HfO_2 thickness after in-situ H-Plasma clean and O-Plasma GeO_x passivation. Low EOT of 0.72nm demonstrated.

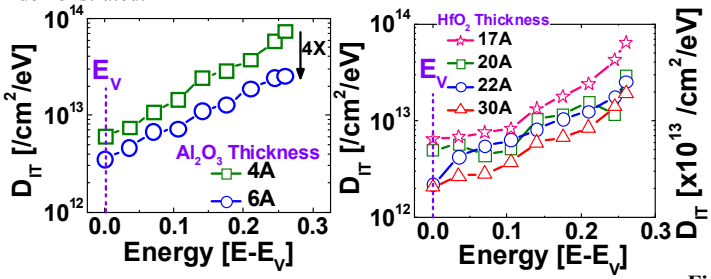

Fig. 9: Extracted density of interface states using equivalent circuit method as function of energy in the bandgap for varying Al_2O_3 and HfO_2 thickness.

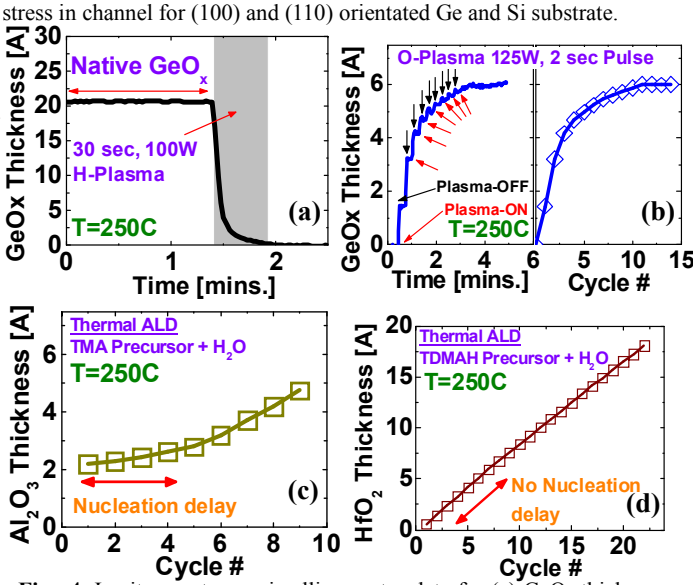

Fig. 4: In-situ spectroscopic ellipsometry data for (a) GeO_x thickness showing native oxide etch with H-Plasma, (b) controlled GeO_x formation with pulsed Oxygen Plasma, (c) Al_2O_3 cap layer deposition for diffusion barrier and nucleation layer and (d) HfO_2 deposition by thermal ALD at 250C

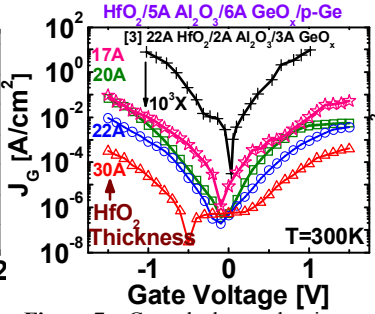

Fig. 7: Gate leakage density vs. voltage for $HfO_2/Al_2O_3/GeO_x/p\text{-}Ge$ MOS capacitors with varying HfO_2 thickness indicating 10^3X reduction

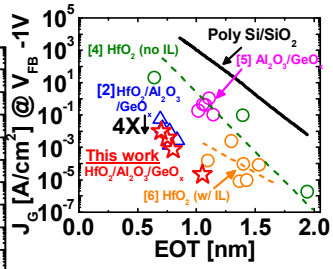

Fig. 8: Gate leakage vs EOT benchmarking of $HfO_2/Al_2O_3/GeO_x/p\text{-}Ge$ gate stack fabricated after H-Plasma clean with literature.

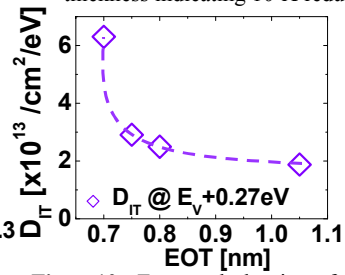

Fig. 10: Extracted density of interface states using equivalent circuit method vs. EOT at midgap

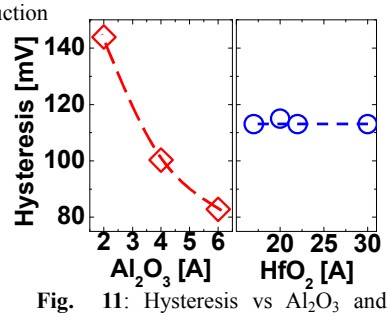

Fig. 11: Hysteresis vs Al_2O_3 and HfO_2 thickness with H-Plasma clean and Oxygen plasma oxidation indicating strong dependence on Al_2O_3 cap layer

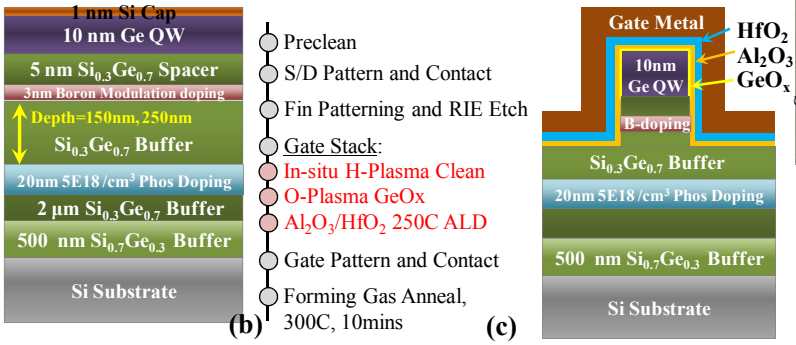

Fig. 12: (a) Schematic of 1.3% s-Ge QW heterostructure with Boron modulation doped SiGe buffer in addition to Phos doping to reduce parallel conduction in the buffer, (b) fabrication process flow for s-Ge QW MOSFET and FinFET with varying fin width, (c) schematic of s-Ge QW FinFET with in-situ H-Plasma clean, oxygen plasma GeO_x formation prior to high-κ deposition.

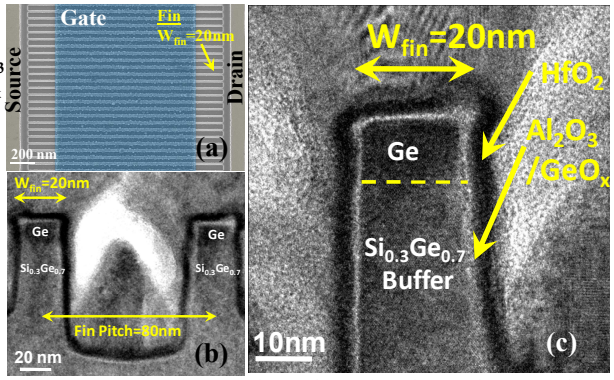

Fig. 13: (a) SEM showing long channel multi-fin device with W_{Fin}=20nm and fin pitch of 60nm, (b) cross section TEM showing s-Ge QW FinFET with 60nm fin pitch(c) HR-TEM showing vertical fin profile for 20nm W_{Fin} device

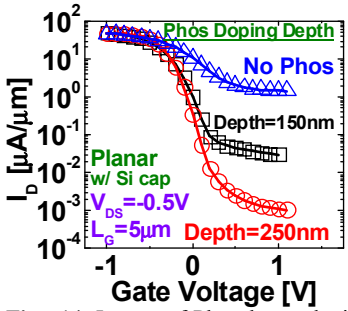

Fig. 14: Impact of Phosphorus doping depth in SiGe buffer on Id-Vg characteristics of s-Ge QW MOSFETs showing reducing I_{OFF} with increasing Phos doping depth.

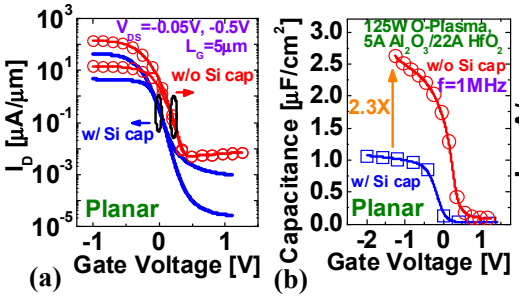

Fig. 15: (a) I_d-V_g characteristic showing impact of Si cap removal prior to high-κ deposition indicating 2X increase in I_{ON} (b) Split CV measured at 1MHz on planar QW MOSFET showing 2.3X higher C_{max} with Si cap removal and GeO_x passivation.

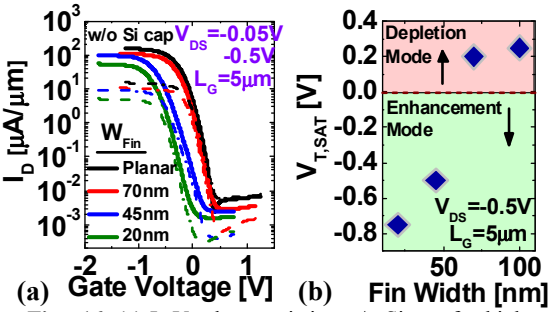

Fig. 16: (a) I_d-V_g characteristics w/o Si cap for high-κ/s-Ge QW MOSFET and FinFET at V_{DS}=-0.05V, -0.5V showing high I_{ON} and excellent I_{ON}/I_{OFF}=2x10^4, (b) $V_{T,SAT}$ vs W_{Fin} indicating enhancement mode operation due to confinement for QW FinFETs. A conservative W_{Eff}=No. of fins *(W_{Fin}+2T_{QW}) was used

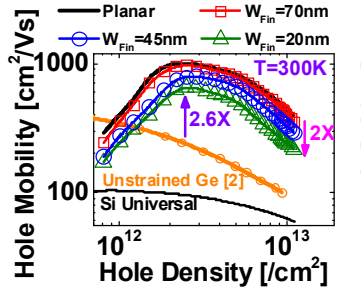

Fig. 17: Effective hole mobility of s-Ge QW MOSFET and FinFET with HfO_2/Al_2O_3/GeOx gate stack showing 2.6X improvement compared to unstrained Ge

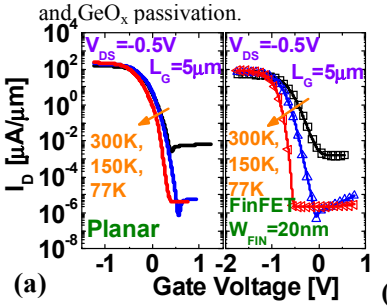

Fig. 18: (a) Id-Vg characteristics at V_{DS}=-0.5V, L_G=5um for high-κ/Ge QW MOSFET and FinFET with reducing temperature, (b) Subthreshold swing vs. temperature for planar MOSFET and FinFET

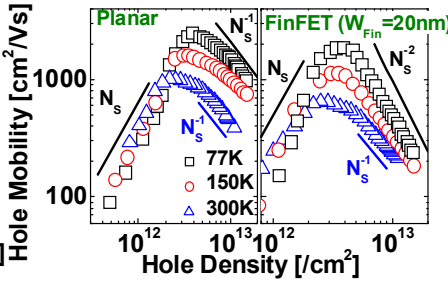

Fig. 19: Temperature dependent hole effective mobility vs hole sheet density for planar QW MOSFET and FinFET indicating Ns dependence.

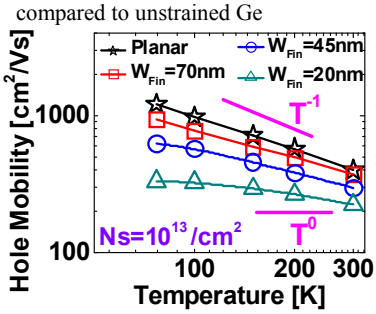

Fig. 20: Hole effective mobility vs. temperature for high-κ/s-Ge QW MOSFET and FinFET at Ns=10^{13} /cm^2.

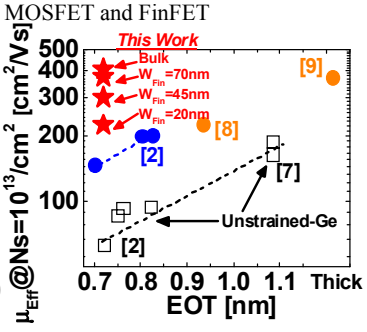

Fig. 21: High field mobility of high-κ/s-Ge QW MOSFET and FinFET in this work vs. EOT, compared with s-Ge pMOSFETs w/o Si cap to date

	W_{fin} (nm)	μ_{Peak} (cm^2/Vs)	ε_{XX} (%)	EOT (nm)	μ_{Peak}*C_{ox} (x10^{-4})
This work	20	700	1.3	0.72	3.1
W. Chern IEDM,2012	18	850	2.5	1.5	1.9
R. Zhang IEDM,2013	800	380	2.5	0.8	1.6
J. Mitard VLSI,2014	15	600	1.3	1.7	1.6

Table I: Benchmarking of key device parameters demonstrated in this work with other high performance s-Ge FinFETs till date.

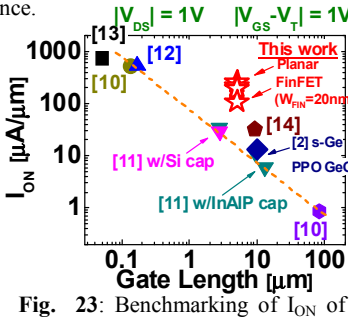

Fig. 23: Benchmarking of I_{ON} of the s-Ge MOSFET and FinFETs with in-situ oxidation achieved in this work with other devices from literature.