Experimental Investigation of Scalability and Transport in $In_{0.7}Ga_{0.3}As$ Multi-Gate Quantum Well FET (MuQFET)

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Compound semiconductors such as $In_{0.7}Ga_{0.3}As$ and InSb are being actively researched as replacement for silicon channel materials for logic applications due to their superior transport properties [1,2]. Planar III-V quantum-well FETs have already demonstrated with superior performance than the state-of-the art Si MOSFETs for low supply voltage (Vcc) applications [1-3]. A key research challenge remains in addressing the scalability of III-V based quantum-well FETs to sub-14 nm node logic applications while still maintaining their excellent transport advantage. In this study, we demonstrate quasi-ballistic operation of non-planar, multi-gate, modulation doped, strained $In_{0.7}Ga_{0.3}As$ quantum well FET (MuQFET), combining the electrostatic robustness of multi-gate configuration with the excellent electron mobility of high mobility quantum well channel, $In_{0.7}Ga_{0.3}As$ (Figure 1).

Device Fabrication: The $In_{0.7}Ga_{0.3}As$ MuQFET devices were fabricated on MBE grown quantum well heterostructure as shown in Figure 1(a). The strained high mobility $In_{0.7}Ga_{0.3}As$ channel is sandwiched between two adjacent high bandgap $In_{0.52}Al_{0.48}As$ layers and is modulation doped by the delta doped layer placed in the bottom barrier and separated from the QW by a 3nm spacer. An assortment of fins with width varying between 40nm and 420nm were patterned using electron beam lithography with nested dummy fins mitigating the electron deflection issues. The source/drain contact was formed using Ni(10nm)/Ge(30nm)/Au(80nm) evaporation and lift-off. A 350 °C annealing in the nitrogen (N_2) ambient for 90s is used to form the alloyed ohmic contact to the quantum-well. A 10nm thick Al_2O_3 high-k dielectric is deposited using Atomic Layer Deposition (ALD) at 300°C. Ti(10nm)/Ni(10nm)/Au(10nm) based wrap-around gates are defined using a electron beam lithography and lift-off process. The fabrication flow is summarized in Table 1, and the titled view SEM image is shown in Figure 2.

Device characterization: The fabricated strained $In_{0.7}Ga_{0.3}As$ MuQFETs were characterized using an HP4156A semiconductor parameter analyzer at room temperature. The typical transfer characteristics for an $In_{0.7}Ga_{0.3}As$ MuQFET with Lg=150nm and W=40nm is shown in Figure 3(a). The Ion/Ioff ratio exceeds 2000, and Ion > 100uA/um at Vd=0.5V. The gate leakage is greatly suppressed due to the use of high-k gate stack instead of a Schottky gate. The output characteristic indicates that the channel is well pinched-off implying high self-gain at very low supply voltage (Figure 3(b)). In Figure 3(c), the transfer characteristics of devices with four different fin widths are compared. It is clear that, with decreasing fin width, the multi-gate configuration markedly improves the gate control over the charge in the channel. Thinner fin width also aids in depleting the channel and induces a positive threshold voltage shift implying the possibility of enhancement mode QWFET in a multi-gate configuration.

Short channel effect: The transfer characteristic of a 60nm Lg $In_{0.7}Ga_{0.3}As$ MuQFET with 40nm fin width is shown in Figure 4(a) where the Ion/Ioff degrades to 300. The sub-threshold slope (SS) and drain induced barrier lowering (DIBL) as a function of gate length are plotted (Figure 4(b)-(c)) for various fin widths ranging from 420 nm to 10 nm. Using three-dimensional numerical simulation, we explore the potential profile in the channel of the fabricated MuQFET. We extract the electrostatic scaling length, Λ, from the electrostatic potential profile which drops off exponentially as a function of the distance into the channel from the source (Figure 5(a)). We also simulated the electrostatic potential profile for two other device configurations including a surface channel $In_{0.53}Ga_{0.47}As$ FINFET [5] and a lattice matched $In_{0.53}Ga_{0.47}As$ multi-gate III-V quantum-well FET [4]. It is evident that our fabricated MuQFETs with EOT of 58nm show superior scalability compared to the planar QWFET for the same EOT, which is consistent with the trend observed in Figure 4(a). If we scale the EOT of the dielectric to 2nm as reported in [4], the electrostatic scaling length is comparable (Table 5(b)). We also compare the SS and DIBL versus normalized gate length (Lg/Λ) for these devices in Figure 5(c). We expect further improvement in the sub-threshold slope of $In_{0.7}Ga_{0.3}As$ MuQFET by proper surface pre-treatment and post-annealing before and after high-k deposition process.

Mobility extraction: 3D numerical simulation (self-consistent Schrodinger-Poisson included) is used to compare the electron density profile in the fin cross-section in MuQFET and classical FINFET (Figure 6(a)). For a given gate overdrive (Vg-Vt), the electron density is highest along the top and sidewall surfaces in FINFETs, whereas the MuQFET shows volume conduction. This suggests that transport in MuQFETs is less affected by surface scattering. Figure 6(a) shows the simulated transfer characteristics of the MuQFETs with and without access resistance. The MuQFET channel mobility is extracted as a function of Lg using the simulated channel carrier density (Figure 6(b)). It is evident that the effective mobility in $In_{0.7}Ga_{0.3}As$ MuQFET is a combination of "ballistic mobility", μ_{ball}, (given by $2qL_g/2\pi mv_{th}$, v_{th} is thermal velocity) and the long channel mobility in the diffusive limit, $\mu_{ballistic}$ [6].

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[2] M. K. Hudait et al, *IEDM Tech. Dig.,* p. 625 (2007)
[3] K. Majumdar et al, *IEEE Trans. on Nanotechnology*, vol. 9, p. 342 (2010)
[4] M. Radosavljevic et al, *IEDM Tech. Dig.,* p. 614 (2010)
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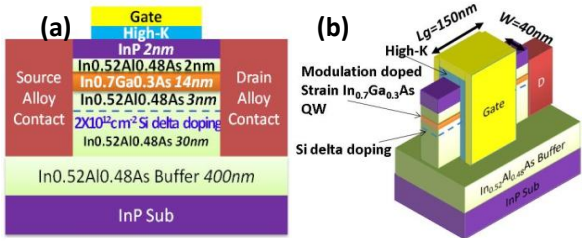


Figure 1. (a) Quantum Well FET layer structure; (b) 3D schematic of high In content $In_{0.7}Ga_{0.3}As$ Multi-Gate Quantum Well FET (MuQFET)

1. Surface Cleaning, Alignment Markers
2. Fins patterning, device isolation using ebeam lithography and BCl_3 dry etch
3. S/D metallization: Ni/Ge/Au
4. Gate dielectric: ALD Al_2O_3 10nm
5. Wrap Gate Stack Ti/Ni/Au definition using ebeam lithography and lift-off
6. Open the S/D contact using Cl_2 dry etch

Table 1. Fabrication flow of $In_{0.7}Ga_{0.3}As$ MuQFET

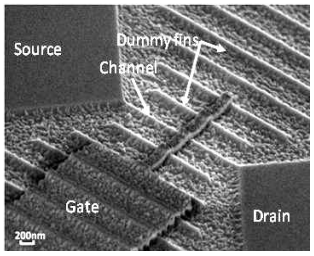


Figure 2. Tilted SEM image of a fabricated $In_{0.7}Ga_{0.3}As$ MuQFET. The nested dummy fins are used to facilitate fin patterning using electron beam lithography

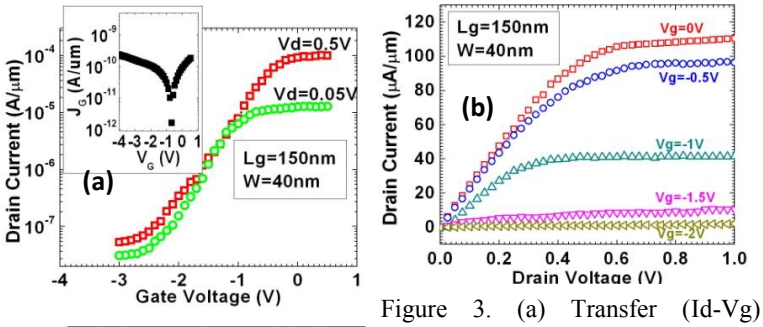


Figure 3. (a) Transfer (Id-Vg) characteristics of $In_{0.7}Ga_{0.3}As$ MuQFET, Lg = 150 nm (Vd=0.05V, 0.5V), shows Ion/Ioff>2000, I_{on}>100uA/um and Ig<$I0^{-9}$uA/um; (b) Output characteristics (Id-Vd) shows low pinch-off voltage; (c) MuQFET transfer characteristics vs. fin width (W=10nm, 40nm, 120nm and 420nm); thinner Wsi improves electrostatics with positive Vt shift.

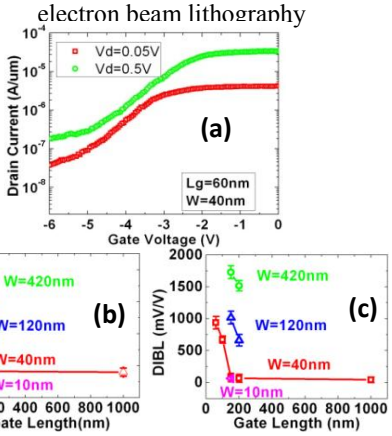
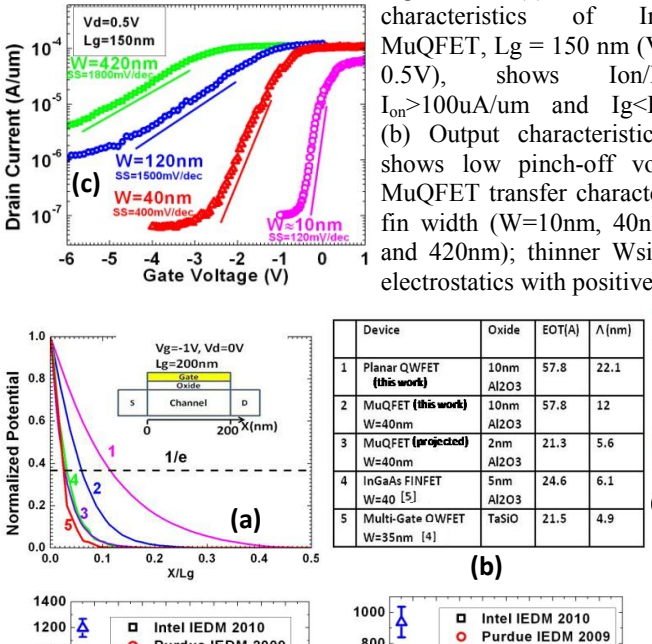
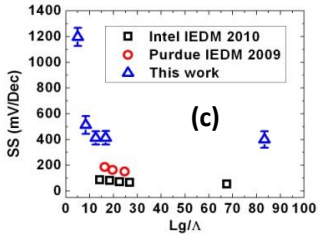


Figure 4. (a) Short Channel MuQFET (Lg = 60nm) characteristic; (b) SS versus Lg for W= 420nm, 120nm, 40nm, 10nm; (c) DIBL versus Lg for W= 420nm, 120nm, 40nm and 10nm



	Device	Oxide	EOT(A)	Λ(nm)
1	Planar QWFET (this work)	10nm Al2O3	57.8	22.1
2	MuQFET (this work) W=40nm	10nm Al2O3	57.8	12
3	MuQFET (projected) W=40nm	2nm Al2O3	21.3	5.6
4	InGaAs FINFET W=40 [5]	5nm Al2O3	24.6	6.1
5	Multi-Gate OWFET W=35nm [4]	TaSiO	21.5	4.9

(b)



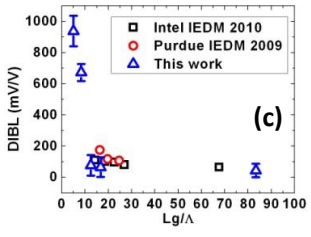
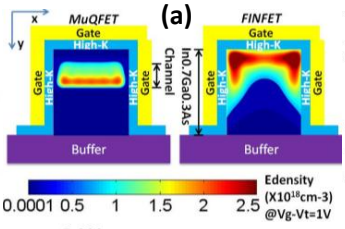
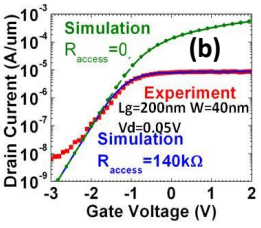
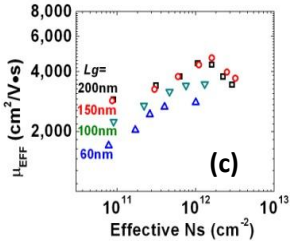


Figure 5. (a) Normalized electrostatic potential for planar, FINFET and MuQFET devices using numerical simulation, The scalng length , Λ, is extracted by fitting V(x)≈V(0)+(Vch-V(0))*(1-exp(-x/Λ)) to the exact potential profile; (b) Summary of scaling length in planar, MuQFET and FINFET devices (c) SS and (d) DIBL versus the normalized gate length, Lg/Λ comparing this work with previous results[4][5].







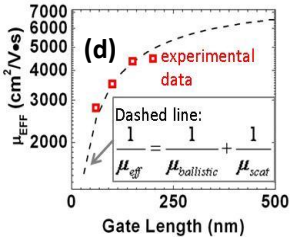


Figure 6. (a) Simulated electron density for MuQFET and FINFET at Vg-Vt=1V employing self consistent Schrodinger-Poisson in x-y plane; (b) Comparison of simulation results with experiment with and w/o access resistance; (c) Carrier density is extracted from simulation to estimate effective mobility at e-density of 10^{12} cm^{-2} vs. Lg (d) Effective mobility is affected by ballistic mobility ($2qL_g/mv_{th}$) [4] indicating quasi-ballistic transport in MuQFET.