Self-aligned Gate NanoPillar $In_{0.53}Ga_{0.47}As$ Vertical Tunnel Transistor

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Introduction: Tunnel field effect transistors (TFET) have gained interest recently owing to their potential in achieving sub-kT/q steep switching slope, thus promising low Vcc operation[1-5]. Steep switching slope has already been demonstrated in Silicon TFET [2]. However, it has been theoretically shown and experimentally proved that Si or Si_xGe_{1-x} based homo-junction or hetero-junction TFETs would not meet the drive current requirement for future low power high performance logic applications [3]. III-V based hetero-junction TFETs have shown promise to provide MOSFET like high drive currents at low operating Vcc while providing the sub-kT/q steep switching slope[1,4,5]. However, the device design demands extremely scaled EOT and ultra-thin body double-gate geometry in order to achieve the desired transistor performance [4]. In this paper, we discuss a vertical TFET fabrication process with self-aligned gate [6] which can ultimately lead to the ultra-thin double-gate device geometry in order to achieve the desired TFET performance.

Nanopillar Tunnel Transistor Fabrication: Fig. 1 shows the cross-section schematics of the fabricated TFET following key process steps. Also shown is a summary of the entire fabrication process flow. $In_{0.53}Ga_{0.47}As$ layers were epitaxially grown on semi-insulating InP substrate using solid state MBE. The top P+ layer is 260nm thick and C doped at $5x10^{19}/cm^3$. This was followed by 100nm thick intrinsic channel and 260nm thick N+ layer, doped at $10^{19}/cm^3$ with Si. 250nm thick Molybdenum(Mo) was blanket deposited on P+ InGaAs using ebeam evaporation. Cr/Ti dry etch masks with minimum width of 250nm were created on Mo using e –beam Lithography, ebeam evaporation and lift-off techniques. Mo and InGaAs were dry etched using Cl_2 and SF_6 based chemistry. Dry etch of InGaAs was carried to a depth of 300nm. To remove sidewall damage and produce undercut, wet etch was performed using H_3PO_4, H_2O_2 and DI water (1:2:40) for 30 secs. An undercut of 55nm was obtained and the net InGaAs MESA height became 380nm. This undercut is important for the formation of self aligned gate. After the wet etch, 5nm Al_2O_3 (high-k) was deposited as gate dielectric using plasma-enhanced atomic layer deposition technique. 20nm Palladium (Pd) gate was vertically deposited using ebeam evaporation. The entire structure was then planarized with BCB and cured at 250°C for 60mins in nitrogen ambient. After curing, BCB was etched back to expose Pd on top of Mo. Pd and Al_2O_3 were then bombarded off using Cl_2 and Ar based dry etch recipe. Lithography was followed to open large contact pads for source, drain and the gate. Ti/Pd/Au probing contacts were then deposited and lifted off.

Device Characterization and Modeling: Figures 2 (a) and (b) show the transmission electron microscopy (TEM) image of a 250nm drawn mesa width fabricated TFET device. Figure 3 shows the two terminal PIN current densities plotted for different MESA widths. Clearly, the Zener (reverse) side of the characteristics overlap on top of each other confirming the success in achieving the isolation between the top source and the side wall gate (self aligned). This also indicates that the PIN leakage floor in the transfer characteristics can be scaled by scaling the mesa width with this planarization approach. Figure 4(a) shows the simulated [7] transfer characteristics for different mesa width devices. Nearly 2 orders of improvement in Ion/Ioff is expected by scaling the mesa area from 20x20 μm^2 to 0.25x5μm^2. Improvement in switching slope (Figure 4(b)) is also expected with MESA scaling due to reduction in leakage floor. Figure 4(c) shows the expected output characteristics for the 250nm width mesa device with an EOT of 2.25nm. The short channel effects observed in the simulation can be reduced in future by scaling the EOT. Figure 5(a) shows the measured Id-Vg characteristics for different mesa width TFET devices. Clearly, the reduction in the leakage floor is observed experimentally due to mesa scaling. Figure 5(b) shows the variation in the switching slope with the mesa width. With mesa scaling, leakage floor reduces and the steeper part of the SS is revealed. Present devices exhibit >kT/q switching slope because of trap assisted tunneling [8]. Better oxide-semiconductor interface and switching slope can be demonstrated in the future and is independent of the current process flow. In order to achieve SS smaller than 60mV/dec slope, not only the leakage floor needs to be reduced, the Tsi needs to be reduced below 20nm [4]. The current process flow has the capability to achieve the desired Tsi width, which will require an optimization of different layer thicknesses and MESA undercut. Figure 5(c) shows output characteristics for the smallest mesa device and shows existence of short channel effects as expected from the simulations. Figure 5(d) shows increasing peak-to-valley ratio with reducing mesa dimensions in the NDR part of the output characteristics. If TFET is expected to operate as a memory element using NDR, reduced mesa dimension and increasing gate control are desired.

[1] S. Mookerjea et al., *IEEE IEDM Tech. Dig.,* Dec. 2009 .
[2]R. Gandhi et al., accepted *IEEE Electron Device. Lett.* (2011)
[3] S. Koester et al., ECS Trans., vol. 33, no. 6, October 2010.
[4]Y. Liu et al., *68th Device Research Conf. Dig*., 2010, p. 17.
[5] H. Zhao et al., *IEEE Electron Device Lett*. 31 (2010) 1392.
[6] H. Saito et al., *Applied Phys. Exp*. 3 (2010) 084101.
[7] Sentaurus Users Guide, Ver. C-2009.06 .
[8] S. Mookerjea et al., *IEEE Electron Device Lett*. 31 (2010) 564.

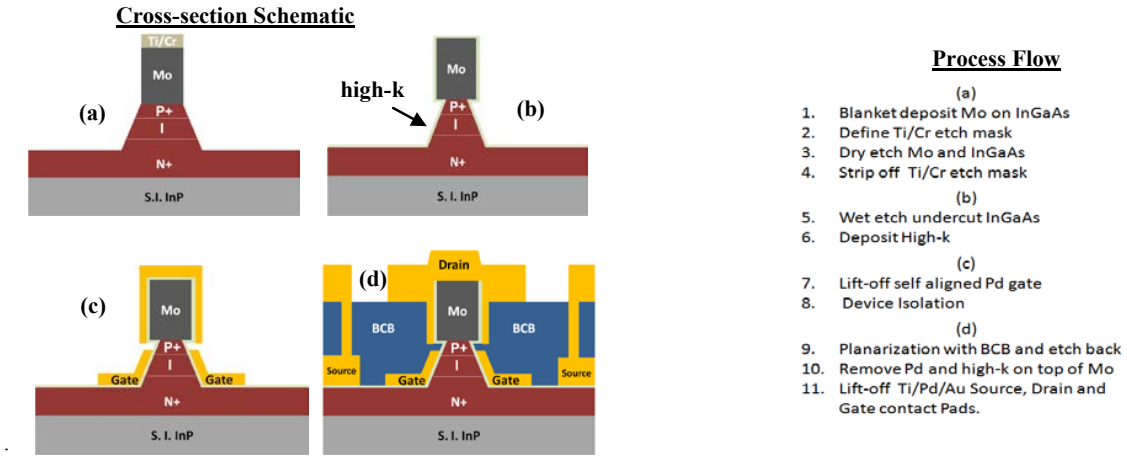

Fig. 1 Cross section schematics of the device follwoing key process steps. Fabrication process flow is shown to the right.

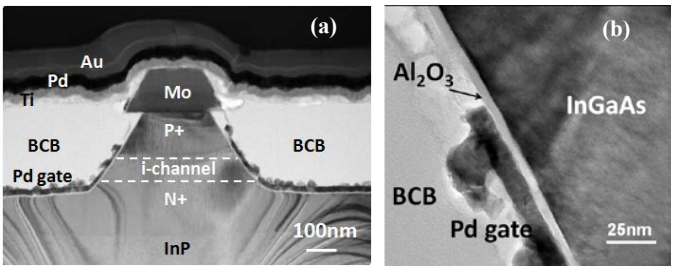

Fig. 2 (a) Cross-section Transmission Electron Microscopy image of the fabricated device structure. (b) Zoomed in image of the left sidewalll showing 20nm self-aligned Pd gate on Al_2O_3 gate dielectric.

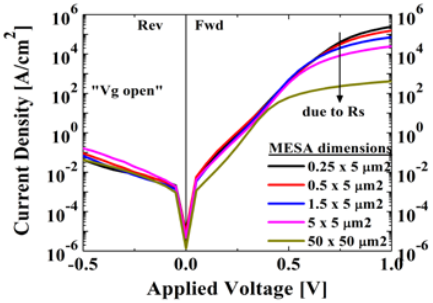

Fig. 3 Two terminal PIN current densities for different MESA area devices. Zener (Rev) BTBT current density scales with MESA area and implies isolation of gate pad from the top source contact

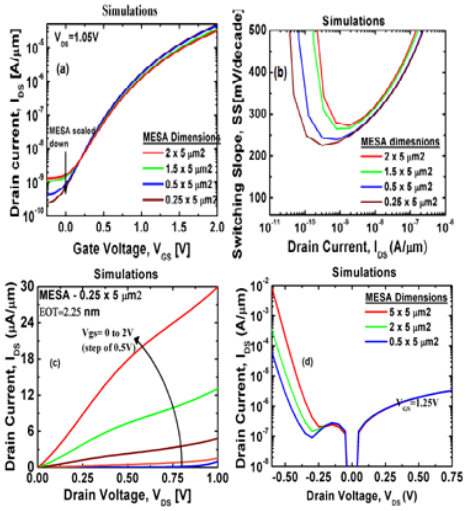

Fig. 4 (a) Simulated Id-Vg curves showing improved on-off ratio due to MESA scaling. (b) Point switching slope improves with MESA scaling (c) Simulated Id-Vd curves for 0.25 x 5 µm^2 MESA (d) NDR characteristics show increasing peak to valley ratio with MESA scaling.

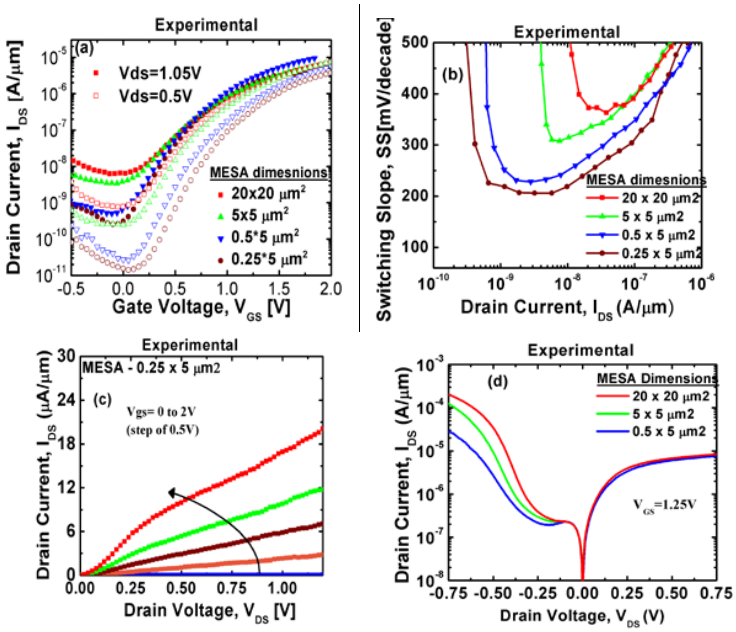

Fig. 5 (a) Measured Id-Vg curves showing improved on-off ratio with MESA scaling. (b) Point switching slope improves with MESA scaling due to reduction in leakage floor. (c) Measured Id-Vd characteristics for the smallest MESA (d) Higher peak to valley ratio in NDR characteristics with MESA scaling indicates reduced thermionic/recombination currents for a given gated current.