Interface States at high-  $\kappa$  /InGaAs interface: H<sub>2</sub>O vs. O<sub>3</sub> based ALD Dielectric

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## 1. Introduction

Interface states at the high-k/III-V interface are considered to be one of the major showstoppers for the implementation of III-V channel MOSFETs in VLSI technology. Due to the large interfacial state density, D<sub>it</sub>, comparable with density of states of free carriers the standard, high-low freq., Terman, and conductance methods become unreliable. Recently, [1,2] proposed obtaining the parameters of the equivalent admittance circuit (including substrate capacitance, Dit, trap time constant, channel resistance and gate leakage) by fitting the experimental frequency dispersion of the capacitance and conductance curves in a self consistent manner.

In this study, we identify the D<sub>it</sub> distribution and the traps characteristic time constant vs. the trap energy by combining the above mentioned method [1,2] with the low-high frequency [3] and Terman techniques [4]. We apply the technique to study the defects in the water (H20) based ALD Al2O3/ In0.53Ga0.47As and in the ozone (O<sub>3</sub>) based ALD  $Al_2O_3/In_{0.53}Ga_{0.47}As$  stacks. H<sub>2</sub>O-based ALD allows reduction in the formation of the native oxide at the high-ĸ/IIIV interface, while O<sub>3</sub>based oxide is known to contain less OH groups within the high-k resulting in less bulk trapping of carriers. Comparing the extracted trap capture cross-section dependences vs. temperature and trap energy, we conclude that: (i) water-based ALD allows reducing the number of electrically active traps (ii) the traps in the water-based ALD high- $\kappa$  film respond (recharge) by more than an order of magnitude slower that those in O<sub>3</sub>-based high-κ film.

## 2. Device Fabrication

N and P doped In<sub>0.53</sub>Ga<sub>0.47</sub>As was epitaxially grown on a InP substrate. After the ammonia based surface clean the Al<sub>2</sub>O<sub>3</sub> films were deposited on In<sub>0.53</sub>Ga<sub>0.47</sub>As using either a H<sub>2</sub>O-based or O<sub>3</sub>-based atomic layer deposition (ALD) followed by post anneal. The TaN/TiN metal was deposited and patterned as top electrode. The AuGe alloy was deposited to form a backside ohmic contact.

## 3. Results

*D<sub>it</sub> extraction:* The admittance characteristics of the fabricated capacitors were measured for 200K to 425K temperature range. Fig. 1 and 2 show the measured capacitance at RT for the H<sub>2</sub>O and O<sub>3</sub>-based ALD high-ĸ. Fig. 3 shows the calculated ideal C-V dependency for the 8nm Al<sub>2</sub>O<sub>3</sub> high-κ/ In<sub>0.53</sub>Ga<sub>0.47</sub>As stack [5] taking into account the conduction band nonparabolicity and carrier distribution in  $\Gamma$ , L and X valleys. We have used low temperature and high temperature C-V data sets in order to accurately evaluate the effects of interface and border traps. At 425 K the traps are fast enough ( $2\pi f \tau >> 1$ , see Fig. 5(b)) for the 1kHz C-V to be considered as a true low frequency C-V. In this case the trap response is quasistatic and the trap capacitance, Cit=qDit. The high temperature low frequency C-V and the "stretch-out" of the low temperature high frequency C-V characteristic (a "true" high frequency C-V) were theoretically reproduced. Fig. 4 shows the result of this iterative fitting exercise for both H2O-based and O3based ALD high-κ. The C-V with non-parabolic (NP) correction including all valleys was used for this exercise. The simulated C-V with Cit represents the quasi-static case and C-V without Cit represents the high frequency case (includes the stretch-out in gate bias due to D<sub>it</sub>). The evaluated D<sub>it</sub> from p and n type samples are in good agreement (Fig. 5(a)). The trap density for the  $O_3$ -based ALD is ~1.5 times higher than that of H<sub>2</sub>O-based ALD sample.

Interfacial layer analysis: An XPS study on these samples shows the presence of the As-O bonds in the O<sub>3</sub>-based ALD sample. The use of O<sub>3</sub> as oxidant for the ALD growth of Al<sub>2</sub>O<sub>3</sub> on In<sub>0.53</sub>Ga<sub>0.47</sub>As has resulted in excessive interfacial oxidation consistent with [6]. Due to the presence of a native oxide at the oxide-substrate interface the measured oxide capacitance for the  $O_3$ -based ALD is ~ 10% lower than that of the H<sub>2</sub>O-based sample.

Trapping kinetics: The characteristic traps capture times (for the mid gap traps) obtained from the conductance peaks (Fig. 5(b)) shows an order of magnitude faster response time for the O<sub>3</sub>-based ALD high-ĸ. The extracted capture cross-section of the mid gap traps in both samples were found to be weakly depend on temperature (Fig. 5(b)) and for the O<sub>3</sub>-based sample to be  $\sim 1$  orders of magnitude larger than that for the H<sub>2</sub>O-based sample. It is opposite to the expected trend if the electrons were to tunnel through the native oxide in the O<sub>3</sub>-based sample before they can get trapped by the high-k defects, leading to a decrease in the capture cross-section. This observation indicates that the traps may have a significantly different atomic structure, and chemical bonds. It is worth noting that the energy dependence of the capture time is rather weak in both samples (Fig. 6(a) and 6(b)). Fig. 7 shows the comparison of the mid-gap  $D_{it}$ compared with other works reported in literature.

## 4. Conclusion

By combining the capacitance and conductance analysis techniques, we obtained the D<sub>it</sub> distribution throughout the band gap of In<sub>0.53</sub>Ga<sub>0.47</sub>As capacitors with H<sub>2</sub>O-based and O<sub>3</sub>-based ALD oxides. The choice of appropriate temperature to obtain the quasi-static C-V and the DC voltage sweep rate is an essential for the correct extraction of D<sub>it</sub>. Simultaneously we obtained the trap kinetics characteristics. We claim that: (i) the H<sub>2</sub>O-based ALD deposition results in a fewer traps in the lower portion of In<sub>0.53</sub>Ga<sub>0.47</sub>As band gap, (ii) is

related to the formation of the thicker native oxide in the O<sub>3</sub>-based samples; (iii) the mid gap traps in the H<sub>2</sub>O-based samples are significantly slower than those in the O<sub>3</sub>-based samples, which indicate their different nature.

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(a) H<sub>2</sub>O Oxidation 0.8 0.8 0.6 0.6 C 0.4 X 1KHz-1MHz 0.2 0.0∟ \_2 300K 」0.0 2 -1 0 Gate Voltage [V] (b) H<sub>2</sub>O Oxidation 0.8 0.8 0.7 1KHz-1MHz 0.6 C/C 0.4 X 0.2 300K \_\_0.0 2 0.0 0 -1 1 Gate Voltage [V]



O, Oxidation

(a)

0.8

Fig.1: C-V characteristics as a function of Fig.2: C-V characteristics as a function of frequency of (a) ntype and (b) ptype frequency of (a) ntype and (b) ptype In<sub>0.53</sub>Ga<sub>0.47</sub>As Moscap with H<sub>2</sub>O based ALD In<sub>0.53</sub>Ga<sub>0.47</sub>As Moscap with O<sub>3</sub> based ALD AI203.







Fig.5: Extracted (a) interface trap density and (b) interface trap time constant and capture cross section at  $E_F \sim Eg/2$  for the water and ozone based ALD Al<sub>2</sub>O<sub>3</sub>.

Temperature [K]

350

300

250

Fig.6: Trap time constant as a function of energy and temperature for (a)  $H_2O$  and (b)  $O_3$  based ALD  $AI_2O_3$ .



Fig.3: Simulated capacitance showing the effect of non parabolic approximation and satellite valley for In<sub>0.53</sub>Ga<sub>0.47</sub>As with 8nm  $AI_2O_3$  high- $\kappa$  ( $\varepsilon r \sim 8$ ) as a function of gate bias.



Fig.4: Measured true Low and High frequency fitted with calculated C-V with D<sub>it</sub> for ntype  $In_{0.53}Ga_{0.47}As$  Moscap with (a)  $H_2O$  and (b)  $O_3$ based ALD Al<sub>2</sub>O<sub>3</sub>.



Fig.7: Midgap D<sub>it</sub> evaluated by conductance method at room temperature compared with other work reported in literature.