Critical Discussion on (100) and (110) orientation dependent transport: nMOS Planar and FinFET

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Abstract

Electron mobility on (100) and (110) planar FETs and SOI FinFETs was evaluated. It is experimentally demonstrated that the (110) sidewall of FinFETs does not present a drawback in terms of electron mobility – contrary to results obtained on (110) planar MOSFETs. This is comprehensively explained by a combination of first principles and empirical approach closely matching the experimental data.

Introduction

FinFETs, owing to improved electrostatics, appear imperative for future scaling. However, the crystal orientation of the fin sidewalls [i.e., (110)<110> or (100)<100>] can have an impact on mobility [1,2]. Bulk planar CMOS has demonstrated orientation dependent mobility [3-5]: 1) hole (h^+) mobility (μ_{eff}) increases significantly for Si(100)<100> compared to Si(110)<110>; 2) the electron (e^-) mobility is severely degraded with the same orientation change (Fig. 1). In this work, we demonstrate CMOS FinFETs in which the e^- μ_{eff} on a (110)<110> sidewall orientation performs comparably to e^- μ_{eff} on (100)<100>. This is attributed to a combination of effective mass and intervalley scattering (first principles when considering non-parabolicity) and low operating electric field in FinFETs resulting in Phonon Scattering limited transport in FinFETs (empirical).

Experimental

Gate first, bulk-Si Planar MOSFETs [3] and SOI FinFETs [6] (Figs. 2,3) with the same Hafnium-based high-κ and TiN metal gate (HK/MG) were processed with channels formed on (100) and (110) surfaces. Split capacitance – voltage (C-V) and various current – voltage (e.g., I_d-V_g and I_d-V_d) measurements (20K – 300K) were conducted with subsequent μ_{eff} extraction, modeling, and simulation.

Results and Discussion

Fig. 4 shows the sidewall mobility characteristics on p- and n-channel FinFETs with different orientations but same wafer (Fig. 2). Compared to the results on Fig. 1, the astonishing feature in FinFETs is that the (100) and (110) electron mobility values are significantly closer to each other. This suggests that the FinFET conventional sidewall plane, which is (110), does not present a drawback regarding the electron mobility while the (110) holes enjoy the high mobility relative to (100) (Fig. 4). A similar mobility trend is seen for SiO_2/poly gate n and pMOS FinFET μ_{eff} on both orientations (Fig. 4b) when compared to HK/MG – indicating that this observation is not due to possible stress caused by highk/metal gate process [7]. The I-V and C-V data used for different FinFET orientations and carrier types [Fig. 5] confirm similar CET, and hence, similarity of electron mobility on different sidewall crystalline orientations. To understand these (100) and (110) differences, a preliminary investigation is done using two paths: 1) 'first principles' approach, and 2) an empirical/Universal Mobility [8] approach.

First Principles – Under the relaxation time approximation, the close match between the e^- mobility vs. inversion carrier density and temperature in (100) and (110) FinFETs implies that the average e^- transport effective mass and phonon scattering rates are comparable. To understand the governing physics for comparable electron transport in (100) and (110) sidewall FinFETs, we employed a nearest neighbor $sp^3d^5s^*$ tight-binding formalism with spin-orbit coupling to simulate the fin band structure[9,10]. Electrostatic confinement induced valley splitting is estimated by triangular well approximation. Shown in Fig.5, the non-parabolicity (NP) of transverse e^- mass in <110> is evident [11,12]. This NP is translated into a considerable deviation from the parabolic confinement mass ($m^{*\Delta2}_{conf}$=0.19m_0) of light Δ_2 valley in (110). As seen in Fig.6, $m^{*\Delta2}_{conf}$ increases with increasing quantization energy (i.e., N_{inv}) and becomes heavier than $m^{*\Delta4}_{conf}$ at 79meV from unconfined band minimum leading to a lower Δ_2 valley energy than Δ_4. Figs.7 and 8 show the valley split energy, occupancy and average conductivity effective mass for (110) and (100) devices. The monotonic increase in split energy for (100) results in suppression of f-type intervalley optical phonon (IOP) scattering, and asymptotical reduction of conductivity effective mass to 0.19m_0. For (110) devices with parabolic m^*_{conf}, heavy Δ_4 valley is primarily occupied while the split energy is less than optical phonon energy, which implies heavy e^- mass and significant IOP scattering. On the other hand, nonparabolic (110) approach showed lower Δ_2 valley energy with increasing N_{inv}, almost "lagging" the (100) band structure and conductivity effective mass. Fig.9 shows the (100) and NP (110) band structure and e^- distribution at N_{inv}=10^{13}/cm^2. Clearly in both devices, e^- occupy mostly the light valley with 0.19m_0 and the valley split energy is either comparable or larger than silicon OP energy at T=300K. Thus, the e^- transport in (110)<110> and (100)<100> sidewall fins are expected to show similar dependence on N_{inv}, due to the similar reduction in mass and intervalley phonon scattering rates.

Empirical – Quantization difference is being compared between planar and FinFET in Fig. 10. It is evident that for the same sheet carrier concentration, double gate devices operate at much lower E_{eff} (~1/10-1/3) than planar devices. This has important repercussions on μ_{eff} enhancement for weak, structurally quantized finFET. Ground subband wavefunctions at N_{inv}=10^{13} /cm^2 shown in Fig. 11 indicate the weaker quantization for Si(110) oriented devices for planar and Double Gate(DG). For mobility modeling, the scattering mechanisms accounted for are: Coulomb scattering (CS), Phonon Scattering and Surface Roughness (SR) Scattering. Relaxation time approximation has been used to model phonon scattering for planar and DG devices. IOP was not found significant from the μeff - T analysis and hence was not taken into account. An empirical formulation of CS and SR scattering has been employed [12]. An important observation is that calculated phonon scattering-limited mobility (Fig.12(a)) degrades only very slightly for (110) as compared to (100). This can be understood by the lower form factor for (110) oriented substrate (Fig. 12(b)), due to lower confinement, which compensates for the high DOS and high transport effective mass. Fig. 13(planar) shows experimental and modeled mobility for e^- in Si(100) and Si(110) planar devices with integrated high-k/Metal Gate. The mobility for (110) is degraded by 55% at N_{inv}=10^{13} /cm^2 as compared to (100). This can be explained by the high density of states which increase the scattering rate, as well as heavier transport effective mass as a result of transformed E-k compared to Si(100). Consequently, the SR scattering rate increases resulting in overall decrease of e^- mobility at low and high field for Si(110). Fig. 14(planar) shows the experimental and modeled μ_{eff} as a function of temperature for planar devices, thereby confirming the assertion about dominant scattering mechanisms in both orientations. On the other hand, there is very insignificant degradation observed for Si(110) than (100) on finFETs (Fig. 13(DG)), attributed to lower SR scattering due to low E_{eff}, and lower CS due to low channel doping. μ_{eff} is mainly limited by phonon scattering at low and high field. Fig. 14(DG) depicts the experimental and modeled μ_{eff} vs T for finFETs showing identical temperature behavior for both orientations. It is proved that phonon scattering plays a dominant role for both orientations in finFETs devices near room temperature.

Our results on FinFET mobility are well correlated with the current drive. The FinFETs with the conventional (110) sidewalls display a very balanced current drive (Fig. 15) since PFET mobility is boosted relative to (100) while the NFET mobility has remained almost the same.

Summary

Electron mobility for FinFETs and planar MOSFETs are compared. It is experimentally demonstrated that the conventional (110) sidewall of FinFETs does not present a drawback in terms of electron mobility. This observation contradicts with the results obtained on (110) planar MOSFETs, where a reduction in mobility relative to (100) had been systematically observed. Increased surface roughness scattering results in degraded performance in planar (110) confirmed by μ_{eff} -T analysis. FinFETs are immune to this phenomenon because of low field operation and low doping, and hence are only limited by phonon scattering which is similar, due to reduced (110) form factor.

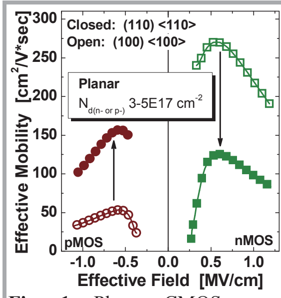


Fig. 1. Planar CMOS μ_{eff}. pMOS improves for (110), but nMOS degrades for (110) [3,4].

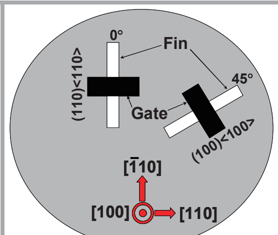


Fig. 2. FinFET devices: 0° (110) or 45° (100) used in inversion split C-V (Q_{inv} extraction) and differential I_d-V_g @ V_d=20 and 40 mV on L_g = 10 μm.

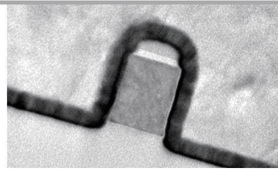
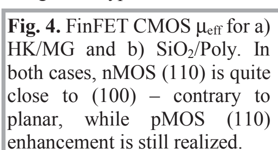


Fig. 3. Cross sectional TEM image: the typical finFET used.



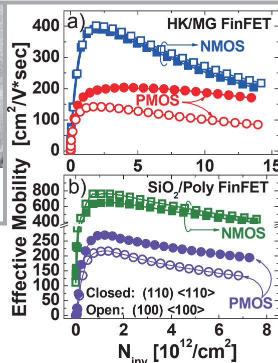


Fig. 4. FinFET CMOS μ_{eff} for a) HK/MG and b) SiO₂/Poly. In both cases, nMOS (110) is quite close to (100) – contrary to planar, while pMOS (110) enhancement is still realized.

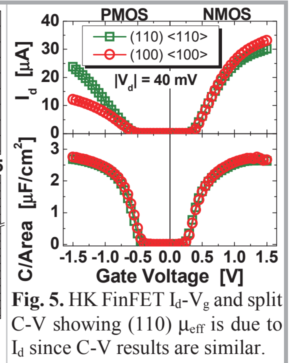


Fig. 5. HK FinFET I_d-V_g and split C-V showing (110) μ_{eff} is due to I_d since C-V results are similar.

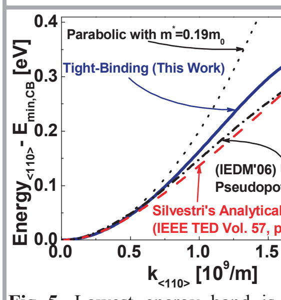


Fig 5. Lowest energy band is shown along the <110> direction of transverse electron mass. Deviation from parabolic dispersion changes quantization mass of the Δ2 valley in (110).

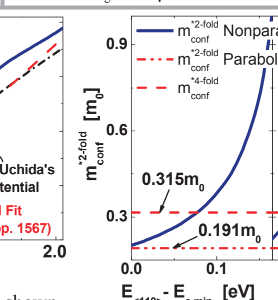


Fig 6. The nonparabolic m_t vs. quantization energy along <110>. Δ_2 quantization mass quickly becomes heavier than that of Δ_4 valley, resulting in Δ_2 being the ground valley with increasing electrostatic confinement.

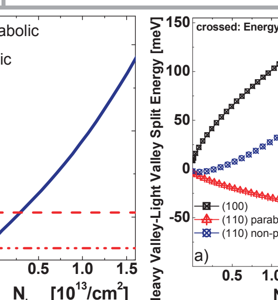


Fig 7. The valley split energies and occupancies for (100) and (110) devices with nonparabolic confinement mass switches light and heavy valleys such that (110) shows a "lagging" behavior of (100).

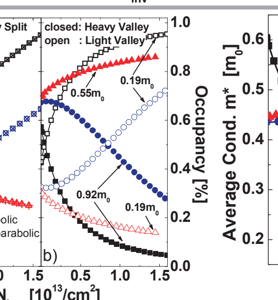


Fig 8. The average conductivity effective mass vs. N_{inv} is shown for (100) along with parabolic and nonparabolic approaches for (110) devices. Unlike the parabolic (110) case, nonparabolic (110) follows (100) mass with increasing N_{inv}.

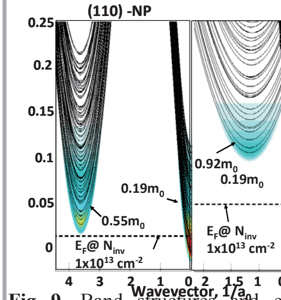


Fig 9. Band structures and electron distribution for NP (110) and (100) at N_{inv}=10¹³/cm². (110) band structure has similar characteristics as (100), leading to comparable μ_n.

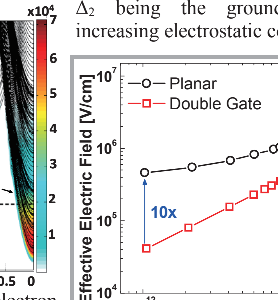


Fig. 10. Calculated E_{eff} vs N_{inv} showing lower field operation for finFET than for planar.

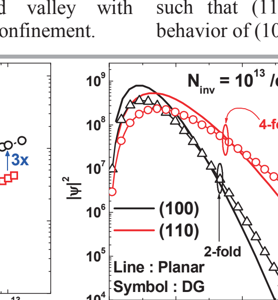


Fig. 11. Ground subband wavefunctions for planar and finFET (DG).

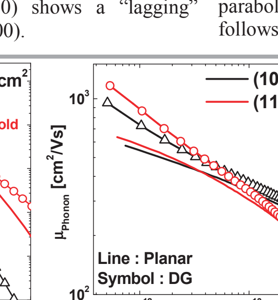


Fig. 12. a) Calculated Phonon-limited mobility for (100) and (110) for planar and DG; **b)** Form factor (ff) vs N_{inv} showing lower ff for Si(110) than (100), compensating for m* ↑ in (110).

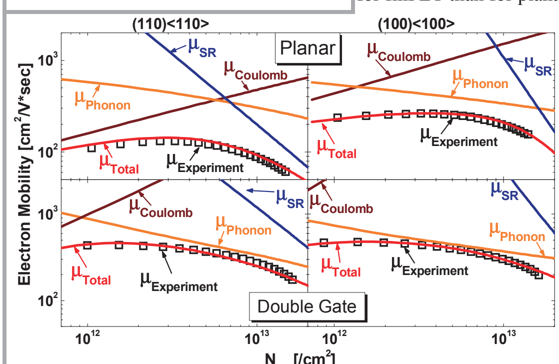


Fig. 13. Experimental and modeled μ_{eff} vs. N_{inv} for nMOS planar and FinFET (100) and (110). Planar (100) mobility is largely limited by phonon scattering, whereas (110) mobility is limited by CS at low N_{inv}, and SR scattering at high N_{inv}. For FinFETs, mobility for both orientations is mainly limited by phonon scattering.

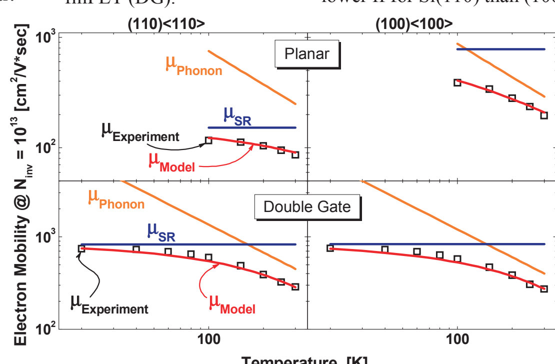


Fig. 14. Mobility as a function of temperature for Planar and DG nMOS (100) and (110) indicating dominant scattering mechanisms where planar (100) is limited by phonon scattering and (110) is limited by SR scattering at 300K. For FinFETs, phonon scattering largely limits the mobility for (100) and (110) oriented devices for low and high N_{inv}.

Fig. 15. CMOS I_d-V_d curves for FinFETs orientated on (110) sidewall surfaces illustrating symmetric behavior of (110) n and pMOS – negating the need for hybrid orientation technology.

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