ECS Transactions, 35 (3) 311-317 (2011)
10.1149/1.3569923 ©The Electrochemical Society

Multi-Gate Modulation Doped $In_{0.7}Ga_{0.3}As$ Quantum Well FET for Ultra Low Power Digital Logic

L. Liu [a], V. Saripalli [b], E. Hwang [a], V. Narayanan [b] and S. Datta [a]

a Department of Electrical Engineering, Penn State University, University Park, PA 16802, USA
b Department of Computer Science and Engineering, Penn State University, University Park, PA 16802, USA

Multi-gate modulation doped $In_{0.7}Ga_{0.3}As$ quantum well FETs (MuQFETs) are simulated, fabricated and analyzed in detail. The devices operate in both classical and non-classical quantum regime. Due to its robust electrostatics, its excellent channel transport properties and its versatile classical and quantum mode operation capability, $In_{0.7}Ga_{0.3}As$ MuQFET is promising device architecture for future ultra low power information processing applications.

Introduction

Compound semiconductor materials (III-V) such as indium gallium arsenide ($In_{0.70}Ga_{0.30}As$) (1), InAs (2) and InSb (3) due their superior carrier transport properties, are being actively researched as replacement for Silicon (Si) channel materials for digital logic applications. Planar quantum–well FETs (QWFETs) in III-V material system have already demonstrated superior performance than the state-of-the-art planar Si MOSFETs particularly for low supply voltage (Vcc) logic applications. A key research challenge remains in addressing the scalability of III-V based quantum-well FETs to sub-14 nm node logic applications while still maintaining their superior transport advantage over their Si counterpart. In this study we propose and experimentally demonstrate a novel non-planar, multi-gate, modulation doped, strained $In_{0.7}Ga_{0.3}As$ quantum well FET (MuQFET), combining the advantages of multi-gate configuration and high mobility quantum well channel. Further, we experimentally demonstrate the enhancement mode (normally off) operation of the modulation doped $In_{0.7}Ga_{0.3}As$ MuQFET (necessary for direct coupled FET logic applications) through aggressive scaling of the fin thickness. By performing three dimensional numerical simulations we elucidate the important differences between the MUQFET device architecture investigated here and a surface channel III-V FINFET (4), with former being more suitable for low power, high performance digital logic applications. In addition, the quantum well layer structure and the ultra-thin fin geometry, confine the electrons in a one-dimensional (1D) quantum wire configuration. With a pair of split wrapped gates configuration with a proper bias in the depletion mode, the electrons can be confined in a quantum dot (0D). As we scale the size of the quantum dots by reducing the distance between the pair of split gates, it is likely that the quantum dot accommodates only a few electrons. Therefore, we expect the ultra scaled devices to operate in the Coulomb blockade (CB) regime as single electron transistors for reconfigurable and ultra-low-power binary decision diagram (BDD) logic

applications (5). We provide preliminary experimental results of drain current oscillations, indicative of potential CB operation, observed in the fabricated split gate InGaAs MuQFET devices.

Modulation Doped $In_{0.7}Ga_{0.3}As$ MuQFET Device Simulation

Figure 1 shows the schematic of a planar pseudomorphic $In_{0.70}Ga_{0.30}As$ quantum-well FET, a lattice matched $In_{0.53}Ga_{0.47}As$ FINFET and a non-planar modulation doped pseudomorphic $In_{0.70}Ga_{0.30}As$ MuQFET devices. The pesudomorphic structure with higher indium content (70%) shows much higher electron mobility than its corresponding

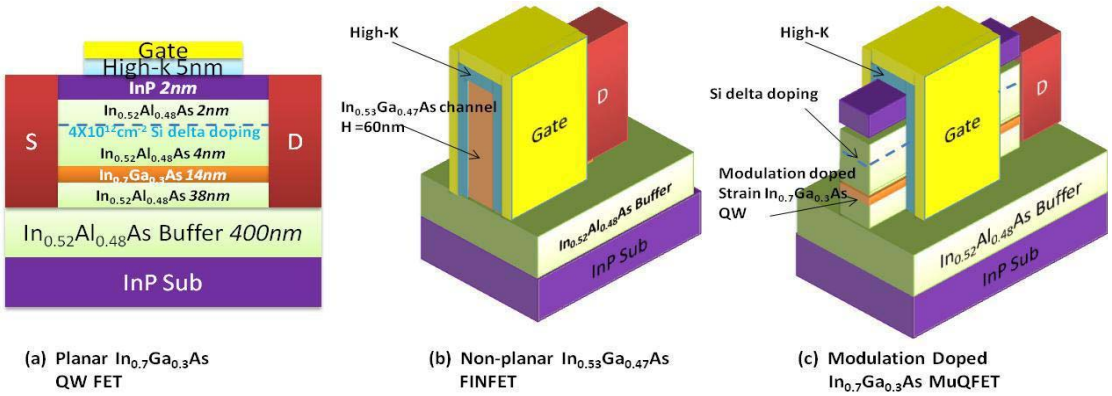

Figure 1 Various III-V transistor architectures

lattice matched composition with indium content of 53%. Recently, Radosavljevic *et al* (6) demonstrated a non-planar multigate $In_{0.53}Ga_{0.47}As$ quantum-well FET device suitable for low power logic applications. The objective of this work is to demonstrate and analyze a non-planar multi-gate device architecture incorporating a modulation doped pseudomorphic $In_{0.70}Ga_{0.30}As$ quantum-well with higher indium content, as shown in Figure 1(c). To understand the important differences between the $In_{0.53}Ga_{0.47}As$ FINFET (Fig. 1b) and the $In_{0.70}Ga_{0.30}As$ MuQFET in terms of electrostatics, carrier confinement, short channel effects and transport properties, we perform three-dimensional (3D) numerical simulations using the Sentaurus device simulator (7).

Figure 2(a) shows the simulated transfer characteristics of the planar QWFET, FINFET and MuQFET devices. The planar QWFET shows depletion mode operation (i.e. normally on at zero gate voltage) since the modulation doped channel retains the electrons at zero gate bias which can only be depleted off at negative gate bias. The non-planar $In_{0.53}Ga_{0.47}As$ FINFET with fin thickness of 30nm and fin height of 60nm exhibits a positive threshold voltage since the device operates in the inversion mode. The nonplanar modulation doped $In_{0.70}Ga_{0.30}As$ MuQFET has a quantum-well thickness of only 14nm (below the critical layer thickness of $In_{0.70}Ga_{0.30}As$ on InP) and, unlike the planar QWFET, the threshold voltage of the MuQFET is tunable from depletion mode to enhancement mode by simply reducing the fin thickness from 60 nm to 15nm. Figure 3a depicts the electron density profile in the fin cross-section of the FINFET and the MuQFET devices at a fixed gate voltage overdrive, $V_G - V_T$, of 0.2V. The MuQFET devices exhibit the highest drive current among all the three device configurations. Figure 2(b) plots the effective mobility of the conduction band electrons in the FINFET and MuQFET devices as a function of their operating effective electric field at $V_G - V_T = 0.2V$.

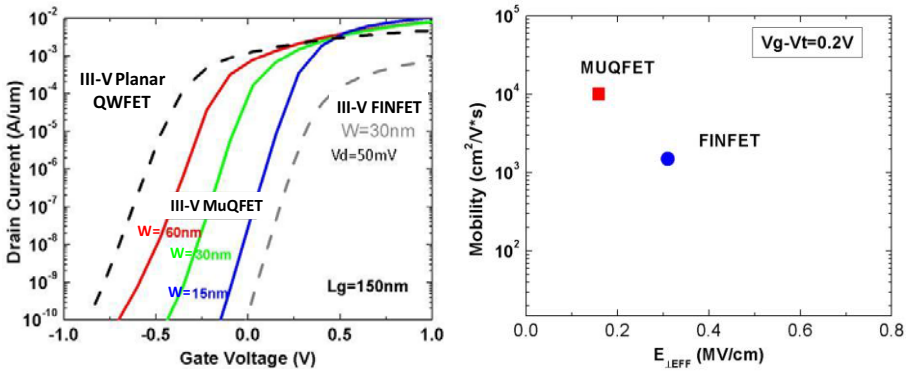

Figure 2 (a) Simulated transfer characteristics of $In_{0.70}Ga_{0.30}As$ quantum-well FET, $In_{0.53}Ga_{0.47}As$ FINFET and non-planar modulation doped $In_{0.70}Ga_{0.30}As$ MuQFET for V_{DS} = 0.05V and gate length, Lg, of 150nm; (b) Effective electron mobility of conduction band electrons in $In_{0.70}Ga_{0.30}As$ MuQFET and $In_{0.53}Ga_{0.47}As$ FINFET as function of the electric field for a given V_G-V_T = 0.2 V.

Interestingly, in FINFETs, due to the surface inversion, carriers accumulate along the two sidewalls and the top surface of the fin causing higher scattering and lower mobility. In contrast, for the MuQFET devices, the carriers are more uniformly spread along the entire width of the fin resulting in pronounced volume conduction and less impact of scattering of the carriers from the etched sidewalls (Figure 3a).This results in much higher mobility and drive current in MuQFET devices compared to their FINFET counterpart. Figure 3b shows the conduction band profile for the FINFET and MuQFET devices further confirming the enhanced bulk conduction phenomenon in the latter.

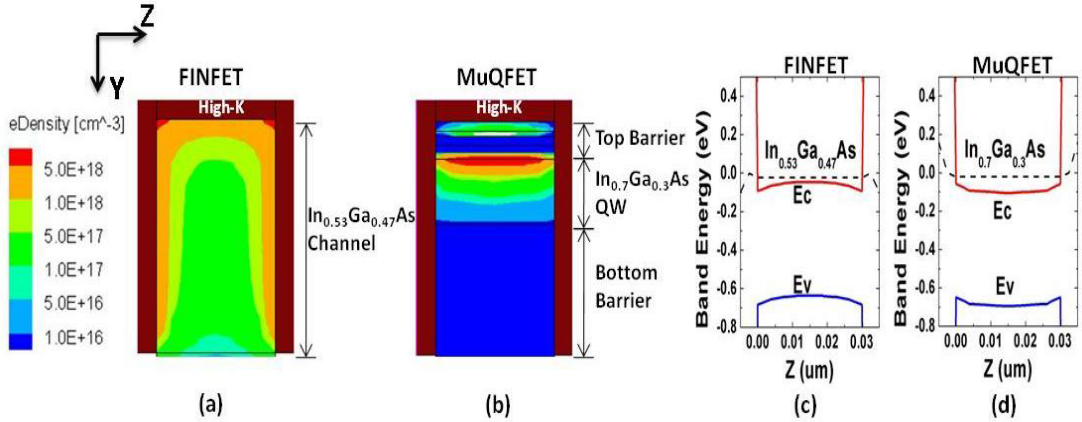

Figure 3 (a)-(b) Electron density along the fin cross-section for $In_{0.53}Ga_{0.47}As$ FINFET and $In_{0.70}Ga_{0.30}As$ MuQFET; (c)-(d) conduction band profile along the fin width direction for $In_{0.53}Ga_{0.47}As$ FINFET and $In_{0.70}Ga_{0.30}As$ MuQFET.

Modulation Doped $In_{0.7}Ga_{0.3}As$ MuQFET Device Fabrication

Modulation doped $In_{0.70}Ga_{0.30}As$ MuQFET devices were fabricated using molecular beam epitaxy (MBE) grown quantum well heterostructure as shown in Figure 4(a). The high mobility $In_{0.7}Ga_{0.3}As$ (11,000 $cm^2V^{-1}s^{-1}$ room temperature Hall mobility) channel is sandwiched between two adjacent layers of $In_{0.52}Al_{0.48}As$ barrier and is modulation doped by the delta doped n-type layer in the top barrier through a 4nm spacer layer. Using

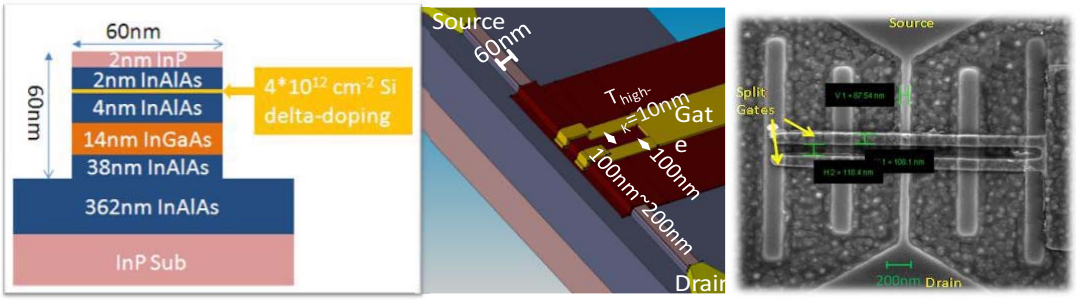

Figure 4 (a) Modulation doped $In_{0.70}Ga_{0.30}As$ quantum well layer structure grown by Molecular Beam Epitaxy (MBE); (b) Schematic of the $In_{0.70}Ga_{0.30}As$ MuQFET with a pair of wrap-around split gates; (c) Top-down SEM image of the fabricated $In_{0.70}Ga_{0.30}As$ MuQFET with 60 nm wide fin (80nm wide including the 10 nm Al_2O_3 dielectric on both sidewalls). Fins are patterned using electron beam lithography. Nested dummy fins are included to avoid thinning of the center fin due to electron deflection effect.

electron beam lithography, fins of varying widths (ranging from 60nm to 500nm) and flared source/drain regions are patterned. A low power BCl_3/Ar plasma dry etch is employed to etch the fin sidewalls to an isolation depth of 60nm. This isolation depth was selected to reach the wide gap $In_{0.52}Al_{0.48}As$ bottom barrier and was considered sufficient to provide device to device isolation, particular at lower than room temperature operating ambient condition. In the future, a more anisotropic dry etch will be employed to etch the fins down to the semi-insulating InP substrate for more robust device isolation. The nested dummy fins crowding the central active fin are intentionally incorporated to reduce the electron deflection error during e-beam pattering due to the underlying semi-insulating substrate. The source/drain metallization is achieved by Ni(10nm)/Ge(30nm)/Au(80nm) evaporation and lift-off. Ni is pre-deposited to help Ge (n type) diffuse in and make direct contact to the quantum well. A 350°C annealing in the N_2 ambient for 90s is used to form the alloyed ohmic contacts. A 10nm thick Al_2O_3 high-k dielectric is deposited using atomic layer deposition (ALD) with H_2O and TMA as the precursors at 300°C. A pair of wrap-around split gates are defined using electron beam lithography and formed using Ti (10nm)/Ni(10nm)/Au (80nm) by evaporation and lift-off process. While for classical FET operation, a single gate is enough to modulate the channel conductivity and provide device operation, we are also interested in the non-classical quantum mode operation of the fabricated device for low supply voltage logic operation (5). The pair of split gates is incorporated to transform the quantum wire MuQFET into a quantum dot by confining the electrons along the channel length as well. A Cl_2 plasma dry etch process is used to etch the Al_2O_3 dielectric to open the source/drain contact regions. The device structure is depicted in Figure 4(b) and a top view scanning electron micrograph (SEM) is shown in Figure 4(c).

Device Characterization

Classical Transistor (FET) Operation: The fabricated devices are measured with an HP4156A semiconductor parameter analyzer over wide a range of temperature (4.2K to 300K). The room temperature transfer characteristics of the $In_{0.70}Ga_{0.30}As$ MuQFETs with

different fin widths are shown in Figure 5(a). The threshold voltage, as predicted by the simulation results, shifts positively with scaling of the fin width. This indicates that the depletion effect from sidewall induced by the difference in the work function between the gate metal electrode and the semiconductor as well as the surface states is becoming more significant with the reduction in the fin dimension, as the MuQFET transitions from a top gate configuration to the multi-gate configuration. The substrate leakage, most likely due to conduction through the $In_{0.52}Al_{0.48}As$ barrier layer, adversely affects the off-state performance of the transistors at room temperature, which would be much improved by cooling down the devices. The low temperature transfer characteristic is shown in Figure 5(b) with Ion-Ioff ratio exceeding 2×10^5. The gate leakage is also suppressed (< 10^{-11}A/um) from the use of high-k dielectric instead of the Schottky gate. In Figure 5(c), the fabricated devices with 60nm fin width exhibit excellent transistor output characteristics. The highest on-current achieved in the fabricated $In_{0.70}Ga_{0.30}As$ MuQFET devices is 60 uA/um at V_{DS} = 0.5V. The device pinch-off occurs at 250mV implying high device self-gain at very low supply voltage.

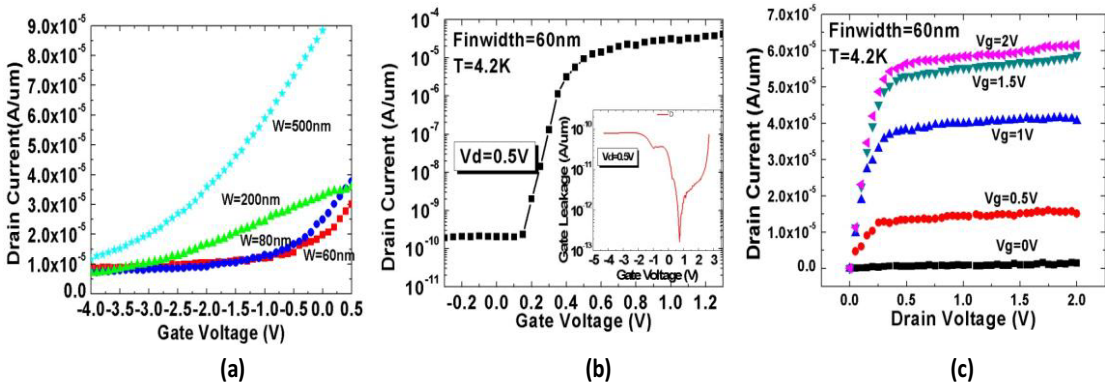

Figure 5 (a) Room temperature transfer characteristics of the $In_{0.70}Ga_{0.30}As$ MuQFET for different fin widths ranging from 500nm to 60nm. The threshold voltage positive shift is observed with scaling of the fin width as expected from device simulations; (b) Transfer characteristic of $In_{0.70}Ga_{0.30}As$ MuQFET with 60nm fin width at 4.2K; (c) Output characteristic of the MuQFET with 60nm fin width at 4.2K.

Non-classical Single Electron Transistor (SET) Operation: The fabricated devices are also measured in the very low drain bias regime (1-2mV) at 4.2K. A drain conductance fluctuation is observed as shown in Figure 6(a). The contour map of the drain conductance suggests formation of a partial coulomb diamond-like shape is shown in Figure 6(b). The drain conductance fluctuation behavior can be attributed to true coulomb oscillations resulting from single electron tunneling into the bound states present in the dot under low drain bias, as the potential of the dot is tuned using the gate bias. 3D numerical simulations are conducted to explore the size of the quantum dot (Figures 7(a)-(b)). At Vg=-0.26V, the tunneling resistance is 2.5MOhm (greater than h/e^2) which is calculated from the I-V simulation of the electrostatically defined tunnel junction at low bias. In this gate bias regime, the electrons are confined in a coulomb island with two

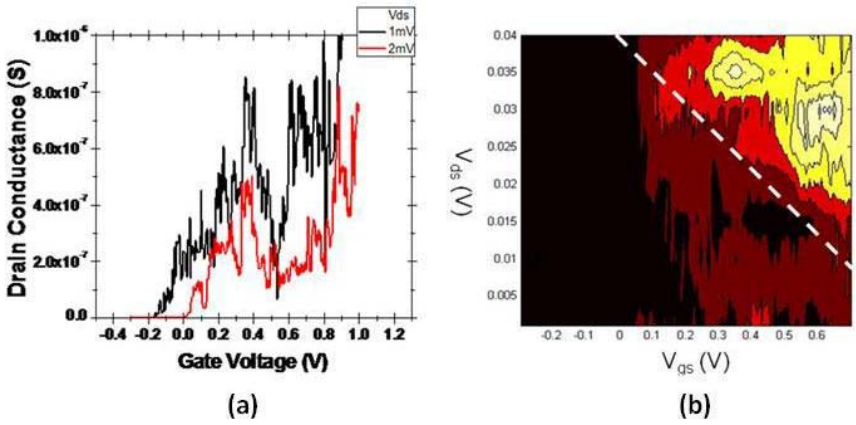

Figure 6 (a) Measured drain current conductance as a function of gate bias for Vd = 1mV and 2 mV at 4.2K; (b) Contour map of the measured drain current fluctuation; a partial diamond is observed in the conductance fluctuations with the white dashed line showing the edge of the partially formed diamond, suggesting single electron charging behavior

quantum point contacts to the source/drain electron reservoirs. The dot boundary is roughly defined by the conduction band profile and is estimated to be of 90nm×60nm×14nm. With an electron density close to 10^{16}cm^{-3} (Figure 7(b)), a few

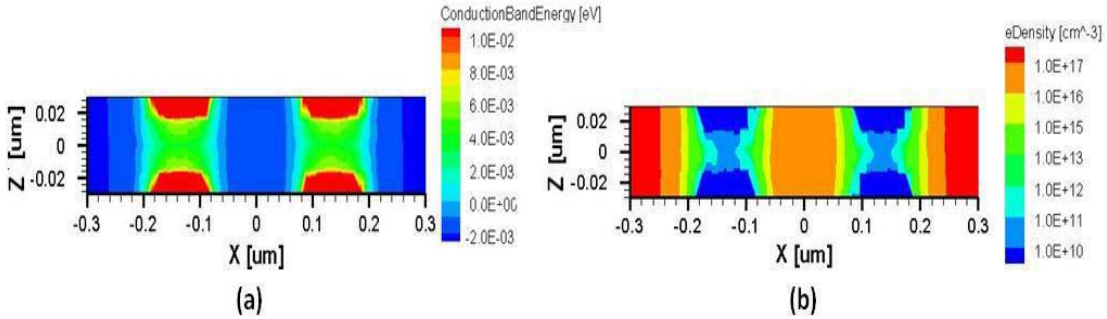

Figure 7 (a) Simulated conduction band profile of the split gate $In_{0.7}Ga_{0.3}As$ MuQFET at Vg=-0.26V, Vd=0V, E_{Fermi}=0V to estimate the size of the quantum dot (top down view). The quantum dot dimension is estimated to be 90nm (split gate electrostatics) × 60 nm (fin width) × 14 nm (quantum well thickness), which suggests one electron for an induced eDensity of 1.3×10^{16} cm^{-3}; (b) simulated eDensity in $In_{0.7}Ga_{0.3}As$ channel under the same bias condition.

electron operation of this transistor is confirmed. It is to be noted that the role carrier trapping/detrapping at the III-V/high-k interface in affecting the drain conductance fluctuation is not ruled out at this point. Further experiments are needed to verify this by including a plunger gate to in addition to the split gates to tune the potential of the dot, while maintaining electrostatic confinement.

Conclusions

In summary, multi-gate modulation doped $In_{0.7}Ga_{0.3}As$ quantum well FETs are simulated, fabricated and analyzed in detail. The devices are shown to be operated in both classical as well as in non-classical quantum regime. The FETs exhibit reasonable on current as well as excellent pinch off at very low drain voltages indicating its promise for low power CMOS digital logic applications. By incorporating a pair of wrap-around split gates, a quantum dot is realized in the $In_{0.7}Ga_{0.3}As$ MuQFET using a combination of split gate induced electrostatic confinement as well as fin width and quantum-well heterostructure induced structural confinement. Drain conductance oscillation is observed indicating potential coulomb blockade operation of the device. We believe that the modulation doped $In_{0.7}Ga_{0.3}As$ quantum well FET is promising device architecture for future ultra low power information processing applications.

References

1. S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady, and R. Chau, *Electron Device Letters, IEEE* **28**(8), 685 (2007).
2. K. Dae-Hyun and J. A. del Alamo, in *Electron Devices Meeting, 2008. IEEE International* (2008).
3. S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, in *Electron Devices Meeting, 2005. IEEE International* (2005).
4. Y. Q. Wu, R. S. Wang, T. Shen, J. J. Gu, and P. D. Ye, in *Electron Devices Meeting, 2009. IEEE International* (2009).
5. V. Saripalli, L. Liu, S. Datta and V. Narayanan, *Journal of Low Power Electronics* **6**(3), 415 (2010).
6. M. Radosavljevic, G. Dewey, J.M. Fastenau, J.Kavalieros, R. Kotlyar, B. Chu-Kung, W.K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah and R. Chau, in *Electron Devices Meeting, 2010. IEEE International* (2010).
7. *Sentaurus Device User Guide*, Version A-2007.12.