Applied Physics Express 4 (2011) 024105
DOI: 10.1143/APEX.4.024105

Experimental Staggered-Source and N+ Pocket-Doped Channel III–V Tunnel Field-Effect Transistors and Their Scalabilities

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Received December 8, 2010; accepted January 22, 2011; published online February 9, 2011

In this paper, we experimentally demonstrate 100% enhancement in drive current (I_{ON}) over $In_{0.53}Ga_{0.47}As$ n-channel homojunction tunnel field-effect transistor (TFET) by replacing $In_{0.53}Ga_{0.47}As$ source with a moderately staggered and lattice-matched $GaAs_{0.5}Sb_{0.5}$. The enhancement is also compared with $In_{0.53}Ga_{0.47}As$ N+ pocket (δ)-doped channel homojunction TFET. Utilizing calibrated numerical simulations, we extract the effective scaling length (λ_{eff}) for the double gate, thin-body configuration of the staggered heterojunction and δ-doped channel TFETs. The extracted λ_{eff} is shown to be lower than the geometrical scaling length, particularly in the highly staggered-source heterojunction TFET due to the reduced channel side component of the tunnel junction width, resulting in improved device scalability.

Tunnel field-effect transistors (TFETs) have gained tremendous interest recently owing to their potential in achieving sub-kT/q steep switching slope (SS) at room temperature (RT) and thus enabling higher on-current for a given on-state-to-off-state current ratio at very low supply voltages.[1–9] However, due to the relatively large tunneling barrier (E_b) and width, silicon, germanium, and III–V based homojunction TFETs (Homj-TFETs) still face major challenges in demonstrating metal–oxide–semiconductor field-effect-transistor-like large drive currents (I_{ON}) which is a prime requirement for any high-performance logic application.[1,6] It has been theoretically shown that I_{ON} can be further enhanced over Homj-TFET by employing i) a staggered heterojunction source or ii) an N+ pocket (δ)-doped channel, without paying any penalty for ambipolar leakage.[6,8] However, for either case, a complementary experimental demonstration is absent in the category of III–V-based TFETs which form a natural choice for enhancing the on-current (I_{ON}) with the availability of a large pool of lattice-matched, narrow-gap, and small-tunneling-mass semiconductors having different band-edge alignments.

In this work, we provide separate demonstrations of I_{ON} enhancement over n-channel $In_{0.53}Ga_{0.47}As$ Homj-TFET by a) replacing the $In_{0.53}Ga_{0.47}As$ source with lattice-matched, staggered $GaAs_{0.5}Sb_{0.5}$ (Hetj-TFET) and b) putting a thin δ-doped layer within the channel adjacent to the p+ source (δ-doped TFET). Both techniques result in a 100% (2×) increase in I_{ON} over Homj-TFET at $V_{DS} = 0.75\,V$ and $V_{GS} = 2\,V$ with the Hetj-TFET exhibiting a high I_{ON} of $60\,\mu A/\mu m$ at $V_{GS} = 2.5\,V$. Using two dimensional numerical simulations,[12] we compare the scalability of staggered-source Hetj-TFET, δ-doped TFET and Homj-TFET using ultrathin-body double-gate (UTB-DG) device configuration operating at supply voltage of 0.5 V.

Figures 1(a)–1(c) show cross-sectional schematic of the fabricated vertical n-channel Homj, Hetj and δ-doped TFET devices. The layers were epitaxially grown using molecular beam epitaxy (MBE) on a semi-insulating indium phosphide (InP) substrate. The P+ source regions comprise of 60-nm-thick $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.5}Sb_{0.5}$ layer for the Homj- and Hetj-TFETs, respectively, both carbon doped at $10^{20}/cm^3$. The 100 nm channel consists of intrinsically doped $In_{0.53}Ga_{0.47}As$. For δ-doped TFET, an ultrathin 3-nm-thick $In_{0.53}Ga_{0.47}As$ layer adjacent to the source, doped n-type with Si at $5 \times 10^{19}/cm^3$, is incorporated within the 100 nm channel of the Homj-TFET to form the N+ pocket. The N+ drain region is formed by 300-nm-thick $In_{0.53}Ga_{0.47}As$ layer, doped with Si at $10^{19}/cm^3$.

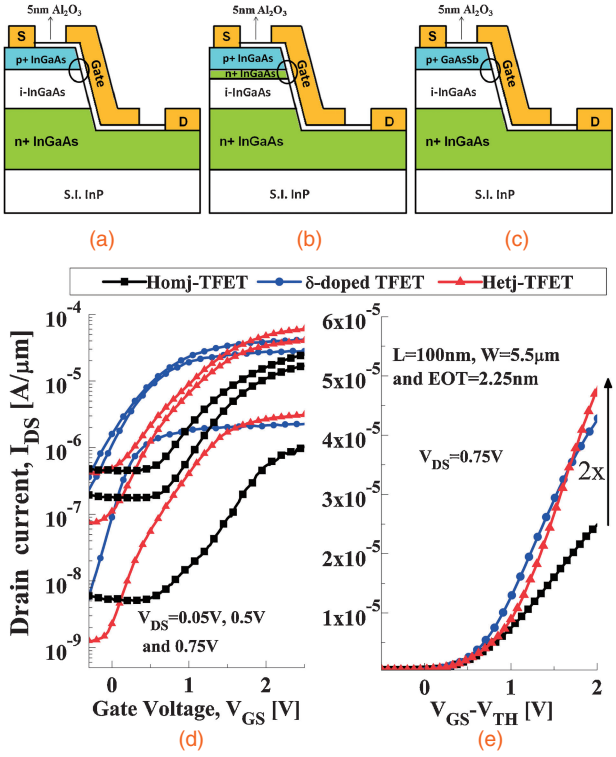

Fig. 1. (a–c) Cross sectional schematics of the fabricated InGaAs Homj-TFET, δ-doped-TFET, and GaAsSb source Hetj-TFET respectively ($L = 100\,nm$, $W = 5.5\,\mu m$ and EOT = 2.25 nm). (d) Measured I_d–V_g characteristics at V_{DS} of 0.05, 0.5, and 0.75 V. (e) I_d–V_g comparison at $V_{DS} = 0.75\,V$ on a linear scale with the turn-on voltages normalized to that of the Homj-TFET. Both moderately staggered Hetj-TFET and δ-doped TFET show 100% (2×) I_{ON} enhancement over Homj-TFET at $V_{GS} = 2\,V$.

The epilayers were patterned into a vertical mesa structure using BCl_3/Ar based reactive ion etching (RIE) followed by a conformal deposition of a 5-nm-thick plasma-enhanced atomic-layer-deposited (PEALD) high-k dielectric (Al_2O_3) at 200 °C.[10] Electron beam evaporation and lift-off techniques were used to form the sidewall gate (Pd/Au)

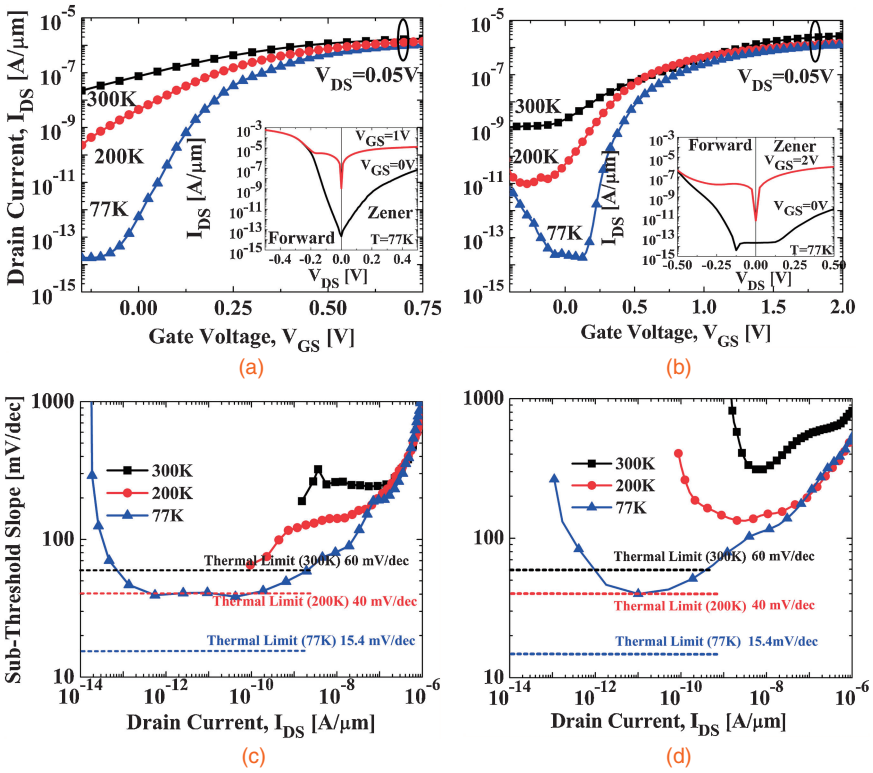

Fig. 2. (a, b) I_d–V_g at different temperatures for δ-doped-TFET and Hetj-TFET respectively at $V_{DS} = 0.05$ V. Insets show output characteristics at 77 K. NDR in the forward side confirms tunneling mechanism in respective devices. (c, d) Point SS plotted as a function of drain current at different temperatures for the δ-doped-TFET and Hetj-TFET, respectively.

electrode as well as the source/drain (Ti/Pd/Au) contacts. Finally, device isolations were performed using consecutive steps of RIE (for the removal of oxide) and citric acid-based wet etch all the way to the semi-insulating InP substrate.

Figure 1(c) shows the experimental RT transfer characteristics (I_d–V_g) of the Homj-TFET, δ-doped TFET and Hetj-TFETs at V_{DS} of 0.05, 0.5, and 0.75 V. Hetj-TFET exhibits maximum I_{ON} of 60 μA/μm at $V_{DS} = 0.75$ V and $V_{GS} = 2.5$ V, the highest value measured till date in any III–V material system in the category of tunnel FETs even with an equivalent oxide thickness (EOT) of 2.25 nm.[5] Both δ-doped TFET and Hetj-TFET turn-on at a lower gate voltage (V_g), compared with the Homj-TFET (fabricated with the same process flow) and, hence, we normalize the gate voltage with respect to the turn-on voltage in order to benchmark the two devices. Figure 1(d) shows the I_d–V_g comparison at $V_{DS} = 0.75$ V. At $V_{GS} = 2$ V, both Hetj-TFET and δ-doped TFET with $I_{ON} \sim 46$ μA/μm show 100% (2×) enhancement over the Homj-TFET ($I_{ON} \sim 23$ μA/μm). The expected enhancement is due to the lowering of both the source side tunneling width and the effective tunneling barrier in the case of the staggered-source TFET,[8] while in the case of the δ-doped TFET it is mainly due to the reduction in the tunneling width for the same tunneling barrier.[6]

Figures 2(a) and 2(b) show the measured I_d–V_g at 300, 150, and 77 K. RT leakage floors are elevated and the measured SS is higher than the 60 mV/dec thermal limit. However, both decrease significantly at low temperatures at a rate faster than the linear dependence of kT/q with respect to temperature T, with a minimum point value of 40 mV/dec at 77 K as shown in Figs. 2(c) and 2(d). The degradation in SS at high temperatures is attributed to trap-assisted tunneling followed by thermionic emission via large mid-gap interface state density.[11] Insets in Figs. 2(a) and 2(b) show the output characteristics at 77 K. Negative differential resistance (NDR) in the drain-to-source forward bias regime, at high V_{GS}, confirms the presence of a gated tunneling junction for both the fabricated devices.

I_{ON} in our devices can be further improved by increasing the electrostatic gate control and by increasing the amount of stagger in the III–V Hetj-TFET.[8,9] However, it is also important to identify whether these enhancement techniques lead to the improvement or degradation in TFET device scalability. To compare the device scalability numerically, we consider a UTB-DG structure with body (T_{SI}) thickness of 7 nm, high-k gate dielectric thicknesses (T_{OX}) of 2.5 nm and an effective EOT of 1 nm. We consider four TFET structures: (a) $In_{0.53}Ga_{0.47}As$ Homj-TFET, (b) $In_{0.53}Ga_{0.47}As$ δ-doped-TFET, (c) moderately staggered $GaAs_{0.5}Sb_{0.5}$/$In_{0.53}Ga_{0.47}As$ Hetj-TFET with effective E_b of 0.5 eV (similar to the one fabricated in this work), and (d) highly staggered lattice-matched $GaAs_ySb_{1-y}/In_{1-x}Ga_xAs$ heterojunction with an effective E_b of 10 meV. Case (d) with an effective E_b of 10 meV can be realized with $y = 0.1$ and $x = 0.0$[13] However, in order to account only for the effect of the increase in stagger on the scalability of TFET, bandgap and dielectric constants of source, channel and drain materials for case (d) were kept the same as those for the case (c). A dynamic non local band-to-band tunneling (BTBT) model was used to compute the tunneling current.[12] Reduced tunneling mass and the change in bandgap due to thin-body quantization were obtained using Nextnano3 and included in the numerical simulations.[13]

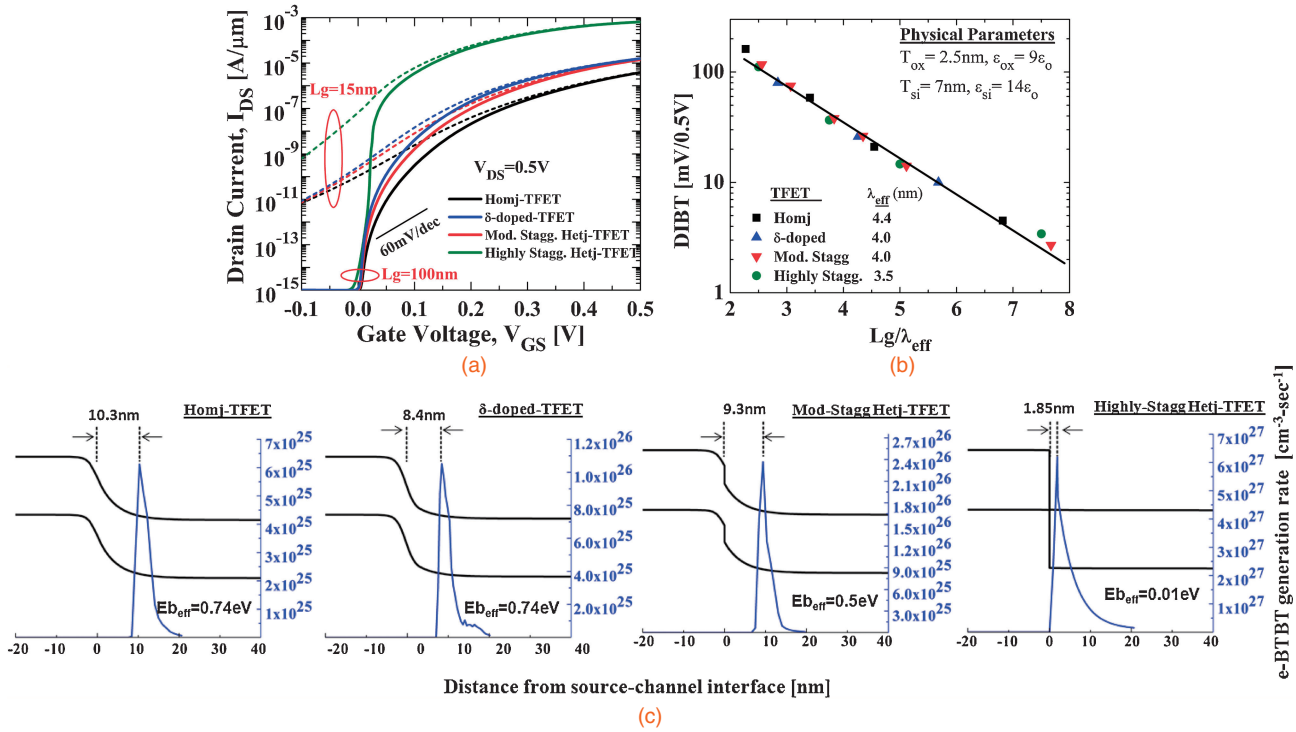

Fig. 3. (a) Simulated I_d–V_g for UTB-DG Homj-TFET, δ-doped TFET, moderately staggered Hetj-TFET and highly staggered Hetj-TFET for small and large channel lengths of 15 and 100 nm and $V_{CC} = 0.5$ V. (b) DIBT plotted vs gate (channel) length (L_g) normalized to λ_{eff} such that the DIBT values lie along one curve. Inset summarizes extracted λ_{eff}. (c) Electron BTBT generation rate profile plotted along the channel in the near turn-on regimes.

Figure 3(a) shows the simulated I_d–V_g for 15 nm (short) and 100 nm (long) gate (channel) length devices for the four TFET structures at a fixed supply voltage of 0.5 V. Figure 3(b) shows the drain-induced barrier thinning (DIBT) plotted as a function of the gate length which, in turn, is normalized to the respective effective electrostatic scaling length λ_{eff}. λ_{eff} for Homj-TFET was extracted from the exponential fit to the simulated potential profile along the channel.[14,15] For the rest of the TFETs, λ_{eff} was obtained by scaling λ_{eff} for Homj-TFET such that DIBT values for each of them followed a single curve. The extracted λ_{eff} is summarized as an inset in Fig. 3(b). The difference in the scaling lengths for different TFET device architectures can be understood by analyzing the electron band-to-band generation (e-BTBT) rate within the channel in the near turn-on regime [Figs. 3(c) and 3(d)]. Clearly, with stagger and pocket doping, the channel side component of tunneling width (x_{ch}) decreases bringing the peak in the generation rate closer to the source-channel junction. Since the electrostatic gate control is maximum near the source (away from the drain potential), the lower tunneling width in the channel leads to a lower λ_{eff} and, hence, higher device scalability. Highly staggered Hetj-TFET shows maximum scalability resulting from the lowest λ_{eff}.

In summary, I_{ON} enhancements over n-channel $In_{0.53}Ga_{0.47}As$ Homj-TFET are experimentally demonstrated by utilizing i) a staggered $GaAs_{0.5}Sb_{0.5}$ source and ii) an N+ pocket (δ)-doped channel. Both techniques show 100% enhancement in drive current over Homj-TFET at $V_{DS} = 0.75$ V and $V_{GS} = 2.0$ V, with the Hetj-TFET showing the maximum I_{ON} of 60 μA/μm at $V_{GS} = 2.5$ V. UTB-DG-TFET simulations were carried out to compare the scalability of staggered-source $GaAs_ySb_{1-y}/In_{1-x}Ga_xAs$ Hetj-TFET with those of $In_{0.53}Ga_{0.47}As$ Homj-TFET and δ-doped-TFET. While δ-doped TFET and moderately staggered Hetj-TFET show improved but similar scalability due to smaller tunneling width, highly staggered Hetj-TFET shows maximum scalability due to the lowest effective electrostatic scaling length resulting from the lowest tunneling width.

Acknowledgments This work was supported by the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND). We thank Professor Thomas N. Jackson, Department of Electrical Engineering, Pennsylvania State University at University Park for the low-temperature plasma-enhanced atomic layer deposition of Al_2O_3.

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