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Fabrication and Characterization of Axially Doped Silicon Nanowire Tunnel Field-Effect Transistors

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ABSTRACT Tunnel field-effect transistors were fabricated from axially doped silicon nanowire p-n junctions grown via the vapor−liquid−solid method. Following dry thermal oxidation to form a gate dielectric shell, the nanowires have a p-n-n^+ doping profile with an abrupt n-n^+ junction, which was revealed by scanning capacitance microscopy. The lightly doped n-segment can be inverted to p^+ by modulating the top gate bias, thus forming an abrupt gated p^+-n^+ junction. A band-to-band tunneling current flows through the electrostatically doped p^+-n^+ junction when it is reverse biased. Current−voltage measurements performed from 375 down to 4.2 K show two different regimes of tunneling current at high and low temperatures, indicating that there are both direct band-to-band and trap-assisted tunneling paths.

KEYWORDS Silicon nanowire, axial doping, vapor liquid solid, tunnel field-effect transistor, band-to-band tunneling

As metal oxide semiconductor field-effect transistor (MOSFET) power densities continue to rise at each technology node, tunnel field-effect transistors (TFETs) have emerged as an attractive low-power MOSFET replacement candidate.[1−5] A key metric of FET performance is the inverse subthreshold slope (*S*), a measure of the gate's control over current injection into the channel. Because MOSFETs rely on gate-controlled thermal injection of carriers into the channel, they are restricted to a minimum *S* of 60 mV/dec at room temperature, limiting the amount that the supply voltage can be reduced to lower power consumption. However, TFETs have been shown to be able to break the 60 mV/dec limit[2,3] because the gate controls tunneling through a barrier rather than emission over it, which filters out the high and low energy tails of the Fermi-Dirac distribution, permitting supply voltage scaling and power reduction.

Nanowire-based (NW) TFETs are predicted to provide improved device performance over their planar counterparts. Because nanowire devices have a circular geometry and a confined-volume body, a gate that wraps around the nanowire will provide excellent electrostatic control over the channel.[6−8] This improved channel control is expected to both reduce the *S* and improve the on-current of NW-TFETs.[6,9] Moreover, confinement effects such as the volume inversion of carriers[10] or the reduction of transverse momentum conservation requirements[11] may further enhance tunneling probabilities in nanowire systems. However, experimental NW-TFETs have not yet reached the dimensions necessary to see these improvements.[12−14] Nanowires grown by the vapor−liquid−solid (VLS) method have the capability to reach diameters below 10 nm[15] and also permit doped junctions and heterojunctions to be formed in situ,[16−18] allowing for the synthesis of complex device structures expected to enhance tunneling current.[19,20] Despite all of the theoretical benefits that a nanowire channel could provide to a TFET, most studies do not predict the effects that a confined geometry will have on the tunneling process itself, such as the impact of surface scattering or carrier confinement on the tunneling action.[21] Therefore, it is critical that the device characteristics of NW-TFETs be correlated to their material properties so that areas of improvement can be identified.

In this letter, we demonstrate NW-TFETs based on axially doped silicon (Si) nanowires grown by the VLS method. The doping profile following thermal oxidation of the as-grown p-n^+ Si nanowires is revealed by scanning capacitance microscopy (SCM), demonstrating a p-n-n^+ structure with an abrupt n-n^+ junction that can be electrostatically doped by the gate to a p^+-n^+ tunnel junction. Gate-dependent measurements of the NW-TFETs show that a reverse-biased tunneling current is induced in the nanowires at sufficiently negative gate biases. The temperature dependence of the tunneling current indicates that it is made up of both a direct band-to-band tunneling and a trap-assisted tunneling current component.

In situ axially doped p-n^+ Si nanowires were synthesized by the gold (Au)-catalyzed VLS method in a hot-wall low pressure chemical vapor deposition (LPCVD) reactor at a

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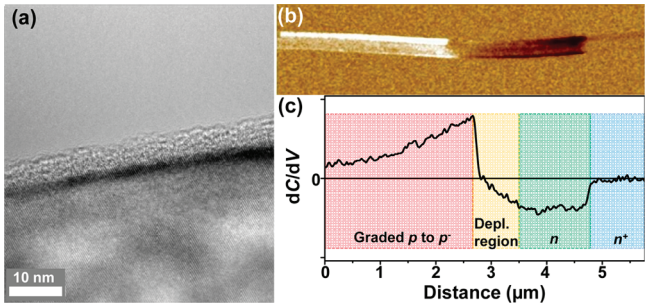

FIGURE 1. (a) TEM image of a 90 nm diameter Si nanowire oxidized at 800 °C for 15 min, resulting in a SiO_2 shell that is 4 nm thick. The wire is single crystal along its entire length. (b) SCM measurement of a thermally oxidized p-n^+ Si nanowire, showing d*C*/d*V* contrast. Bright areas correspond to p-type doping, while dark areas are n-type. The intensity is related to the magnitude of d*C*/d*V*. (c) Line scan of d*C*/d*V* determined by averaging across the width of the Si nanowire. The metallurgical junction is present where d*C*/d*V* = 0. The thermally oxidized nanowire has a graded *p*-region and an abrupt *n*-n^+ junction.

substrate temperature of 500 °C using silane (SiH_4) as the Si source gas and trimethylboron (TMB)[22] and phosphine (PH_3)[23] as the boron (B) and phosphorus (P) dopant sources, respectively. The Au catalyst nanoparticles were formed by heating a 3 nm thick layer of Au that was sputter deposited on an oxide-coated Si substrate, which gave as-grown nanowires with diameters between 60 and 100 nm. Axial doping was accomplished by abruptly switching from the initial dopant gas TMB to the second dopant gas PH_3 during VLS growth, with the growth times selected to form a 7 μm long p segment followed by a 5 μm long n segment. The dopant gas to SiH_4 flow ratios used to grow the p and n segments correspond to resistivities of $\sim 6 \times 10^{-2}$ (TMB) and $\sim 4 \times 10^{-3}$ (PH_3) Ω-cm as measured previously on uniformly doped Si nanowires.[23] The p segment was grown first to avoid depositing a radial p-type shell along the entire length of the Si nanowire,[24,25] which would short the p-n junction. A similar n-type overcoating has not been observed previously using PH_3 as an n-type doping source.[16,17,26]

A silicon dioxide (SiO_2) shell was grown by thermal oxidation of the Si nanowires to passivate the high density of interface trap states at the wire surface and to serve as the gate dielectric of the NW-TFETs.[27,28] After VLS growth, the native oxide was removed from the Si nanowires using a dilute hydrofluoric (HF) acid etch, followed by a selective wet etch to remove the Au catalyst nanoparticles from the tips of the wires. The Si nanowires then underwent a standard RCA cleaning procedure immediately prior to thermal oxidation at 800 °C in dry O_2 for 15 min, resulting in a SiO_2 shell of uniform thickness ranging from 3 to 5 nm depending on nanowire diameter, as observed by transmission electron microscopy (TEM) (Figure 1a). TEM analysis of oxidized Si nanowires also revealed that they were single crystal along their entire length from base to tip, with no visible radial Si overcoating or significant tapering.

In this work, the dopant gas was switched directly from TMB to PH_3 during VLS growth of the nanowire to create the most abrupt p-n junction possible. A graded transition region that is on the order of the nanowire diameter is expected between the p and n segments as residual B precipitates out of the Au catalyst into the wire and P is incorporated into the Au catalyst.[29] To measure the junction abruptness, the thermally oxidized Si nanowire p-n^+ junctions were examined by scanning capacitance microscopy (SCM).[30] The metalized AFM tip, the SiO_2 shell, and the Si nanowire core form a MOS capacitor, and the resulting change in capacitance, d*C*, with sample bias, d*V*, provides a measure of the doping density in the wire segment underneath the tip. In practice, an AC bias voltage is applied to the sample and d*C*/d*V* is measured directly. A moderately doped region can be easily depleted and accumulated by the tip bias and thus the amplitude of d*C*/d*V* will be large. In contrast, heavily doped regions are not easily depleted and lightly doped regions are not easily accumulated by the applied bias, and thus the amplitude of d*C*/d*V* will be very small. At the metallurgical junction d*C*/d*V* = 0. Although the amplitude of d*C*/d*V* is directly related to the Si nanowire doping density, the exact relationship depends on many factors, including the tip radius and the oxide thickness.[30] Thus, d*C*/d*V* is a measure of the relative doping density along the nanowire and an actual density cannot be extracted. The doping type of a given segment is derived from the slope (positive or negative) of the *C*−*V* curve with respect to the applied bias. Because d*C*/d*V* is a result of carrier accumulation and depletion, the depth of the sample that is probed by SCM is a function of the doping density and can vary from single to hundreds of nanometers for heavily and lightly doped segments, respectively.

The SCM measurement was performed by shorting together the ends of a single Si nanowire p-n^+ junction, electrically contacted by patterned metal electrodes, and applying a small signal AC voltage to the nanowire while a metallized atomic force microscope (AFM) tip was scanned across the wire. The SCM profile plotted in Figure 1c reveals that the magnitude of d*C*/d*V* is slightly larger on the p segment (far left side) than on the n^+ segment (far right side), showing that the p-type doping concentration is lighter than the n-type concentration, consistent with electrical measurements of uniformly doped Si nanowires.[23] The profile also shows an increasingly positive d*C*/d*V* from the 0 to 2.7 μm mark, followed by an increasingly negative d*C*/d*V* from the 2.7 to 3.5 μm mark. This indicates that the last section of the p segment is graded from p to p^-, followed by the depletion region. Between the right side of the depletion region and the n^+ segment, d*C*/d*V* is constant and negative, indicating that there is a $\sim$ 1.2 μm long moderately doped n segment. Notably, there is a sharp transition from the n to the n^+ segment near the 4.7 μm mark. Previous work on uniformly n^+-doped Si nanowires showed that the P concentration decreases exponentially from the surface to the core of the wire, reaching values of up to 10^{20} cm^{-2} at the surface.[31] Because SCM only probes the doping concentra-

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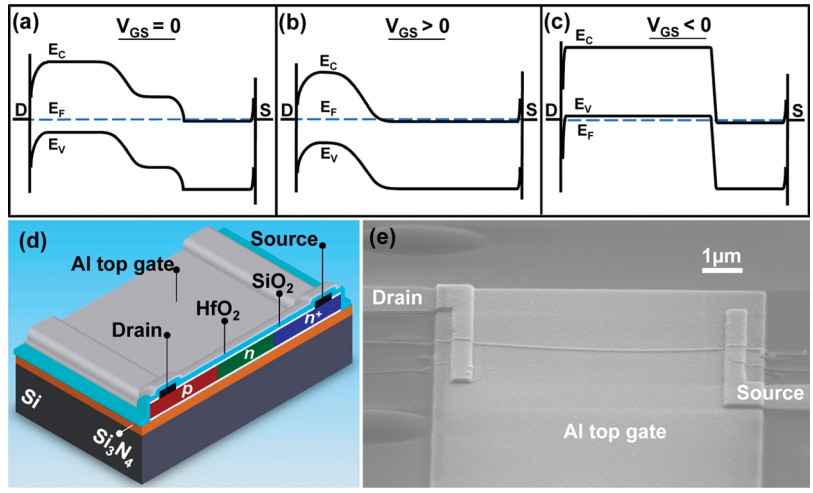

FIGURE 2. Energy band diagram at the Si/SiO_2 interface immediately below the gate along the length of the Si nanowire at (a) $V_{GS} = 0$, (b) a positive V_{GS}, and (c) a large negative V_{GS}. The source and drain contacts at the end of the nanowire are labeled in the diagram as "S" and "D", respectively. When $V_{GS} = 0$, the device behaves like a p-n junction. A positive V_{GS} accumulates the n segment, depletes the p segment, and widens the p-Schottky barrier. A negative V_{GS} inverts the n segment, accumulates the p segment, and narrows the p-Schottky barrier, creating an abrupt electrostatically doped p^+-n^+ junction. (d) Cross-sectional schematic of the Si NW-TFET device structure. The gate dielectric is composed of a thin SiO_2 shell surrounding the Si nanowire and 20 nm thick HfO_2 layer that covers the entire nanowire as well as the source and drain contacts. The Al gate overlaps the contacts to improve current injection into the p segment. (e) FESEM image of a fabricated Si NW-TFET.

tion in the topmost layer of the n^+ segment, the abrupt n-n^+ junction could be limited to the near surface region of the Si nanowires. In this case, gate controlled inversion of the n region would form an abrupt p^+-n^+ junction around the periphery of the wire at the Si/SiO_2 interface.

The SCM results show that even though the p- and n-type dopant gas sources were switched abruptly during VLS, a p-n-n^+ doping profile was obtained following thermal oxidation of the Si nanowires. The equilibrium diffusivities of both B and P in crystalline Si at the VLS growth conditions of 500 °C for 12 min or the oxidation conditions of 800 °C and 15 min are insufficient to explain the ~2.5 μm long graded p region and the >1 μm long uniform n region that separate the p- and n^+ end segments.[32] Large increases in diffusivity have been reported for low-temperature diffusion of Si with high defect densities, high P surface concentration, and large surface-to-volume ratio, suggesting that one or more of these mechanisms may be responsible for the observed profile.[31,32] Additional SCM studies are currently underway on as-grown and thermally oxidized p-n^+ Si nanowires to elucidate these mechanisms. However, it should be noted that the p-n-n^+ doping profile is critical to achieving the gated tunneling properties, as confirmed by the electrical measurements of the fabricated Si NW-TFETs.

A simplified energy band diagram of an electrically gated p-n-n^+ Si-SiO_2 core−shell nanowire, based on the SCM doping profile, is shown in Figure 2a. From measurements on uniformly doped Si nanowires, it is known that the moderately doped p and n segments can be inverted or depleted by an applied gate bias, but the n^+ segment is unaffected.[23] If a positive gate voltage, V_{GS}, is applied to the p-n-n^+ Si nanowire, the p segment will be depleted, the n segment will be accumulated, and the n^+ segment will remain n^+ (Figure 2b). However, when a negative V_{GS} is applied, the p segment will be accumulated to p^+, the n region will be inverted to p^+, and the n^+ region will again remain n^+ (Figure 2c). This results in an abrupt electrostatically doped p^+-n^+ junction at the chemically doped n-n^+ junction, permitting band-to-band tunneling current when this junction is reverse biased.

The top-gate NW-FET device structure illustrated in Figure 2d was used to study the electrical characteristics of single Si-SiO_2 p-n-n^+ core−shell nanowire junctions. The wires were removed from the growth substrate by ultrasonic agitation and suspended in isopropyl alcohol. This suspension was dispersed on a silicon nitride (Si_3N_4)-coated (120 nm) Si substrate and single wires were positioned at predetermined locations between large-area metal electrodes by electric-field assisted assembly.[33] Source (S) and drain (D) contacts were defined at the ends of the Si nanowires using electron-beam (e-beam) lithography. Following exposure and development of the e-beam resist, the SiO_2 shell in the contact areas was removed using a dilute buffered oxide etch (BOE) and Ti/Ni (120/120 nm) metal electrodes were deposited by thermal evaporation. Atomic layer deposition (ALD) was used to coat a 20 nm thick conformal HfO_2 layer over the entire device to serve as a gate dielectric and also to isolate the S/D contacts. Finally, a top-gate that overlapped the channel and the S/D contacts was patterned by e-beam lithography and 120 nm of Al was deposited using thermal evaporation. The overlapping Al top gate is necessary because of the Schottky barrier at the drain contact to the p segment, which limits current flow through the nanowire device.[34] The Schottky barrier can be narrowed by applying

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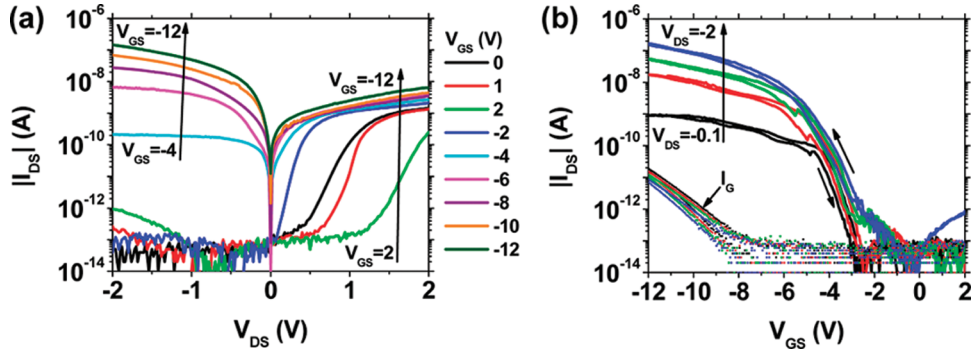

FIGURE 3. (a) I_{DS} vs V_{DS} at V_{GS} from 2 to −12 V for a single 90 nm diameter Si nanowire p-n-n$^+$ junction. As V_{GS} becomes increasingly negative, the reverse-biased tunneling current increases. (b) I_{DS} vs V_{GS} at negative V_{DS} of −0.1, −0.5, −1, and −2 V. The arrows indicate the bias sweep direction.

a negative V_{GS} to electrostatically dope the Si wire segment at the drain contact from p to p$^+$, improving current injection through the drain.[6,35] Because of uncertainty in the orientation of the p and n segments following assembly, the gate overlaps both the drain and the source contacts, as the latter is not significantly modulated by the gate field.

Current−voltage (I−V) measurements were performed on individual Si nanowire p-n-n$^+$ junctions, as shown in Figure 2e, in vacuum at room temperature. In all cases the source was grounded and voltage was applied to the drain, such that a positive drain-to-source voltage, V_{DS}, corresponds to a forward-biased p-n junction. The I_{DS}−V_{DS} characteristics of a single 90 nm diameter Si nanowire device collected at V_{GS} between −2 and 2 V (Figure 3a) show that the p-n-n$^+$ junction is rectifying with very little or no measurable reverse bias current and varying forward bias current, I_{DS}. As mentioned previously, the Schottky contact to the p segment can be modified via electrostatic doping with the gate. When the barrier is sufficiently wide ($V_{GS} \geq 0$ V, Figure 2a,b), the I_{DS}−V_{DS} characteristics are due to a p-n$^+$ junction diode and Schottky diode connected back-to-back in series. When a positive V_{DS} is applied, and the p-n$^+$ junction is forward biased, the p-Schottky diode is reverse biased, limiting the current through the p-n$^+$ junction. As V_{GS} increases from 0 to 2 V, the resistance of the p nanowire segment increases and the Schottky barrier widens, reducing the forward-biased I_{DS} through the nanowire. When a small negative V_{GS} is applied, the p segment accumulates holes, the Schottky drain contact is converted into an ohmic tunneling contact, and the forward-biased I_{DS} rises. At this condition, V_{DS} drops mostly across the p-n junction, and thus it is most appropriate to extract the p-n$^+$ junction diode properties when $V_{GS} = -2$ V. The extracted ideality factor is $n = 1.6$ and the reverse biased current is only weakly dependent on voltage. This indicates that carrier recombination and generation contributes to but is not the dominant source of current in these VLS-grown p-n$^+$ junctions.[36]

The I_{DS}−V_{DS} characteristics plotted in Figure 3a also show that a large reverse current arises and increases as V_{GS} decreases from −4 to −12 V. This can be attributed to band-to-band tunneling current in the p$^+$-n$^+$ junction that is formed by inverting the n segment and accumulating the p segment of the p-n-n$^+$ Si nanowire ($V_{GS} < 0$, Figure 2c). The I_{DS}−V_{DS} plot indicates that the p$^+$-n$^+$ junction current is resistance limited in both the forward and the reverse bias regimes. This resistance is a combination of the nanowire series resistance and the contact resistances. When V_{DS} is positive, the Schottky contact formed between the metal and the p$^+$ Si nanowire segment at a constant value of V_{GS} is reverse biased, giving a higher contact resistance than for negative V_{DS}. This results in a lower maximum forward diode current than reverse diode current for the same V_{DS} (magnitude) and V_{GS}.

Interband tunnel junctions typically have a peak and valley region with an area of negative differential resistance (NDR) under small forward biases, which is a consequence of electrons tunneling from the n$^+$ conduction band to the p$^+$ valence band over a narrow energy band.[37] Although these gated p$^+$-n$^+$ Si nanowire junctions exhibit an elevated forward-bias current at low V_{DS}, there is no sign of a current valley or NDR. This may indicate that the doping in the n$^+$ segment or the electrostatically doped p$^+$ segment is not degenerate enough to push the Fermi level well into the respective bands. Additionally, there may be tunneling current through trap states in the bandgap[38] that is on the order of or greater than the direct band-to-band tunneling current, masking the current valley and NDR.

Figure 3b shows the V_{GS} dependence of the reverse-biased tunneling current at values of V_{DS} between −0.1 and −2 V. There is minimal gate leakage current at all values of V_{DS}, which shows that the measured I_{DS} is dominated by current flowing through the Si nanowire p$^+$-n$^+$ junction diode. There is noticeable hysteresis in I_{DS} with gate bias sweep direction, suggesting that there is a high density of neutral oxide traps in the SiO_2 and HfO_2 gate dielectrics, a known concern of high-k dielectrics.[39] The tunneling current turns on with an S of approximately 370 mV/decade, well above the theoretical MOSFET limit of 60 mV/decade. However, the 20 nm

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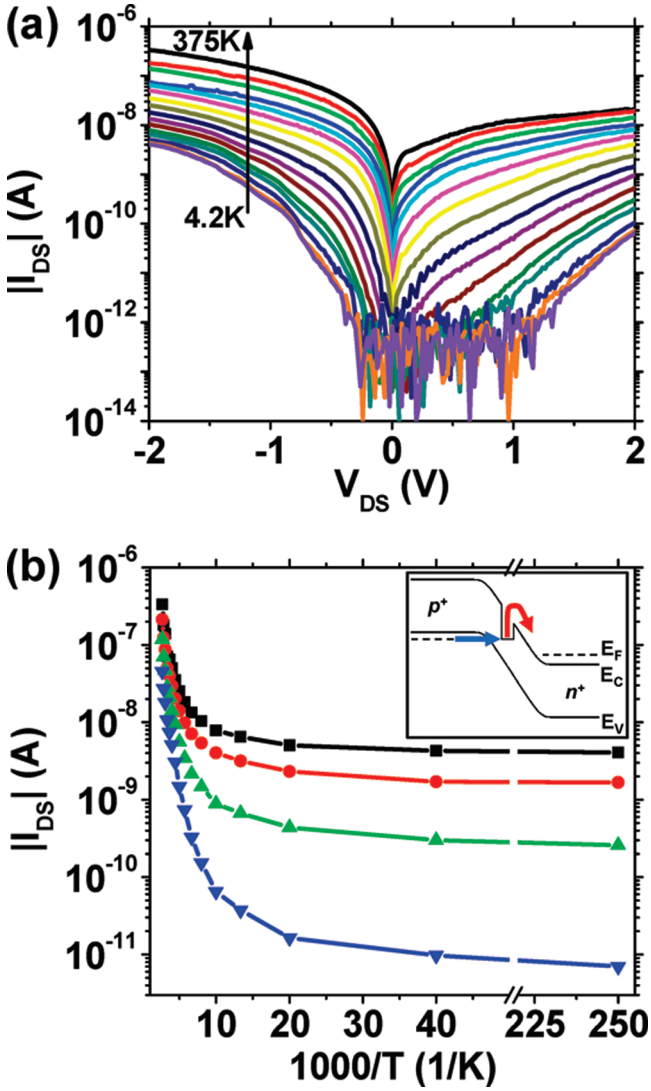

FIGURE 4. (a) I_{DS} vs V_{DS} at a constant V_{GS} of −10 V as a function of temperature from 375 K to 4.2 K in steps of 25 K. (b) The corresponding Arrhenius plot at V_{DS} of −2.0 (black squares), −1.5 (red circles), −1.0 (green triangles), and −0.5 V (blue inverted triangles). The current decreases exponentially with temperature at the highest temperatures but decreases little at the lowest temperatures. Inset: diagram showing the trap-assisted tunneling mechanism. Carriers tunnel from the valence band into a trap and are then thermally emitted into the conduction band.

HfO_2 gate dielectric is relatively thick, and a reduction in the gate dielectric thickness will improve the subthreshold slope.[6,9]

To confirm that the observed reverse-biased I_{DS} for $V_{GS} \leq -4$ V is due to band-to-band tunneling, temperature-dependent $I_{DS}-V_{DS}$ measurements were performed from 375 to 4.2 K (Figure 4a) at a constant value of $V_{GS} = -10$ V. Below the diode turn-on voltage, the forward-biased current decreases exponentially with temperature, following the p-n junction diode current $I_{DS} \sim \exp(V_{DS}/nkT)$.[36] The reverse-biased current also decreases with temperature, although not as dramatically as the forward-biased current, and there is still significant current at 4.2 K. The Arrhenius plot in Figure 4b shows that the reverse current decreases exponentially with temperature between 375 and 150 K. Below 150 K, the current becomes less temperature dependent, and between 75 and 4.2 K the current is nearly constant. While true direct tunneling current is temperature independent,[36] direct band-to-band tunneling in indirect bandgap semiconductors such as Si has a slight temperature dependence because of (1) the increase in the bandgap energy with decreasing temperature, and (2) the necessary involvement of phonons to satisfy momentum conservation requirements as electrons transfer from the valence to the conduction band.[40−43] The exponential temperature dependence at high temperatures suggests that the reverse-biased diode current in these Si NW-TFETs is composed of a direct tunneling current component and a trap-assisted tunneling (TAT) current component.[44]

The mechanism responsible for the TAT current component is illustrated in the inset of Figure 4b. Electrons from the valence band in the electrostatically doped p^+ Si nanowire segment tunnel partway through the bandgap into traps and are then thermally emitted out of the traps into the conduction band of the n^+ segment. In this high electric field tunneling regime, the activation energy determined from the slope of the Arrhenius plot at high temperatures decreases with increasing V_{DS} and V_{GS} (not shown), which is consistent with field-enhanced (Poole-Frenkel) thermal emission of electrons from the traps.[36] Because accurate values of the electric field in the gated junction region of these Si NW-TFETs are difficult to determine for all bias conditions, the actual trap energy could not be extracted from the measured field-dependent activation energies. Nevertheless, there are several likely causes of the TAT observed in these devices. First, it has been shown that there is a significant concentration of Au in the Si nanowires due to the VLS growth being Au mediated,[45,46] and Au is a well-known midbandgap trap in Si. Second, because transport occurs in the electrostatically doped p^+ inversion layer near the surface, it is also possible that interface states at the multifaceted Si nanowire surface could contribute to the TAT current.[47]

In summary, axially doped Si nanowire p-n^+ junctions were grown by the VLS method and fabricated into TFETs. Following thermal oxidation, SCM revealed that the Si nanowires have a p-n-n^+ doping profile with an abrupt n-n^+ junction. By using a top gate, the nanowires were electrostatically doped to form an abrupt p^+-n^+ tunnel junction. Without an applied gate bias, the Si nanowire diode current was a function of both the p-n junction diode and the p-Schottky diode, while with a negative gate bias a large reverse-biased tunneling current flowed through the Si nanowire. Temperature-dependent $I_{DS}-V_{DS}$ measurements showed that the tunneling current was due to both direct band-to-band tunneling and trap-assisted tunneling. This work demonstrates the importance of correlating the material properties of NW-TFETs to their device characteristics to facilitate performance enhancements.

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