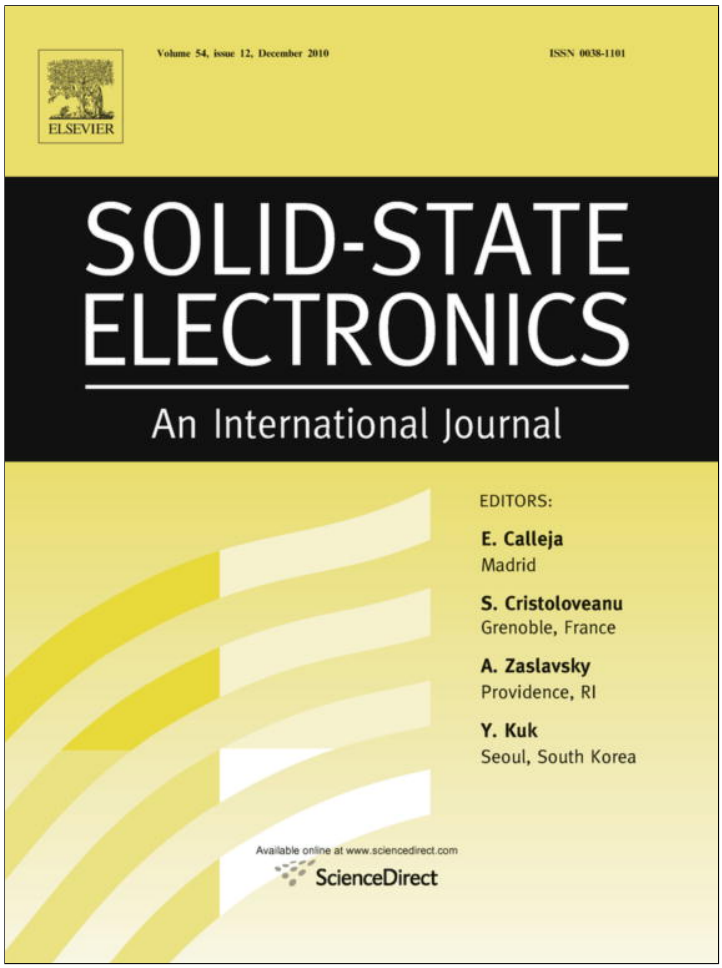

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# Effect of interface states on sub-threshold response of III–V MOSFETs, MOS HEMTs and tunnel FETs

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ABSTRACT

The effect of interface states on the current–voltage characteristics in the sub-threshold region of three different types of III–V based transistor architectures has been studied using a drift–diffusion based numerical simulator. Experimentally extracted interface state density profile is included in the simulation to analyze their effect on the sub-threshold response of InGaAs based MOSFETs, MOS HEMTs and tunnel FETs. Based on the Fermi-level position at the oxide/semiconductor interface and the corresponding interface state density ($D_{it}$), the sub-threshold response for the three devices can vary, with tunnel FETs having the least sub-threshold degradation due to $D_{it}$.



## 1. Introduction

Over the last four decades, logic transistor scaling following Moore's Law has resulted in unprecedented increase in logic performance. However, the exponentially rising transistor count has also led to increased energy consumption in modern VLSI devices. In order to aggressively scale the supply voltage ($V_{cc}$) for logic transistors, high mobility channel transistors (such as III–V based transistors) [1,2] and steep sub-threshold slope transistors [3] will be needed. It has been demonstrated that ultra-high mobility compound semiconductor-based MOSFETs and quantum well FETs (QWFETs) (e.g. $In_{0.7}Ga_{0.3}As$ and InSb) [1,2] operate at low $V_{cc}$ with high performance. InGaAs MOS HEMTs with InP composite barrier stack has been demonstrated with 3.5 times higher effective carrier velocity than strained Si *n*-MOSFETs [4]. In this work, we investigate the device performance in the sub-threshold region of three different types of III–V based transistor architectures using a drift–diffusion based numerical simulator. We analyze the impact of the interface state density ($D_{it}$) present at the high-$\kappa$ dielectric and $In_{0.53}Ga_{0.47}As$ interface on the sub-threshold response of each design, and discuss the advantages and disadvantages of each of the three architectures. In the next few sections, we describe the device architectures, the $D_{it}$ profile used in simulation, and discuss the effect of the $D_{it}$ on the performance characteristics of each device.

## 2. III–V based transistor architectures

Three different III–V channel based device architectures have been simulated and analyzed in this study. The two-dimensional (2D) layout of each device will be introduced in the following sub-section below. These include an inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, an accumulation mode buried channel InAs MOS HEMT, and an $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET.

### 2.1. Inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET

A cross section of the inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET is illustrated in Fig. 1a. This is a traditional, bulk MOSFET device design with 65 nm gate length. The simulated device consists of an $In_{0.53}Ga_{0.47}As$ substrate with the background p-type doping of $N_a = 1 \times 10^{18}$ cm$^{-3}$. On the top of the channel sits a 5 nm thick high-$\kappa$ oxide layer with 2 nm equivalent oxide thickness, which separates the surface channel from the metal gate. The metal gate work function used is 4.55 eV. The highly doped n-type source and drain regions are simulated using a Gaussian-type distribution with a peak doping dose of $N_d = 1 \times 10^{20}$ cm$^{-3}$ and junc-

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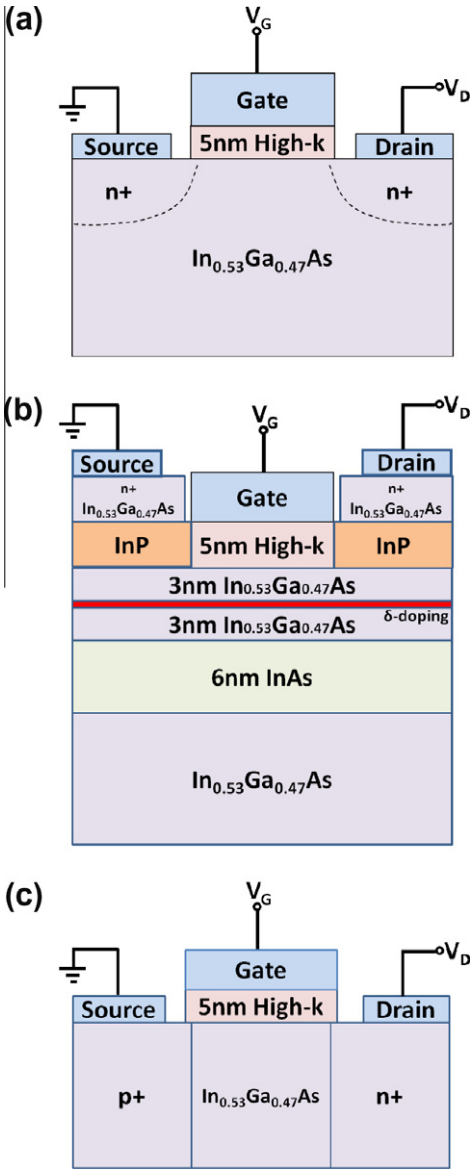


**Fig. 1.** Cross section of 65 nm gate length: (a) inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, (b) accumulation mode buried channel InAs MOS HEMT and (c) $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET.

tion depth of 20 nm. The interface state trap model is used at the interface between the high-$\kappa$ oxide layer and the $In_{0.53}Ga_{0.47}As$ substrate layer.

### 2.2. Accumulation mode buried channel InAs MOS HEMT

A cross section of the accumulation mode buried channel InAs MOS HEMT with $In_{0.53}Ga_{0.47}As$ burrier layer is illustrated in Fig. 1b. The gate length of this device is also 65 nm. The simulated device consists of a $In_{0.53}Ga_{0.47}As$ substrate, a 6 nm InAs channel, a 7 nm $In_{0.53}Ga_{0.47}As$ barrier layer, and 5 nm of high-$\kappa$ oxide layer with 2 nm equivalent oxide thickness below the metal gate. The region between the source/drain $In_{0.53}Ga_{0.47}As$ contact and the $In_{0.53}Ga_{0.47}As$ barrier layer are InP cap layers. The substrate, channel and barrier layers are undoped and remain intrinsic, the n-type source/drain region are uniformly doped at $N_d = 1 \times 10^{20}$ cm$^{-3}$. Finally, a 1 nm $\delta$-doping layer ($N_d = 5 \times 10^{19}$ cm$^{-3}$) is used at the middle of the $In_{0.53}Ga_{0.47}As$ barrier layer. The interface state trap model is used at the interface between the high-$\kappa$ oxide layer and the $In_{0.53}Ga_{0.47}As$ barrier layer.

### 2.3. $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET

A cross section of $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET with a 65 nm gate length is illustrated in Fig. 1c. The simulated device consists of a $In_{0.53}Ga_{0.47}As$ substrate, the majority of the p-type substrate is uniformly doped at $N_a = 1 \times 10^{15}$ cm$^{-3}$, the n$^+$ region at the source side is uniformly doped at $N_d = 1 \times 10^{19}$ cm$^{-3}$, and p$^+$ region at the drain side is uniformly doped at $N_a = 5 \times 10^{19}$ cm$^{-3}$. Similar to the inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, between the metal gate and the substrate sits a 5 nm thick high-$\kappa$ oxide layer with 2 nm equivalent oxide thickness, the metal gate work function is modeled as 4.55 eV. Tunneling happens under the high-$\kappa$ oxide layer between the n$^+$ region and the majority p-type substrate. The interface state trap model is used at the interface between the high-$\kappa$ oxide layer and the $In_{0.53}Ga_{0.47}As$ substrate layer.

## 3. Measured and simulated interface state density profile

The measured and simulated interface state density ($D_{it}$) profiles used in this work are plotted in Fig. 2. In each figure, zero corresponds to the position of the valence band, and the dot-line shows the position of the conduction band. Fig. 2a shows the experimentally measured $D_{it}$ profile at the interface of an in situ deposited $LaAlO_3$ high-$\kappa$ dielectric and $In_{0.53}Ga_{0.47}As$ interface and was recently reported in [5], this measured distribution of $D_{it}$ profile is extracted from the frequency dispersion in the $C$–$V$

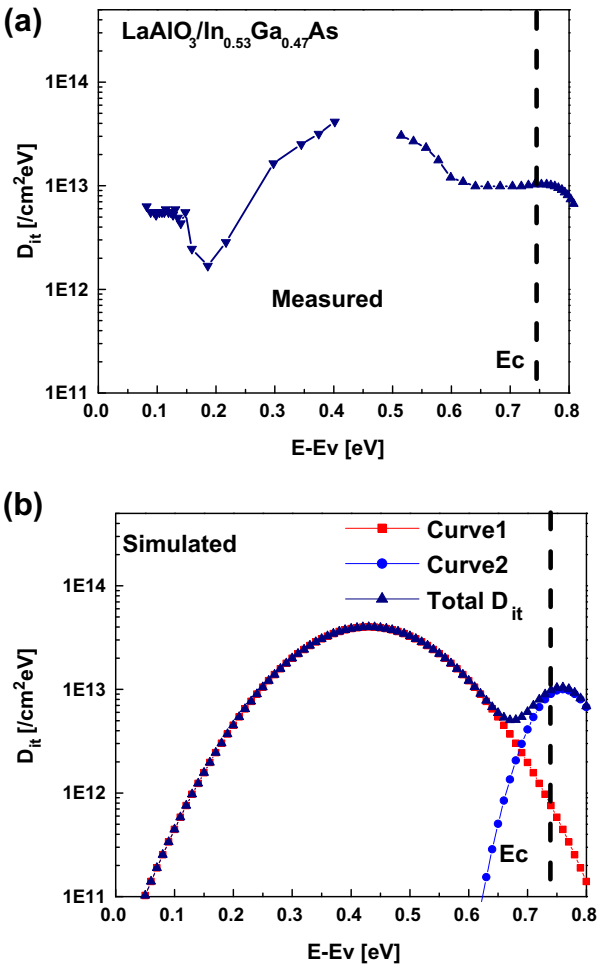


**Fig. 2.** (a) Extracted $D_{it}$ distribution from experiential measurement. (b) $D_{it}$ distribution used in simulations.

and the $G$–$V$ measurement of $LaAlO_3/In_{0.53}Ga_{0.47}As$ interface on a $In_{0.53}Ga_{0.47}As$ MOSFET, and by solving a small signal equivalent circuit, we can extract $D_{it}$, $\tau$ and $Q_{inv}$, and evaluate the energy voltage relationship by using true $Q_{inv}/V_G$ relationship. For our simulation purpose, we approximate the $D_{it}$ by superposition of two Gaussian trap distributions, the profile is plotted in Fig. 2b. The left Gaussian trap distribution which spans across a large portion of the band gap is likely due to the Ga–O or As–O bond defects, and the right distribution that extends into the conduction band is attributed to the As–As anti-bonding states [6]. In this study, the interface states are considered to be either donor states or acceptor states.

## 4. Impact of interface state on sub-threshold response

We present a drift–diffusion based numerical simulation and analysis of the affect of $D_{it}$ distribution present in two situations at the high-$\kappa$ dielectric and $In_{0.53}Ga_{0.47}As$ interface compare to the ideal case on the sub-threshold response of the three different types of transistor architecture: MOSFETs, MOS HEMTs and tunnel FETs. Figs. 3–5 show the simulated transfer characteristics at $V_D$ = 50 mV of the three devices along with their Fermi-level movement within the band diagrams as the device turn on.

### 4.1. Inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET

Fig. 3a shows the simulated transfer characteristics of MOSFET, the sub-threshold slope of no $D_{it}$ included is 81 mV/dec. When the drain current $I_{DS} = 10^{-11}$ A/μm, the Fermi-level sweeps the highest part of the $D_{it}$ distribution within the band gap, if the interface states were donor states, a significant portion of donor states stay positively charged as shown in Fig. 3b, resulting in severe degradation in sub-threshold slope (250 mV/dec). As the drain current increases, the Fermi-level will sweep though much smaller magnitude of $D_{it}$, the degradation in sub-threshold slope becomes less (119 mV/dec). When $I_{DS}$ increases to $10^{-5}$ A/μm, the Fermi-level enters the conduction band and the donor states stay neutralized, and there is almost no affect of the $D_{it}$. If the interface states were acceptor states, the acceptor states were negatively charged and resulting in a shift in threshold voltage ($V_T$).

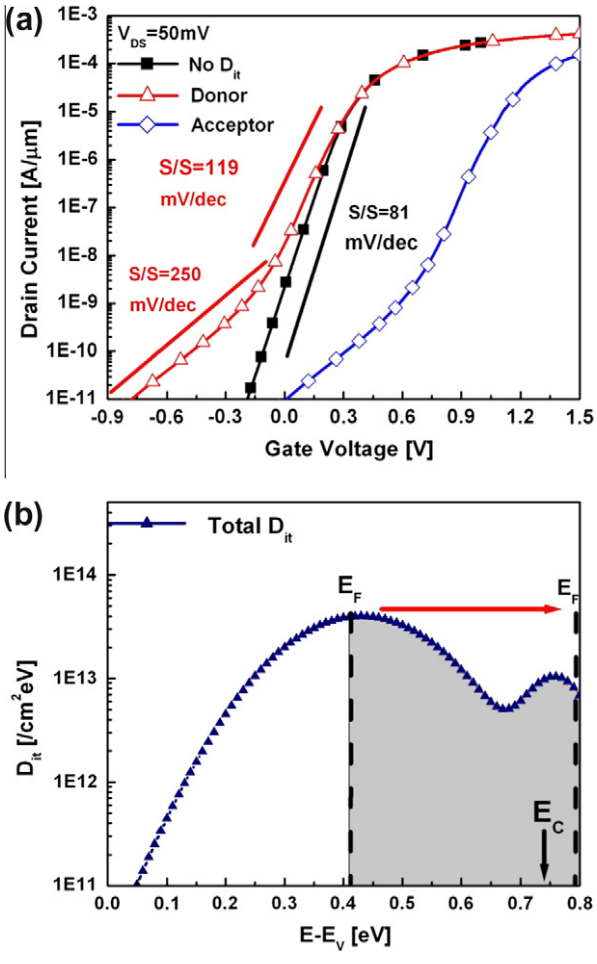


**Fig. 3.** (a) $I_D$–$V_G$ characteristics at low drain bias ($V_D$ = 50 mV) for inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET. (b) The Fermi-level position and movement from $I_{DS} = 10^{-11}$ A/μm to $I_{DS} = 10^{-5}$ A/μm.

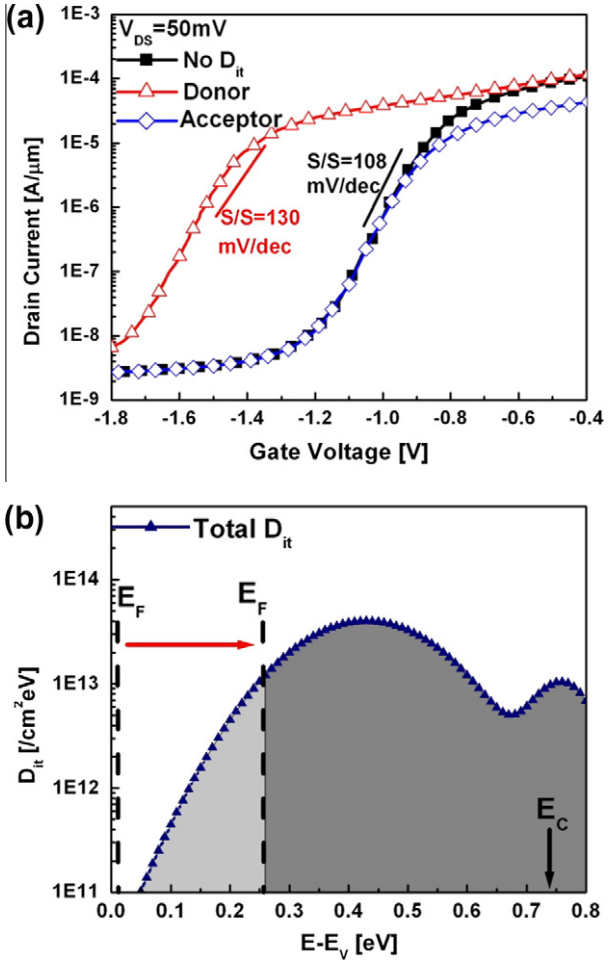


**Fig. 4.** (a) $I_D$–$V_G$ characteristics at low drain bias ($V_D$ = 50 mV) for accumulation mode buried channel InAs MOS HEMT. (b) The Fermi-level position and movement from $I_{DS} = 10^{-8}$ A/μm to $I_{DS} = 10^{-5}$ A/μm.

### 4.2. Accumulation mode buried channel InAs MOS HEMT

The impact of the $D_{it}$ distribution in MOS HEMTs leads the degradation in the sub-threshold slope less than MOSFETs as shown in Fig. 4a. The higher off-state current for this device compared to the InGaAs MOSFET is due to the generation–recombination of the InAs channel. For this architecture, when $I_{DS} = 10^{-8}$ A/μm, Fermi-level is very close to the valence band, if the interface states were donor states, all donor states stay positively charged. When $I_{DS}$ increases to $10^{-5}$ A/μm, as shown in Fig. 4b, the Fermi-level sweeps in the lower band gap, which is the lower $D_{it}$ portion of the distribution, part of the donor states is neutralized. The $V_T$ shift is due to significant amount of positively charged donor states.

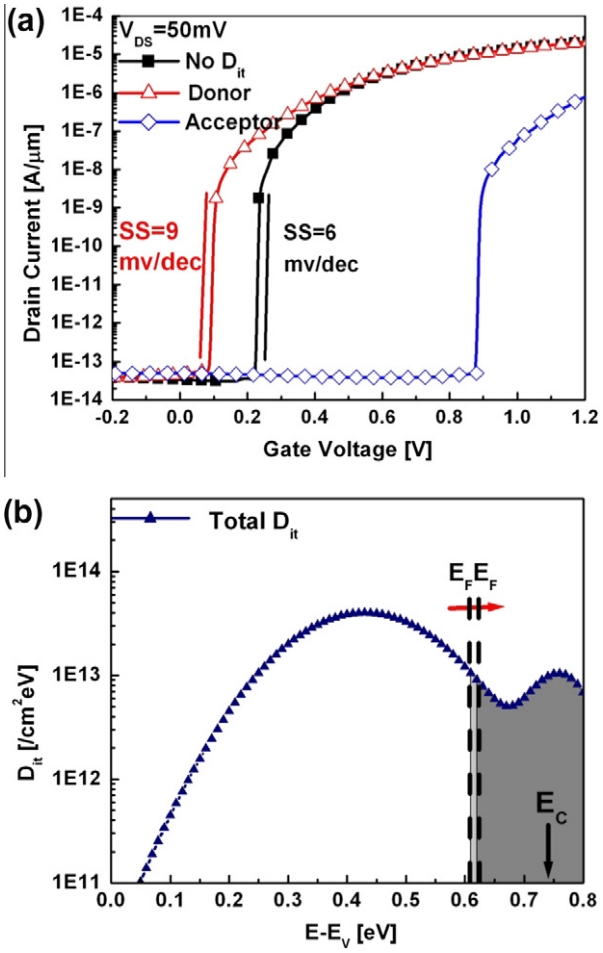


**Fig. 5.** (a) $I_D$–$V_G$ characteristics at low drain bias ($V_D$ = 50 mV) for $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET. (b) The Fermi-level position and movement from $6 \times 10^{-14}$ A/μm to $10^{-8}$ A/μm.

### 4.3. $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET

Tunnel FETs turns on abruptly when the valence band edge in the $p^+$ source region is raised above the conduction band edge in the channel which is already weakly inverted in the off-state, this gives rise to steep (<kT/q) sub-threshold slope. Fig. 5b shows that, when $I_{DS}$ increase from $6 \times 10^{-14}$ A/μm to $10^{-8}$ A/μm, the Fermi-level sweeps the interface by only a small amount (~0.01 eV), the steep sub-threshold behavior is retained as shown in Fig. 5a. Also, the $V_T$ shift is due to the positively charged donor states and negatively charged acceptor states.

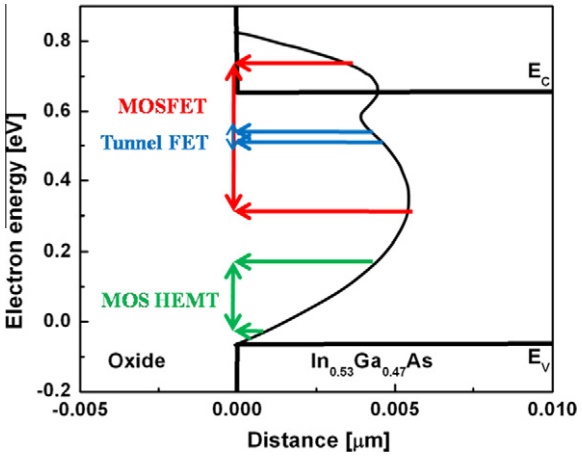


**Fig. 6.** Fermi-level movement for MOSFET, MOS HEMT and tunnel FET.

## 5. Conclusion

In this work, we have investigated how the same exact $D_{it}$ distribution at non-ideal $In_{0.53}Ga_{0.47}As$ and high-$\kappa$ dielectric can affect the sub-threshold response of III–V MOSFETs, MOS HEMTs and tunnel FETs though drift–diffusion simulations. It was demonstrated that according to the Fermi-level movement at the oxide/semiconductor interface of each the device architecture as in Fig. 6, the same $D_{it}$ distribution can affect the sub-threshold response of different transistor in different ways.

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