Energy-Delay Performance of Nanoscale Transistors Exhibiting Single Electron Behavior and Associated Logic Circuits

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Date of Receiving: **to be completed by the Editor**

Date of Acceptance: **to be completed by the Editor**

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Abstract *— In this paper, we characterize the Energy-Delay performance of logic circuits realized using Single Electron Transistor (SET) devices. As technology scaling progresses, it is getting increasingly challenging to continue reducing energy, especially at low activity factors and low* V_{CC}*, due to increasing leakage energy dominance. A SET can be viewed as the ultimate transistor operating in the limit of scaling; hence, we use this device as an example to understand the challenges of energy-reduction in the nanoscale. We explore the design space for SET-devices based on physical dimensions and electrostatic properties. Based on this design space, we characterize SETs into categories of applications: complementary-logic design, and BDD design with sense amplification. Based on these two circuit design styles, we compare the Energy-Delay products of benchmark logic circuits, implemented using nanometer CMOS and SETs.*

Keywords **—** Single Electron Transistor, Energy-Delay product, Complementary Logic Gate Design, BDD-Sense Amplifier Logic Design.

1 INTRODUCTION

Attaining low energy operation with low-to-moderate performance (10 KHz-100 MHz) is a desirable goal for a number of applications such as environmental monitoring sensors and biological implants. Such systems are typically characterized by infrequent activity cycles with energy drawn from a built–in battery. Thus, it is necessary to study how to minimize the energy consumption of switching circuits. The energy consumption of a logic module can be expressed as:

$$E_{total} = \alpha.(\frac{1}{2}.C_{Load}.V_{cc}^2) + I_{Leak}.V_{cc}.\tau_{switching} \quad (1)$$

As expression (1) shows, for a given technology node, the easiest way to minimize the total energy consumption is to scale the supply voltage, V_{cc}. However, in the case of CMOS, scaling V_{cc} can cause the logic circuit to operate below the threshold (V_T) causing an exponential increase in switching delay ($\tau_{switching}$). This can cause the leakage energy component to become the dominant contributor to E_{total}, especially for low activity (α) factors. Thus, the problem of minimizing E_{total} for a circuit topology turns into an optimization problem for which a number of approaches have been suggested [1] [2] [3].

While the optimizations mentioned above are good for optimizing E_{total} for a given technology node or a circuit topology, it is important to realize that the key contributor that actually drives the switching energy towards the theoretical minimum switching energy at room temperature, *kT.ln2* [4], is technology scaling. The load capacitances of the logic circuit due to gate and junction capacitances are cut in half with each technology generating, making each generation, switching energy wise, more energy efficient compared to the previous one.

$$I_{Leak}(V_{ds}) = \mu_{eff} C_{ox} \frac{W}{L}(m-1).(\frac{kT}{q})^2.e^{-qV_T/mkT}.(1-e^{-qV_{ds}/kT}) \quad (2)$$

As equation (2) shows, I_{Leak} has an exponential dependence on V_T. Given that V_T has to decrease at-least nominally with every technology generation in order to accommodate V_{cc} scaling [5], as equation (2) shows, the leakage current for a given V_{ds} increases with each technology generation. It is important to notice that even if V_T is kept constant, I_{Leak} still increases as technology is scaled because of C_{ox} scaling ($C_{ox} = \varepsilon/t_{ox}$,and t_{ox} is scaled with technology [5]). Thus, the total energy consumption will be dominated by leakage current as technology scaling progresses.

A Single Electron transistor (SET) is a transistor in the limit of scaling with a very small feature size, and hence very small self capacitance. Thus, it can be turned on and off using very few electrons, i.e. intrinsically very little charge is necessary to operate the device. Given, the trend that leakage energy dominates the energy consumption of scaled transistors; it is useful to look at the energy-delay tradeoff of an SET device in order to understand what kind of challenges face us in order to reach closer to the theoretical minimum energy limit for switching logic circuits.

The background information and preliminaries pertaining to SETs are presented in Section 2.1. In order to design circuits using SETs, it is necessary to understand the electrostatics and derive analytical expressions for the On/Off currents of the SET, which is done in Sections 2.2 and 2.3. In order to operate SETs at Room Temperature, a SET nanodot has to be dimensionally scaled down; thus, making quantization effects more significant. In Section 2.4, an approximation for including energy quantization into the analytical derivations from Section 2.3 is introduced.

By using the analytical derivations from Section 2, Section 3.1 explores the design space that is available for SET based circuits. Section 3.2 presents a case study of a programmable SET device in order to understand the feasibility of the design space of Section 3.1. Based on the design space described in Section 3.1, circuit design case studies are considered in Section 4, and their Energy-Delay performance characteristics are simulated. Section 5 summarizes the paper and draws

conclusions based on the Energy-Delay performance characteristics obtained in Section 4.

2 ANALYTICAL MODELING

2.1 Background

Classically, a Single Electron Transistor (SET) (Fig 1A) is a Coulomb Blockade device which exhibits current peaks (I_{Peak}) and valleys (I_{Valley}) in the I_D-V_G (Fig 1B), due to the influence of the self-charging Energy E_0 of the device (Given by $E_0 = q^2/C_\Sigma$, where C_Σ is the self-capacitance). In order to realize these Coulomb oscillations, it is necessary for the self charging energy E_0 to be dominant over thermal fluctuations ($E_0 >> k.T$), and it is also required that the tunneling resistance be significantly larger than the quantum of resistance ($R_T >> h/q^2$), in order for quantum fluctuations to be minimal [6]. These two conditions are necessary for charge to be localized on the nanodot when it is in Coulomb blockade mode (i.e. the Off state).

In order to build switching logic circuits using SETs, it is necessary to operate the device within the region of transconductance occurring from I_{Valley} to I_{Peak} (Fig 1B). Thus, it is important to derive analytical expressions for I_{Peak}/I_{Valley} ratio and also for the V_{Gate} swing required to start from I_{Valley} and reach I_{Peak}. Closed form expressions for these quantities help us to understand how these quantities depend on the dimensions and the electrostatics of the device.

2.2 Device Electrostatics

In order to derive the electrostatics, a simple symmetric three terminal SET device shown in Fig 1A is assumed. The coupling capacitance between the gate and the nanodot is C_G, and the coupling capacitances between the source/drain and the nanodot are, C_S and C_D ($C_S = C_D$ due to symmetry assumption). The self capacitance C_Σ of the nanodot is equal to the sum of the various coupling capacitances ($C_\Sigma = C_G+C_D+C_D$). The nanodot is isolated from the source and drain contacts by tunnel barriers with resistance R_T ($> h/q^2$). For subsequent derivations, the source contact of the device in

Fig1A is grounded ($V_{Source} = 0$). When a voltage V_{Drain} (assuming $V_{Gate} = 0$, $V_{Source} = 0$) is applied to the drain contact, the potential of the nandot is increased by a fraction proportional to the coupling capacitance C_D between the drain and the nanodot. This increase in potential is shown (as a decrease in energy) in the energy diagram in Fig 2A. With an applied drain bias of V_{Drain}, the potential of the nanodot when the first peak of the Coulomb oscillations is reached is given by $q/(2.C_\Sigma) + V_{Drain}/2$ as shown by the energy diagram in Fig 2B. Thus, for an applied drain bias of V_{Drain}, the amount of gate voltage that needs to be applied in order to reach the first Coulomb oscillation peak (starting from $V_{Gate} = 0$) can be derived as shown in Eqs. (3)-(5).

By symmetry, $C_D = C_S$ and $C_\Sigma = C_G + 2.C_D$

$$\frac{C_G}{C_\Sigma}.V_{Gate} = \frac{1}{2}.(\frac{q}{C_\Sigma} + V_{Drain}) - \frac{C_{Drain}}{C_\Sigma}.V_{Drain} \quad (3)$$

$$V_{Gate} = (\frac{q}{2.C_\Sigma} + \frac{V_{Drain}}{2} - \frac{C_D}{C_\Sigma}.V_{Drain}).\frac{C_\Sigma}{C_G} \quad (4)$$

$$V_{Gate}(I_{Peak}) = \frac{q}{2.C_G} + \frac{V_{Drain}}{2} \quad (5)$$

As shown in Fig 3, the dot potential changes by q/C_Σ between two consecutive current peaks. Due to the symmetry of the device, the valley occurs between the two peaks. Thus, the nanodot potential at the valley must be $q/(2.C_\Sigma)$ less than the nanodot potential at the first Coulomb peak as shown in Fig 3. In order to reach the first valley (starting from $V_{Gate} = 0$), the gate voltage that needs to be applied can be derived as shown in Eqs. (6)-(9).

$$\frac{C_G}{C_\Sigma}.V_{Gate} = \frac{1}{2}.(\frac{q}{C_\Sigma} + V_{Drain}) - \frac{C_{Drain}}{C_\Sigma}.V_{Drain} - \frac{1}{2}.\frac{q}{C_\Sigma} \quad (6)$$

$$\frac{C_G}{C_\Sigma}.V_{Gate} = \frac{V_{Drain}}{2} - \frac{C_{Drain}}{C_\Sigma}.V_{Drain} \quad (7)$$

$$V_{Gate} = (\frac{V_{Drain}}{2} - \frac{C_D}{C_\Sigma}.V_{Drain}).\frac{C_\Sigma}{C_G} \quad (8)$$

$$V_{Gate}(I_{Valley}) = \frac{V_{Drain}}{2} \quad (9)$$

According to Eq. (5) and Eq. (9), for any V_{Drain}, the amount of gate swing required to start from

I_{Valley}, and reach I_{Peak} is given by $q/(2.C_G)$.

2.3 Analytical Expressions for Peak and Valley Currents

The description of electron currents resulting from single electron tunneling is well understood [6] [7] and is best described as a Stochastic Markov chain process (Fig 4A), where each state indicates the charge state of the device. The master equation (Eq. 10) is used to solve for the occupation probabilities of each state ($P_i(t)$ is the time-dependent probability that the device has charge *i*).

$$\frac{\partial P_i(t)}{\partial t} = \sum_{j \neq i} [\Gamma_{ij} P_j(t) - \Gamma_{ji} P_i(t)] \quad (10)$$

This is the most general description of single electron tunneling and is the model used in SIMON [6], a well known Monte Carlo simulator for SETs. A commonly used approximation though, is to model the process of tunneling as a birth-death process (Fig 4B) where the charge state of the device changes between N and N + 1 electrons only. Analytical expressions for the I_D-V_G curve of an SET device have been derived previously [8] [9] based on the birth-death process model.

Since the aim is to obtain simple expressions for I_{Peak} and I_{Valley}, we start by considering only two states N=0 and N=1, and the tunneling rates between these states ($\Gamma_{0 \rightarrow 1}$ and $\Gamma_{1 \rightarrow 0}$). By solving the Master equation (Eq 10) under this assumption, it is observed that these two tunneling rates cause the first Coulomb oscillation peak for a positive V_{Gate} sweep, as shown in Fig 5A. Also, the tunneling rates between the states N=0 and N= -1 ($\Gamma_{0 \rightarrow -1}$ and $\Gamma_{-1 \rightarrow 0}$) cause the second Coulomb oscillation peak for a negative V_{Gate} sweep. Thus, the tunneling rates contributing to the first valley current are the four tunneling rates ($\Gamma_{0 \rightarrow 1}$/ $\Gamma_{1 \rightarrow 0}$ and $\Gamma_{0 \rightarrow -1}$/ $\Gamma_{-1 \rightarrow 0}$) (Fig 5). Based on the electrostatics derived in Section 2.1, the first valley occurs at $V_{Gate} = V_{Drain}/2$. Thus, an approximation for the contribution of the tunneling rates $\Gamma_{0 \rightarrow 1}$/ $\Gamma_{1 \rightarrow 0}$ to I_{Valley} (at $V_{Gate} = V_{Drain}/2$) can be derived, and I_{Valley} will be twice this value due to an equal contribution (by symmetry) from the tunneling rates $\Gamma_{0 \rightarrow -1}$/ $\Gamma_{-1 \rightarrow 0}$. In the

rest of this subsection, an analytical approximation for I_{Valley} is derived.

At the valley point ($V_{Gate} = V_{Drain}/2$), the Free Energy changes (ΔF) corresponding to the various barrier-tunneling events across the source/nanodot and drain/nanodot tunnel barriers are shown in Eqs. (11)-(14).

$$C_\Sigma = C_G + 2.C_D \ , \ V_{Gate} = \frac{V_{Drain}}{2} \ , \ E_0 = \frac{q^2}{C_\Sigma}$$

$$\Delta F_{Source\rightarrow Dot} = \frac{E_0}{2} - \frac{q}{C_\Sigma}.(C_D V_{Drain} + C_G \frac{V_{Drain}}{2}) = \frac{1}{2}.(E_0 - q.V_{Drain}) \quad (11)$$

$$\Delta F_{Dot\rightarrow Source} = -\frac{1}{2}.(E_0 - q.V_{Drain}) \quad (12)$$

$$\Delta F_{Drain\rightarrow Dot} = \frac{E_0}{2} - \frac{q}{C_\Sigma}.(C_D V_{Drain} + C_G \frac{V_{Drain}}{2}) + q.V_{Drain} = \frac{1}{2}.(E_0 + q.V_{Drain}) \quad (13)$$

$$\Delta F_{Dot\rightarrow Drain} = -\frac{1}{2}.(E_0 + q.V_{Drain}) \quad (14)$$

For reasonably small drain voltages, $\Delta F_{Source\rightarrow Dot} >> kT$ holds true i.e. $E_0 - q.V_{Drain} >> 2.k.T$ holds. Under this assumption, the tunneling rates (Γ) for the barrier tunneling events can be approximated as shown in Eqs. (15)-(18). The tunneling rates (Γ) are computed assuming a constant density of energy states in the contact and the nanodot as described in [6].

$$\Gamma_{\Delta F} = \frac{\Delta F}{q^2.R_T.(e^{\Delta F/k.T} - 1)} \text{ and } E_0 - q.V_{Drain} >> 2.k.T$$

$$\Gamma_{Source\rightarrow Dot} \approx \frac{1}{2.q^2.R_T}.(E_0 - q.V_{Drain}).e^{-(E_0 - q.V_{Drain})/2.k.T} \quad (15)$$

$$\Gamma_{Dot\rightarrow Source} \approx \frac{1}{2.q^2.R_T}.(E_0 - q.V_{Drain}) \quad (16)$$

$$\Gamma_{Drain\rightarrow Dot} \approx \frac{1}{2.q^2.R_T}.(E_0 + q.V_{Drain}).e^{-(E_0 + q.V_{Drain})/2.k.T} \quad (17)$$

$$\Gamma_{Dot\rightarrow Drain} \approx \frac{1}{2.q^2.R_T}.(E_0 + q.V_{Drain}) \quad (18)$$

By this approximation, the occupation probabilities of the nanodot for the charge states N=0 and N=1 can be approximated as shown in Eqs. (19)-(22).

$$\Gamma_{0\rightarrow 1} = \Gamma_{Drain\rightarrow Dot} + \Gamma_{Source\rightarrow Dot} \approx \frac{1}{2.q^2.R_T}.(E_0 - q.V_{Drain}).e^{-(E_0 - q.V_{Drain})/2.k.T} \quad (19)$$

$$\Gamma_{1\rightarrow 0} = \Gamma_{Dot\rightarrow Drain} + \Gamma_{Dot\rightarrow Source} \approx \frac{E_0}{q^2.R_T} \quad (20)$$

$$Pr(0) = \frac{\Gamma_{1\rightarrow 0}}{\Gamma_{1\rightarrow 0} + \Gamma_{0\rightarrow 1}} \approx 1 \quad (21)$$

$$Pr(1) = \frac{\Gamma_{0\rightarrow 1}}{\Gamma_{1\rightarrow 0} + \Gamma_{0\rightarrow 1}} \approx \frac{1}{2.E_0}.(E_0 - q.V_{Drain}).e^{-(E_0 - q.V_{Drain})/2.k.T} \quad (22)$$

Using the approximations for the occupation probabilities Eqs (21)-(22) and considering the tunneling rates across the source-side tunnel barrier ($\Gamma_{Source \rightarrow Dot}$ and $\Gamma_{Dot \rightarrow Source}$), an analytical approximation for I_{Valley} (the expression is multiplied by 2 to account for the contribution of the tunneling rates $\Gamma_{0 \rightarrow -1}$/ $\Gamma_{-1 \rightarrow 0}$) is derived as shown in Eq. (23). Similarly an analytical expression for I_{Peak} is derived shown in Eq. (24).

$$I_{valley} \approx \frac{1}{q.R_T}.\frac{(E_0 - q.V_{Drain})(E_0 + q.V_{Drain})}{2.E_0}.e^{-E_0/2.k.T}.e^{q.V_{Drain}/2.k.T} \quad (23)$$

$$I_{Peak} = \frac{1}{2.R_T}.\frac{V_{Drain}}{2} \quad (24)$$

A comparison of the values for I_{Peak} and I_{Valley} obtained through SIMON and those computed using the analytical approximations Eqs. (23)-(24) is shown in Fig 6, and shows the validity of this approximation. According to Eq. 23, I_{Valley} reduces exponentially as E_0 is increased, which happens as the SET nanodot's physical dimension is scaled down. This clarifies the role that the self-charging energy E_0 plays in the operation of an SET. Assuming that the density of states in the nanodot is continuous, the self-charging energy (E_0) opens up a gap in the energy state distribution of the nanodot (allowing us to turn the device On and Off when $E_0 >> kT$). Thus, I_{Valley} decreases exponentially as the nanodot's dimension is scaled down because this energy separation increases.

2.4 Modeling Quantization

In order to operate SETs at room temperature, the nanodot's dimension needs to be scaled down so that $E_{nanodot} >> k.T_{300}$. However, as the device is scaled down, there is an increase not only in the self-charging energy (E_0) but also in the quantization energy (E_Q). In order to compare E_0 and E_Q as the device dimension is scaled, the nanodot is approximated as a sphere, and as an infinite potential well, as suggested in [10]. Under these assumptions, the self charging energy (E_0) and the quantization energy (E_Q) are modeled by Eqs. (25) and (26).

$$E_0 = \frac{e}{2.\pi.\epsilon_{Si}.d} \qquad \text{where } \epsilon_{Si} = 11.7 \quad (25)$$

$$E_Q = \frac{1}{2.m^*}.(\frac{\hbar.\pi.N}{d})^2 \quad \text{where } m^*_{Si} = 0.26\ ,\ N = 1 \quad (26)$$

Note: Equations 25 and 26 are approximations suggested in [10]

By plotting E_0 and E_Q as functions of the nanodot dimension (Fig 7), the nanodot diameter (d) such that the self-energy of the nanodot ($E_{Self} = E_0 + E_Q$) is large enough for room temperature operation ($E_{Self} >> 8.kT_{300}$), is found to be 3nm and below. At this dimension, the main contributor to E_{Self} is the quantization energy E_Q. Thus, there is a need to take quantization energy (E_Q) into consideration when modeling room temperature SETs.

There have been numerous demonstrations of room temperature operation of SETs, a summary of which is given in [11]. In order to include quantization into the tunneling rate equations, many models have been proposed and validated against experimental data [12] [13]. However, our aim in this paper is to model the dependence of I_{Peak}/I_{Valley} ratio and the peak-to-valley V_{Gate} swing, on the physical dimensions, and the electrostatics of an SET device. By recognizing that the self-charging energy (E_0) opens up a gap in the energy state distribution of the SET nanodot, and the quantization energy (E_Q) adds to this energy gap, Eq. (27) can be used to model I_{Valley} in the quantized case, and Eq. (28) to obtain the $V_{Gate}(I_{Peak})$ in the quantized case.

$$I_{valley} \approx \frac{1}{q.R_T}.\frac{(E_0 + E_Q - q.V_{Drain})(E_0 + E_Q + q.V_{Drain})}{2.(E_0 + E_Q)}.e^{-E_0/2.k.T}.e^{-E_Q/2.k.T}.e^{q.V_{Drain}/2.k.T} \quad (27)$$

$$V_{Gate}(I_{Peak}) = \frac{1}{2}.(E_0 + E_Q).\frac{C_G}{C_\Sigma} + \frac{1}{2}.V_{Drain} \quad (28)$$

The approximation that is used here, is to model an SET with quantized energy levels as a classical SET with an increased energy gap (i.e. effective Coulomb gap = $E_0 + E_Q$). We clarify that our approach is only an approximation, because the rate equations used in Eqs. (15)-(18) are meant for an

SET with a continuous distribution of energy levels in the nanodot, and are not directly applicable for an SET with quantized energy levels (precise tunneling rate equations for discrete energy levels are shown in [12][13]). In order to check the validity of the approximations, the discrete energy-level simulation model in SIMON is used. Discrete energy levels are specified in SIMON at $+E_Q/2$ eV and $-E_Q/2$ eV, where E_Q is the quantization energy for a given dot dimension. SIMON models energy level broadening as a Gaussian function, and hence provides the height (H) and width (W) of broadened energy levels as tunable parameters. For validation of Eq. 27, the energy level broadening is considered to be minimal, and hence set the Width (W) parameter to 1meV. Since the broadening is assumed to be minimal, the peak current is limited mainly by the tunnel barrier resistance, and hence can be considered to be the same as in Eq. 24. The height (H) is set such that the current peak for discrete energy level simulation equals that in Eq. 24. This is reflected in Fig 8A, in which I_{Peak} is the same for the analytical approximation as well as the Monte Carlo simulation.

Fig 8A shows that I_{Valley} estimated using Eq. 27 follows the same trend as I_{Valley} obtained from SIMON, and is off by less than one order of magnitude. Fig 8B shows the Monte Carlo simulation of a 2.5 nm nanodot in the quantized and continuous energy cases. In the case of continuous energy levels, the V_{Gate} sweep between consecutive peaks is given by $E_0.(C_\Sigma/C_G)$, where as in the case of quantized energy levels, the V_{Gate} separation between consecutive peaks is wider due to quantization energy E_Q, and is given by $(E_0 + E_Q).(C_\Sigma/C_G)$. As shown in Fig 8B, the approximation proposed for quantization matches closely with the Monte Carlo simulation for discrete energy levels. Thus, we can state that this approximation for including quantization energy (E_Q) is reasonable.

3 SET DESIGN SPACE EXPLORATION

3.1 Description of SET Design Space

Eq. 27 (I_{Valley} of an SET) and Eq. 28 (V_{Gate} (I_{Peak}) of an SET) enable us to describe a design space

for SET devices, with the device physical dimensions and electrostatic properties as the parameters. This sub-section provides a description of this design space. Based on Eqs. (25)-(26) and Fig. 7, the nanodot diameter should be 3nm or below for room temperature operation. Since Eq. 27 for I_{Valley} is valid only when $E_0 + E_Q - q.V_{Drain} >> k.T$, the nanodot diameter is chosen to be in the range of 1.5nm to 2.5nm for our design space (so that E_0+E_Q is sufficiently large for Eq 27 to hold). Since we are interested in transistor operation in the sub-200 mV range at room temperature, drain voltages up to 200 mV are considered. Using Eq. 27, the I_{Peak}/I_{Valley} ratio can be plotted as a function of the nanodot diameter and the applied drain bias. The surface plot in Fig 9A shows that I_{Peak}/I_{Valley} ratio increases by four orders of magnitude as the nanodot diameter is reduced from 2.5nm to 1.5nm.

$$V_{Gate}(I_{Peak} \rightarrow I_{Valley}) = \frac{1}{2}.(E_0 + E_Q).\frac{C_G}{C_\Sigma} \quad (29)$$

Eq. 28 gives the gate voltage at which the current-peak occurs in the I_D-V_G curve of an SET with energy quantization. Since the current-valley occurs at $V_{Gate} = V_{Drain}/2$, the gate voltage swing for I_{peak}-to-I_{valley} (Eq. 29) is independent of V_{Drain}. This voltage swing is dependent on the nanodot diameter (which determines $E_0 + E_Q$), and the electrical parameter $\mathbf{C_G/C_\Sigma}$ which is called the gate-control ratio. The gate-control ratio is an electrostatic parameter of the SET device which indicates how well the gate controls the potential of the nanodot. The contour plot in Fig 9B shows $V_{Gate}(I_{Peak} \rightarrow I_{Valley})$ as a function of the nanodot diameter and the gate-control ratio. This contour plot shows that this gate voltage swing increases as the nanodot diameter scales down, and worsens when the gate-control ratio is lower.

It is useful from a circuit-design standpoint to combine the plots in Fig. 9A and Fig. 9B to plot the switching slope (SS) characteristic of an SET, as a function of the nanodot diameter and applied drain bias, for different gate-control ratios. Fig 10A shows the SS contours (mV/Dec) for an SET with a

high gate-control ratio (C_G/C_Σ) of **7/10**, as a function of the nanodot diameter (1.5nm to 2.5nm) and applied drain bias (up to 200 mV). Fig 10B shows the same for an SET with a poor gate-control ratio (C_G/C_Σ) of **4/10**. The observation from Fig 10A, is that even though I_{Peak}/I_{Valley} ratio increases as the nanodot diameter scales down, $\Delta V_{Gate}(I_{Valley} \rightarrow I_{Peak})$ also increases, thus keeping the switching slope nearly constant. Since we are interested in transistor operation at 200 mV, from Fig. 10A, it can be observed that the largest nanodot diameter which can operate at V_{Drain} = 200 mV with a SS close to 200 mV/Dec is 2nm (E_0 = 0.123 eV, E_Q = 0.361 eV). SETs with nanodot diameter larger than 2nm have a SS larger than 200 mV due to a degraded I_{Peak}/I_{Valley} ratio. Such an SET (diameter 2nm, gate-control ratio 7/10) can be turned On and Off with a current ratio of 10, by a V_{Gate} swing whose magnitude equals the magnitude of the applied drain bias (200 mV). It is possible to build logic gates with such a device, and an SET with these characteristics is used as a reference device for illustrating SET logic gate operation in Section 4.1.

From Fig 10B, it can be observed that when the gate-control ratio is low, the SS swings for all nanodot diameters at a drain bias of 200 mV are degraded and are in excess of 250 mV, mainly due to the poor control of the gate over the nanodot potential. The consequence of this is that, it is not possible to build logic gates using using SET devices with poor gate-control, because the V_{Gate} swing necessary to turn the devices On and Off is greatly in excess of the applied drain bias (200 mV). Thus, in the case of SETs with poor gate-control, some form of external amplification is necessary to increase the gate swing, in order to drive the next logic stage. Thus, a sense amplifier based circuit design style is necessary which is discussed in Section 4.2.

3.2 SET- Device Design Case Study

The architecture of a programmable SET device with wrap-gate-tunable tunnel barriers was proposed in [14]. Such a device structure has been implemented in TCAD Sentaurus [15] using a

modulation-doped SiGe/Strained-Silicon heterostructure as shown in Fig. 11. Device simulation performed at 4K shows a 2D electron-gas (2DEG) forming in the strained-silicon layer at the bottom as shown in Fig 11. When -230 mV bias is applied on the wrap gate, a depletion layer is formed in the strained-silicon layer as shown in Fig. 12A, which acts as a tunnel barrier. Fig. 12B shows electron tunneling across the depletion tunnel-barrier width when the wrap-gate bias is -230 mV; a current of 0.4 nA flows for the applied drain bias of 1mV at 4K, thus giving the depletion tunnel-barrier resistance to be 1.25 MΩ. As shown in Fig 12A, a nanodot is formed in the 2DEG in the strained-silicon layer, which is isolated from the source/drain contacts by the depletion barriers formed under the wrap-gates. Using AC analysis in Sentaurus, the control-gate/nanodot (C_{CG}) coupling capacitance was found to be 17.3 aF, the wrap-gate/nanodot (C_{WG}) coupling capacitance was found to be 20.7 aF and the drain(source)/nanodot coupling capacitance (C_D/C_S) was found to be 3.7 aF. Based on these parameter estimates, the device is modeled in SIMON and the Coulomb oscillations are obtained as shown in Fig 13 (TCAD Sentaurus has been used to study the electrostatics of the device, but it does not have the appropriate device model to simulate Coulomb oscillations).

Fig. 12C shows that when the wrap-gate bias is -220 mV, a depletion region is not formed under the wrap-gates causing the structure to behave like a conducting wire (i.e. a short). Fig 12D shows that the when the wrap-gate bias is -240 mV, a very large depletion region is formed under the wrap-gates causing the structure to behave like a non-conducting wire (i.e. an open). Thus, using rigorous TCAD simulations, the functionality of a programmable SET device which can behave like an open, a short, or as a Coulomb Blockade device, is illustrated. Furthermore, the C_G/C_Σ (gate-control ratio) for this device structure is 0.4, making it a weak gate-control device. Thus, this design case-study helps us observe that practically realizable SET devices have weak-gate control.

4 CIRCUIT DESIGN

4.1 Logic Gate Operation using SETs

In this sub-section, sub-200 mV digital logic operation at room temperature is illustrated and characterized, using 2nm SETs with different gate-control ratios (as described in Section 3.1). For complementary logic circuit operation, pull-down as well as pull-up devices are required. Because the Fermi level E_F (0 eV) lies in the middle of the energy gap (E_0+E_Q), by symmetry, the SET device (Fig 1A) behaves as a pull-up SET when negative drain and gate biases are applied, such that, its currents are identical to those of a pull-down SET with equal but positive drain and gate biases. It is assumed that, a SET device operating at a certain V_{CC} is V_T-adjusted such that the device operates at the I_{Valley} when V_{Gate} = 0 and V_{Drain} = V_{CC} (this assumption is made so that the SET device operates with the best possible On/Off current ratio when V_{Gate} switches from 0 to V_{CC}). Based on this assumption about the operation of SETs, the I_D-V_G curves of a pull-up SET and a pull-down SET with 2nm nanodot diameter, gate-control ratio (C_G/C_Σ) = 0.7 and operating voltage V_{CC} = 200 mV are shown in Fig 14A. The corresponding I_D-V_D curves for the same are shown in Fig 14 B. The I_D-V_G characteristics for the 2nm SET device, with quantized energy levels, are obtained using the discrete energy level simulation model in SIMON (the conditions used for obtaining these curves are same as those described in Section 2-4). The I_D-V_G characteristics are populated into a look-up-table, and a Verilog-A look-up-table based model is created for the SET device. Circuits are built using instances of the Verilog-A device model, and are simulated using Cadence® Spectre® simulation software.

Assuming that the pull-up and pull-down SET devices operate as described above, the voltage-transfer characteristics (VTC) of an SET inverter with good gate-control (C_G/C_Σ = 0.7) devices can be plotted for different V_{CC} as shown in Fig 15A. Fig 15B shows the VTC of an SET inverter with poor gate control (C_G/C_Σ = 0.4) devices. As described in Section 3.1, SET devices with poor gate-control (C_G/C_Σ = 0.4) have degraded SS, and cannot turn On properly when equal gate and drain voltages are

applied. The consequence of this is clearly visible in Fig. 15B where the inverters have VTC curves with slope < -1 and hence cannot function as logic gates.

A 2-input nand ring oscillator circuit described in [1] is used to compare the ED performance of SET based digital logic with that of 16nm and 22nm (Low V_T) CMOS digital logic at different Activity Factors. The 16nm and 22nm CMOS digital circuits are simulated using predictive BSIM models [16]. For CMOS, the dimensions of the source/drain junction are assumed to be 2.5Lg x W, in order to compute the junction plate and sidewall capacitances for the CMOS transistors. Since the feature size of the SET being considered is 2nm, and since the junctions do not scale accordingly, we nominally use a 10nm x 10nm junction for SETs. Based on the values for junction plate capacitance (CJ = 0.5 milliF/m^2), and the junction sidewall capacitance (CJSW = 0.5 nanoF/m) used in the predictive BSIM models, a junction capacitance of 20aF is obtained for SET devices (the gate capacitance of the SET is ~ 1aF and is ignored in the energy calculation). The ED performance comparison in Fig.16 shows that the energy consumption of the SET digital circuit at high Activity Factor is considerably lower than the energy of the CMOS digital circuits, due to the reduction in load capacitances. However, Fig. 16 shows that at low activity, the energy consumption of the SET digital circuit and the energy of the CMOS digital circuits lie in close proximity, showing the dominance of leakage energy consumption (at low activity factors).

4.2 Sense Amplifier-Based Design using SETs

The use of pass-transistor logic stacks with sense amplifiers was proposed in [17], in order to continue reducing energy when the circuit energy consumption becomes dominated by leakage energy at low supply voltages. Since the energy consumption of complementary digital logic using SETs (at low activity, low V_{CC}) is dominated by leakage energy, a similar approach using sense-amplifiers is considered. Furthermore, from the case-study in Section 3.2, it is difficult to physically realize nanoscale devices with good gate-control, and based on the discussion in Section 3.1, SET devices

with poor gate-control require external amplification in order to produce a V_{Gate} swing necessary to drive the next logic stage; thus, giving another reason to consider a sense amplifier-based circuit design for SETs. In this section, we propose using SETs (i.e. poor gate–control devices) to implement the Binary Decision Diagrams (BDDs) of logic functions, followed by a differential CMOS sense amplifier in order to reduce leakage and perform amplification to drive the next logic level. Similar to the concept in [17], the BDD logic stack does not consume any leakage energy during switching, since there are no paths to ground in it. The schematics of an 8-input XOR gate (which is a low activity logic) using CMOS gates, and using BDD-logic with sense amplifier (similar to Xor circuit in [18]) are shown in Fig 17. The sense amplifier used for sensing the differential output of the BDD stack is a current-controlled latch sense amplifier described originally in [19], and is implemented using 16nm (Low V_T) CMOS. The root of the BDD stack is driven with a supply voltage ranging from 125-to-275 mV, and the sense amplifier is driven with a constant supply voltage of 300mV. The output of the sense amplifier is in the voltage range of 0-to-300mV, and is used to drive the next logic stage. Fig 18 shows the ED performance of the 8-input Xor logic gate implemented using CMOS gates, and BDD-logic with sense amplifier. From Fig 18, it is clear that the CMOS logic gates become leakage energy dominated at low V_{CC}, and BDD-logic with sense amplifier helps to continue reducing energy even at low V_{CC}. However, it is also clear that the amount of energy reduction obtained using the sense amplifier-based technique diminishes with technology scaling. The Minimum Energy of 8-input Xor BDD-logic (with sense amplifier) is, 96 aJ for 22nm CMOS, 79 aJ for 16nm CMOS, and 76 aJ for 2 nm SET (weak gate control devices + 16nm CMOS sense amplifier). The reason for this diminished energy reduction is that, the energy consumption is dominated by the leakage energy of the sense amplifier as illustrated in Fig 18.

5 CONCLUSION

In this paper, the challenge of energy-reduction in the context of technology scaling is explored, using Single Electron Transistors as a case study. Analytical equations for the electrostatics and the peak/valley currents of SETs (as well as an approximation for including quantization energy) are derived. A design space for room temperature operation of SETs, based on the physical dimensions and the electrostatic properties of the device is described. By studying this design space, SETs can be classified as those with good electrostatic gate-control (which are suitable for complementary logic gate design), and those with weak electrostatic gate-control (which require a sense amplifier-based design). A comparison of the ED performance of a benchmark 2-input nand ring oscillator circuit, implemented using 22nm/16nm CMOS, and SET devices with good gate-electrostatics, is presented. For the SET implementation of this circuit, there is no reduction in energy at low activity and low V_{CC}, due to leakage energy dominance. Hence, complementary-logic gate circuits may not be suitable for energy reduction as technology scaling continues. In order to reduce leakage, and also to provide the necessary sense-amplification for SETs with weak gate-electrostatics, we propose using SETs to implement the BDDs of logic functions. The outputs of the BDD-logic stacks are used to drive differential sense-amplifiers which produce the gate-voltage swing necessary to drive the next stage of logic. Though, a similar technique has been used to achieve energy reduction at low V_{CC} for 90nm CMOS [17], we observe that the energy reduction through this technique is diminished in the nanoscale (22nm/16nm CMOS and 2nm SET) due to dominance of the energy consumption of the sense-amplifier. Thus, there is a need for design and exploration of low energy consumption sense amplifiers in order to continue energy reduction with technology scaling. Coupled with energy-efficient sense amplifiers, SET based BDD-Logic circuits are capable of continuing the drive towards lower switching energy.

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FIGURES AND TABLES

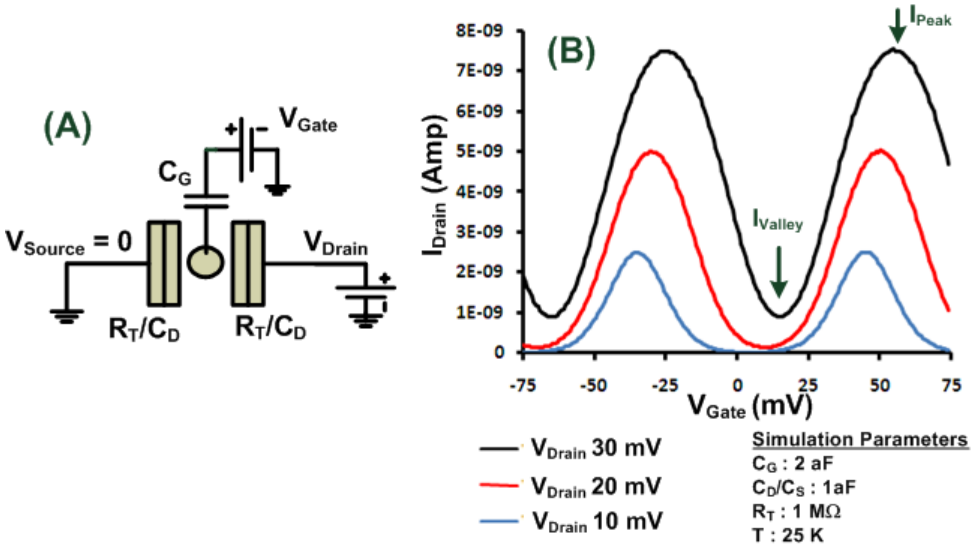

Figure 1: (A) Schematic of a symmetric Single Electron Transistor. (B) Coulomb oscillations (Peaks and Valleys) obtained using the Monte Carlo simulator SIMON.

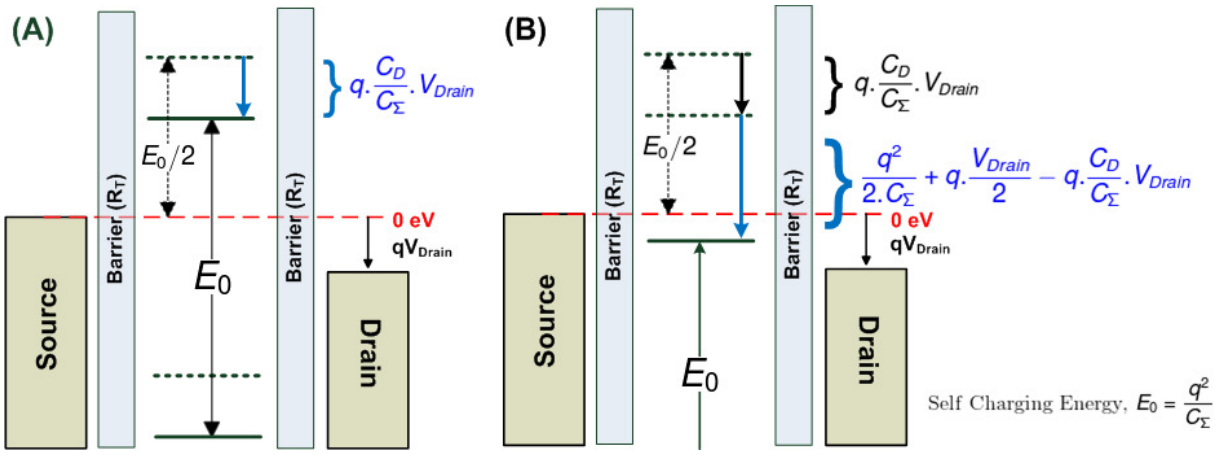

Figure 2: (A) Effect of V_{Drain} bias on SET nanodot potential. (B) Energy diagram of the SET nanodot at the peak of Coulomb oscillation.

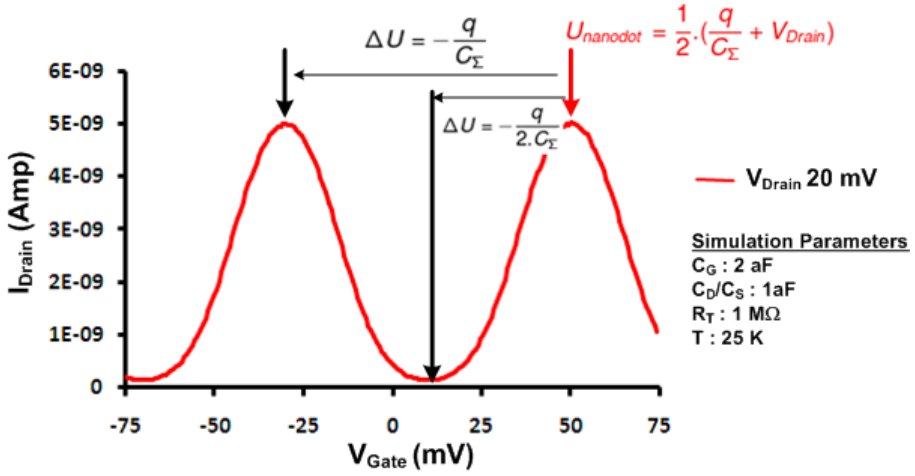

Figure 3: Electrostatic potential of the nanodot at I_{Valley} as a function of total self capacitance and drain bias.

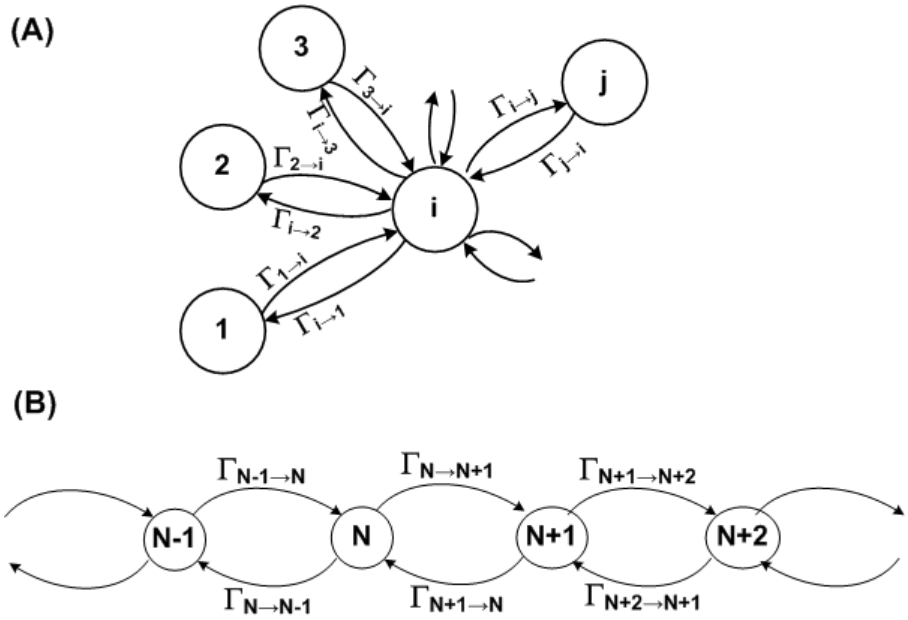

Figure 4: (A) Description of single electron tunneling as a Stochastic Markov chain process. (B) Single electron tunneling as a birth-death process.

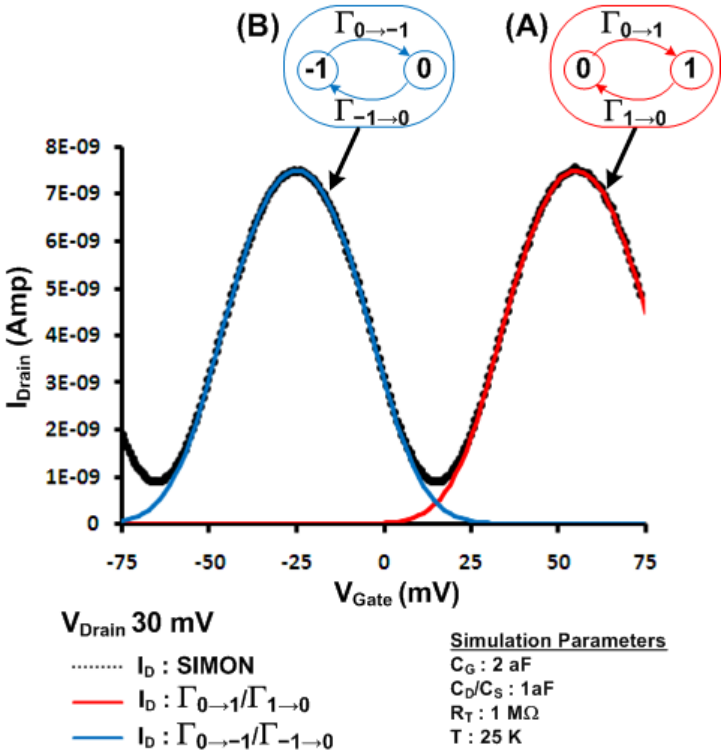

Figure 5: Contribution of various tunneling rates to Coulomb oscillation peaks

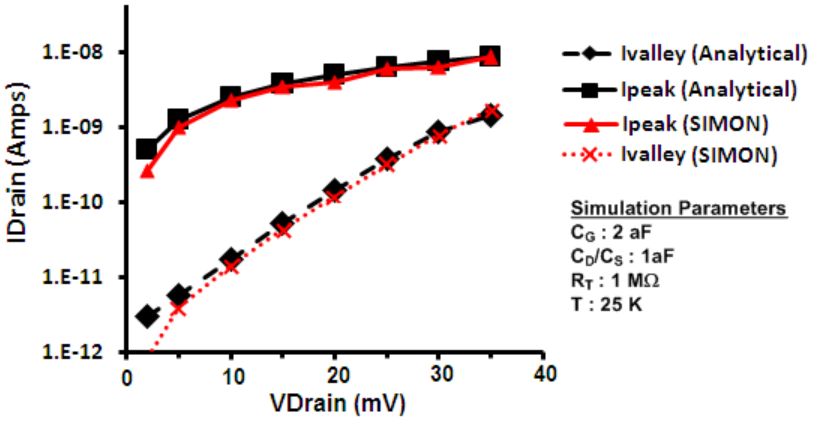

Figure 6: Comparison of I_{Peak} and I_{Valley} obtained through Monte Carlo simulation and physics based approximate analytical calculation.

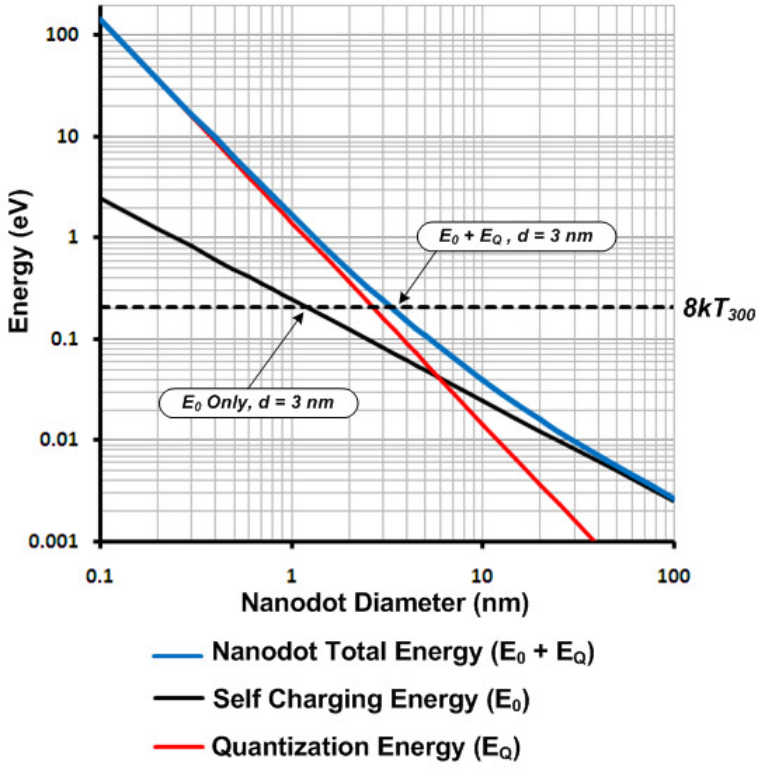

Figure 7: Comparison of self charging energy, E_0, and quantization energy, E_Q, as function of nanodot diameter.

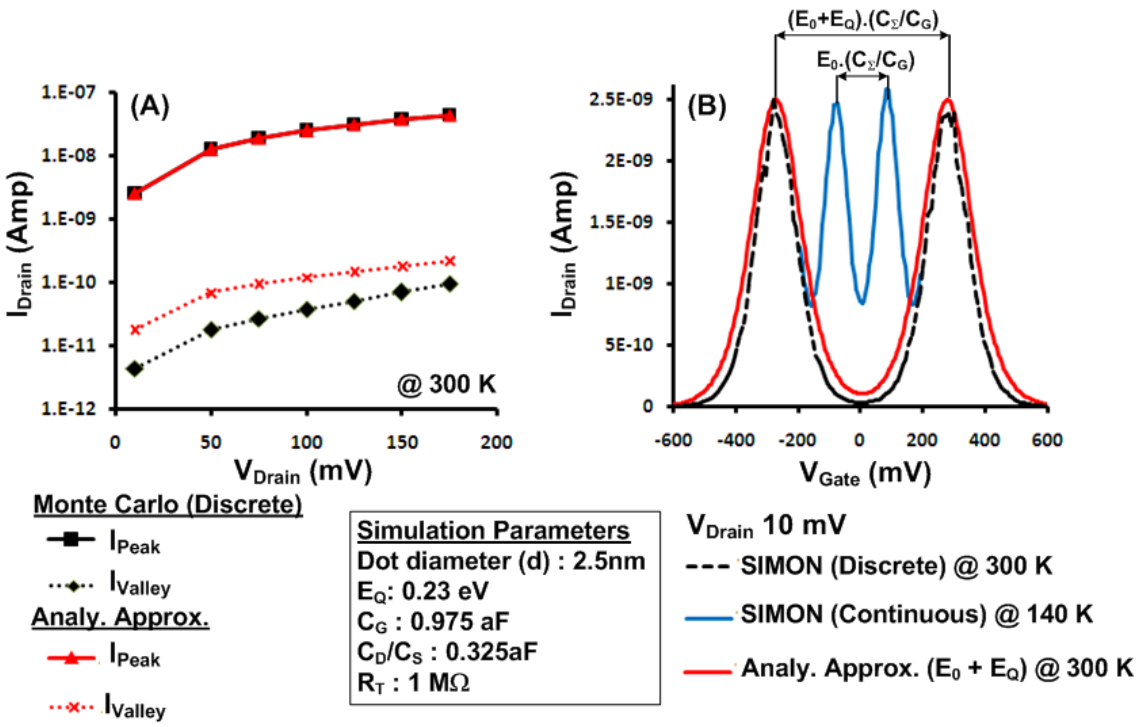

Figure 8: (A) Comparison of I_{Peak} and I_{Valley} obtained through analytical calculation and Monte Carlo simulation. (B) Comparison of analytical calculation with Monte Carlo simulations in the discrete and continuous case.

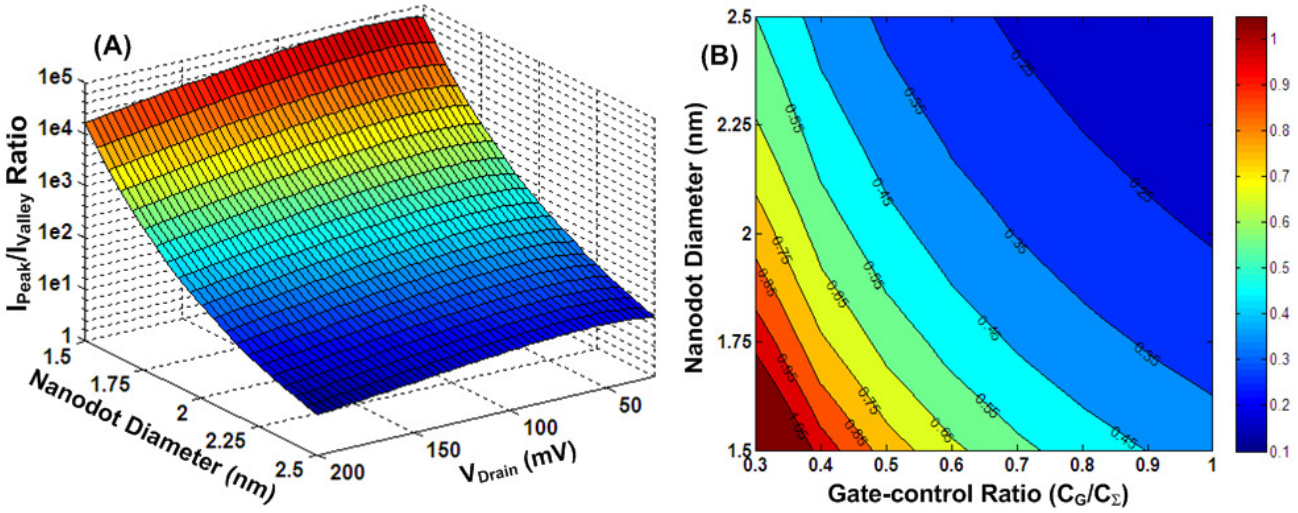

Figure 9: (A) Surface plot of I_{Peak}/I_{Valley} ratio as a function of nanodot dimension and applied drain bias. (B) Contour plot of $\Delta V_{Gate}(I_{Valley} \rightarrow I_{Peak})$ as a function of nanodot diameter and gate-control ratio.

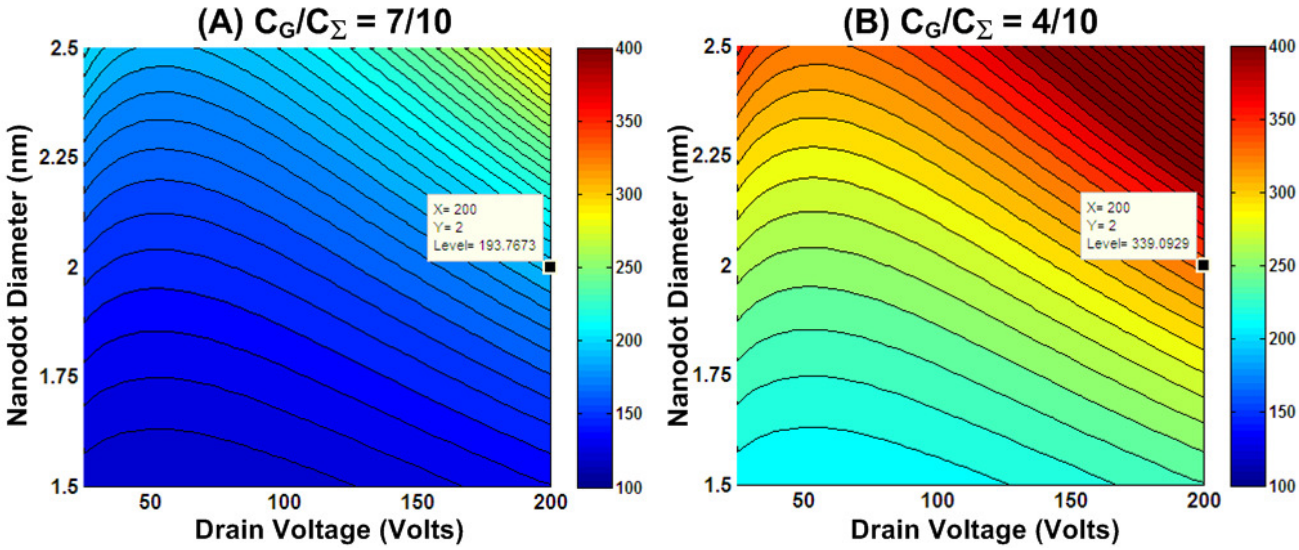

Figure 10: Switching Slope (SS) ($\Delta V_G/\Delta Log(I)$) contour plots as a function of nanodot dimension and applied drain bias for (A) gate-control ratio 0.7 and (B) gate-control ratio 0.4

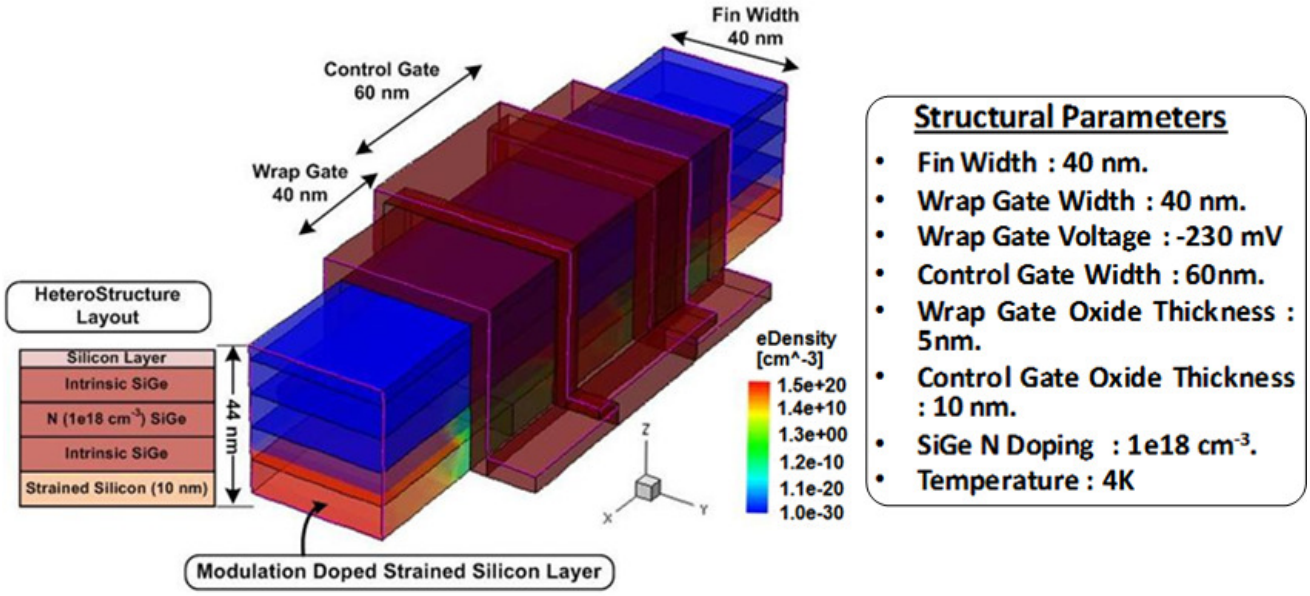

Figure 11: Structural definition of a programmable SET device with wrap-gate tunable tunnel barriers, in TCAD Sentaurus.

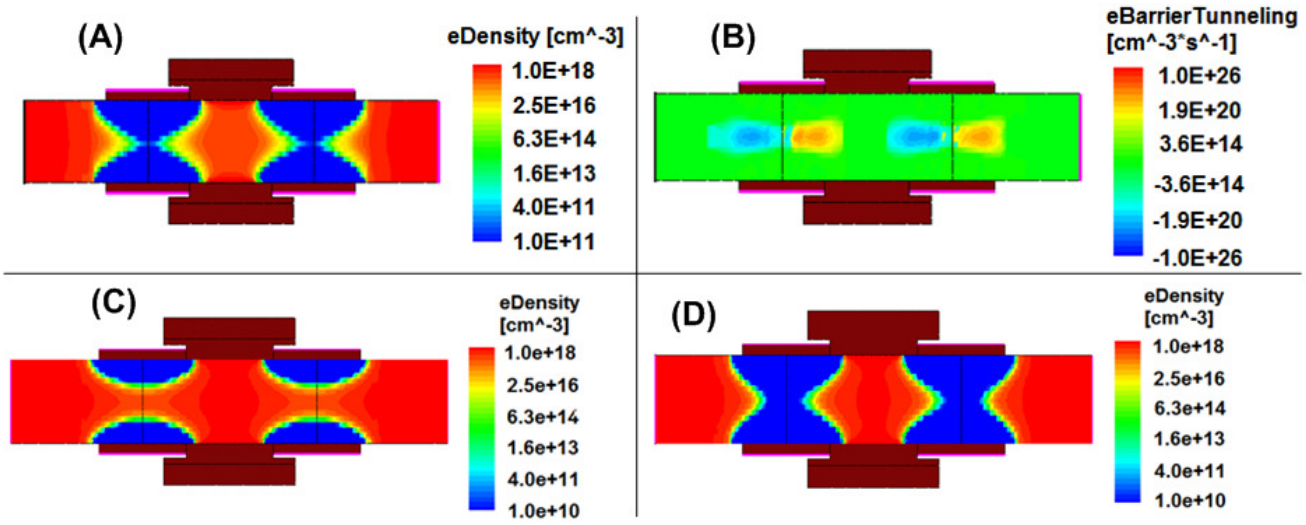

Figure 12: Functional simulation of a programmable SET device. (A) Device operation in Coulomb Blockade (with 1MΩ depletion tunnel-barrier resistance) at $V_{WrapGate}$ -230 mV. (B) Electron tunneling across depletion barrier at $V_{WrapGate}$ -230 mV (C) Device operation as an Open at $V_{WrapGate}$ -220 mV (D) Device operation as a Short at $V_{WrapGate}$ -240 mV.

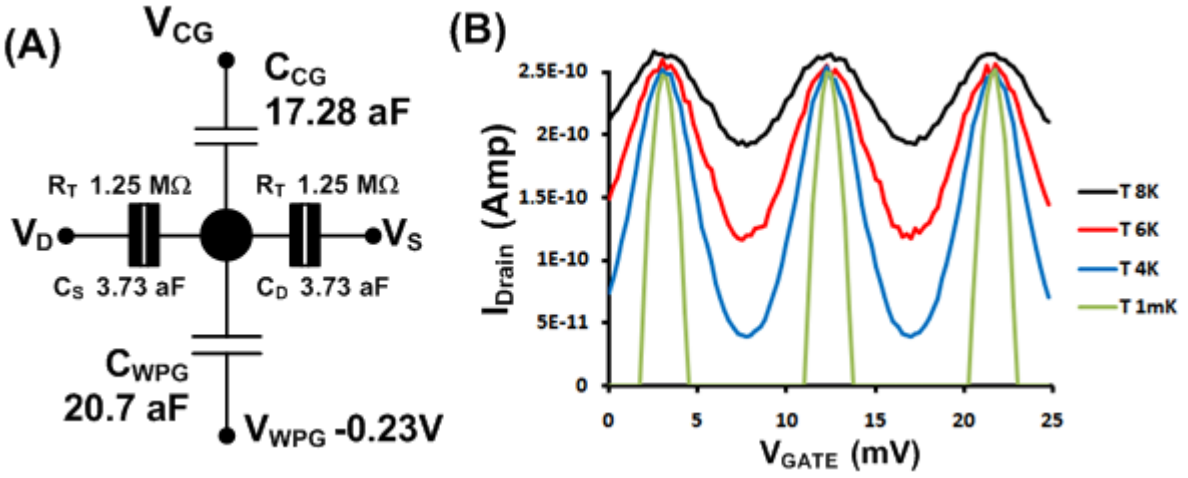

Figure 13: (A) Model of the programmable SET as a Coulomb Blockade device ($V_{WrapGate}$ = -230mV) (B) Coulomb oscillations of the programmable SET device using Monte Carlo simulation.

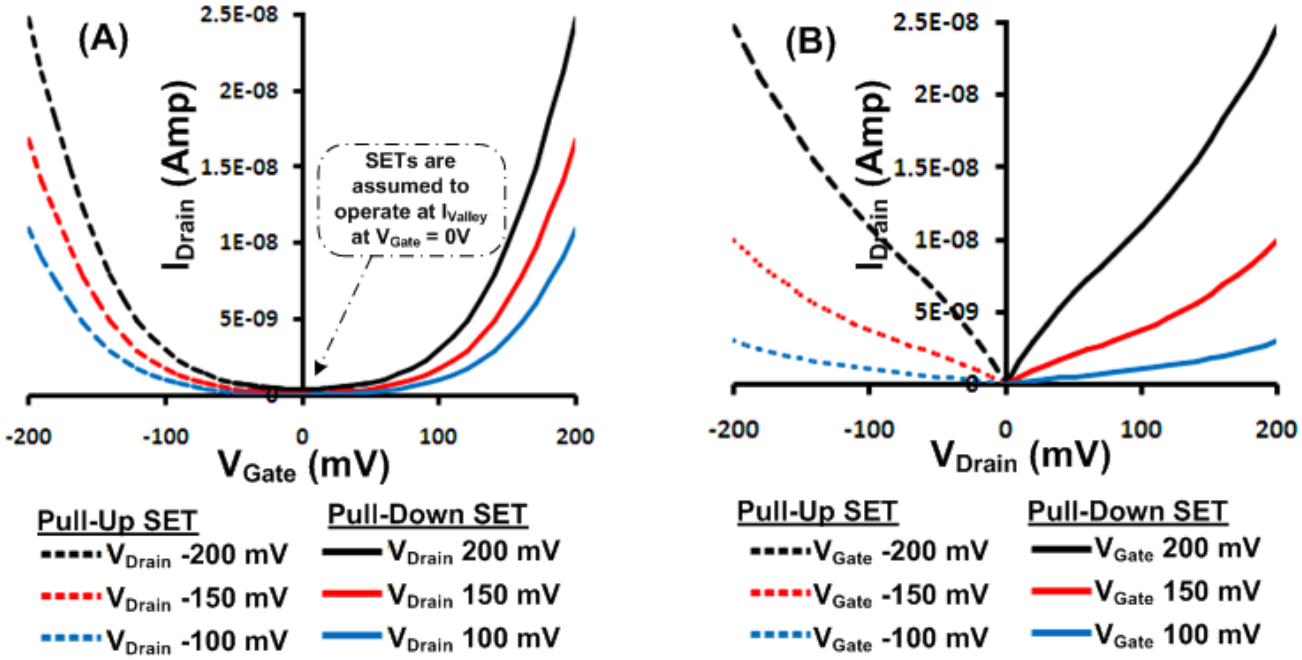

Figure 14: (A) I_D-V_G for Pull-Up and Pull-Down SETs at V_{CC} 200mV assuming that the SETs operate at I_{Valley} when V_{Drain} = 200mV and V_{Gate}=0V. (B) I_D-V_D for the Pull-Up and Pull-Down SETs assuming the same operating condition.

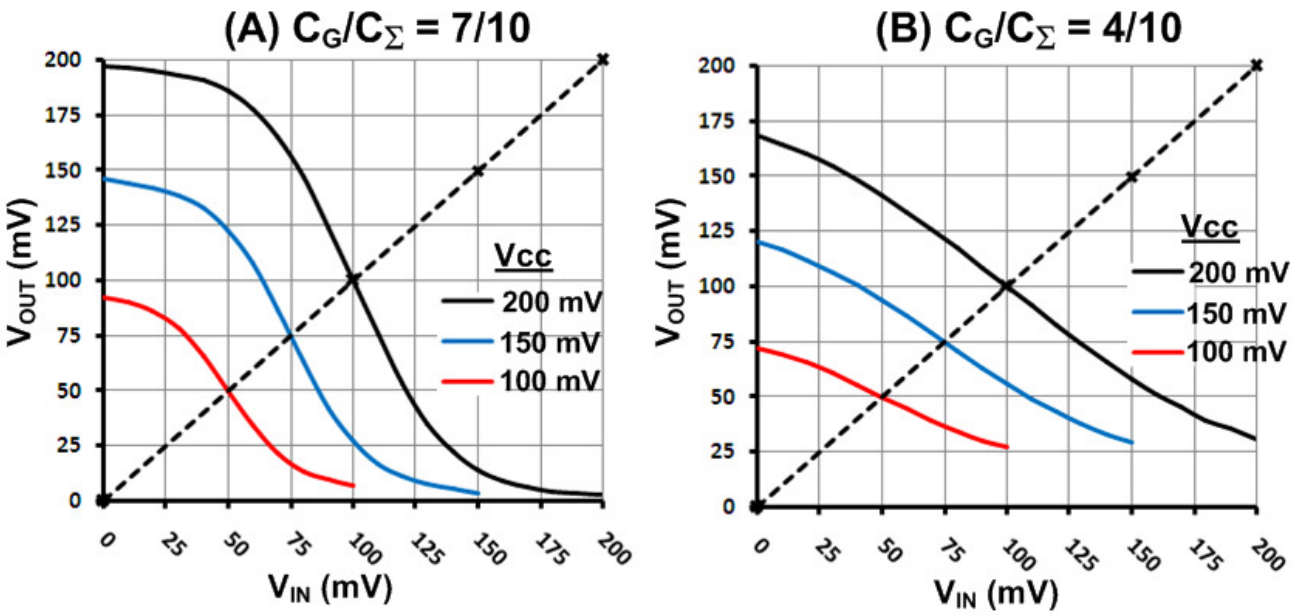

Figure 15: SET inverter voltage transfer characteristics (VTC) for (A) gate-control ratio 0.7 and (B) gate-control ratio 0.4

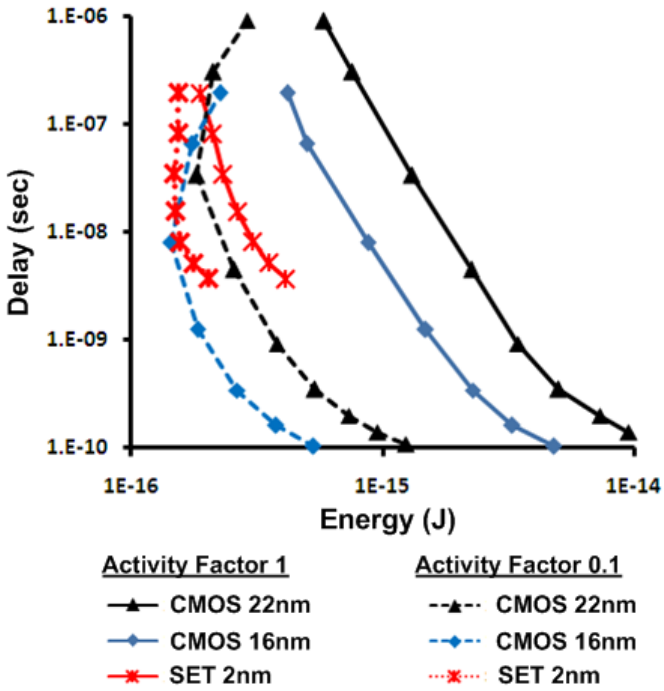

Figure 16: 2-input nand ring oscillator Energy Delay performance for different activity factors.

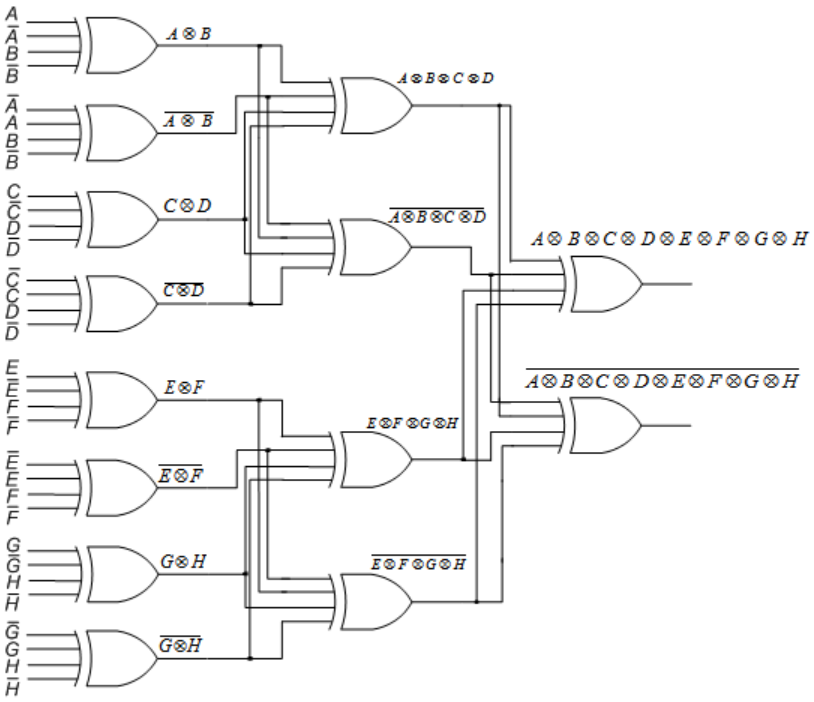

Fig 17 A: Complementary logic gate implementation of 8-input Xor logic

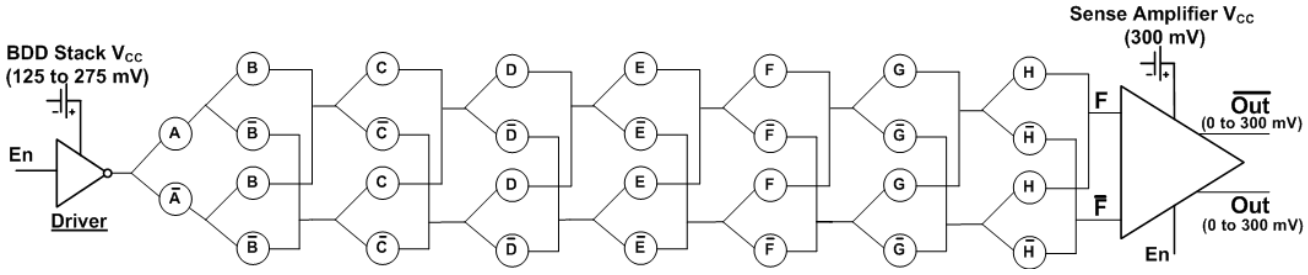

Fig 17 B: Sense-Amplifier and BDD logic stack implementation of 8-input Xor logic

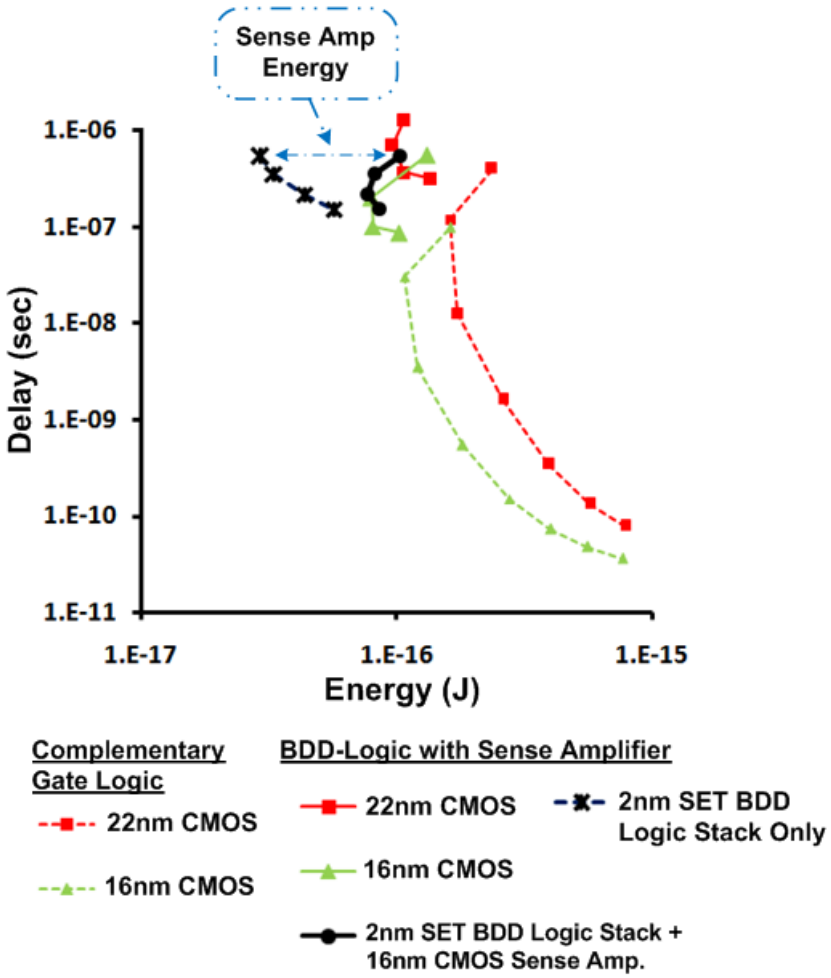

Figure 18: Energy delay performance of 8-input Xor logic using complementary gate logic and BDD-logic with sense amplifier.

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