Temperature-Dependent I–V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET

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***Abstract*—We report on the experimental temperature-dependent characteristics of vertical $In_{0.53}Ga_{0.47}As$ tunnel field-effect transistors (TFETs) at low drain bias to provide key insight into its device operation and design. Leakage floor (I_{OFF}) is determined by the ungated p^+-i-n^+ reverse bias leakage and is dominated by Shockley–Read–Hall generation–recombination current. The temperature dependence of subthreshold slope arises from tunneling into mid-gap states at the oxide–semiconductor interface, followed by thermal emission into the conduction band. At intermediate gate voltages, pure band-to-band tunneling dominates, while at higher gate voltages, current transport is diffusion limited. The temperature-dependent study of $In_{0.53}Ga_{0.47}As$ TFET highlights the importance of passivating the III–V and dielectric interface.**

***Index Terms*—InGaAs, temperature, traps, tunnel field-effect transistors (TFETs), vertical.**

I. Introduction

TUNNEL field-effect transistors (TFETs) with a gate-modulated Zener tunnel junction at the source have recently attracted a great deal of interest for high-performance logic applications [1]–[3] because they allow sub- kT/q subthreshold slope (SS) device operation over a certain gate bias range near the OFF state. TFETs, in principle, can achieve much higher $I_{ON} - I_{OFF}$ ratio over a specified gate voltage swing compared to MOSFETs whose SS is limited to kT/q. This enables aggressive supply voltage scaling for low-power logic operation without impacting its ON–OFF current ratio.

There have been recent studies in understanding the temperature dependence of SS and ON current of TFETs [5], [6]. In this letter, for the first time, we report on the experimentally measured temperature-dependent characteristics of a 100-nm-channel-length sidewall-gated $In_{0.53}Ga_{0.47}As$ vertical TFET [7]. We identify four distinct transport mechanisms at play in $In_{0.53}Ga_{0.47}As$ TFETs to explain the temperature dependence of their transfer characteristics.

Manuscript received January 27, 2010; revised March 3, 2010. Date of publication April 19, 2010; date of current version May 26, 2010. This work was supported in part by the Nanoelectronics Research Initiative through the Midwest Institute for Nanoelectronics Discovery. The review of this letter was arranged by Editor G. Meneghesso.

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Digital Object Identifier 10.1109/LED.2010.2045631

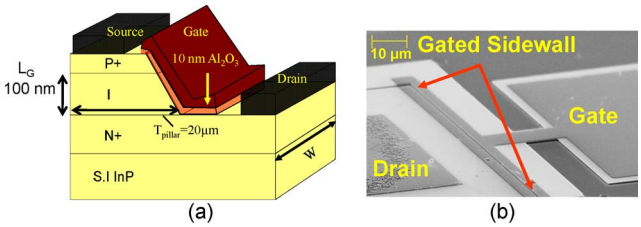

Fig. 1. (a) Cross-sectional schematic of the fabricated vertical $In_{0.53}Ga_{0.47}As$ TFET along with the important process steps. (b) Tilted-view SEM image of fabricated device, showing the gate air-bridge structure used to gate the mesa sidewall. 1) MBE grown P^+-I-N^+ epitaxial structure. 2) Surface Cleaning. 3) Source metallization (Ti/Pt/Au) and citric acid based mesa etch. 4) Native oxide removal and 10 nm ALD Al_2O_3 at 300 C. 5) Gate metallization (Pt/Au) and Al_2O_3 etch from S/D regions. 6) Drain metallization (Ti/Pt/Au) and Isolation.

Section II describes the fabricated vertical device architecture; Section III explains the temperature-dependent transfer and output characteristics, followed by conclusions in Section IV.

II. Fabricated Device Structure

Fig. 1 shows a schematic of the fabricated vertical TFET along with its tilted-view SEM image. The device is fabricated on a molecular beam epitaxy (MBE)-grown p^+-i-n^+ epitaxial layer structure which is patterned into a vertical mesa structure and subsequently gated on its sidewall by atomic layer deposition (ALD) high-k dielectric (Al_2O_3) and metal gate stack. A vertical device architecture using MBE-grown epitaxial layers results in *in situ* doped highly abrupt tunnel junctions, a key requirement for high-performance TFETs. The p^+ source layer is 60 nm thick with a doping of $1 \times 10^{20}/cm^3$; the I-region, which is intrinsically doped and 100 nm thick, sets the channel length; and the n^+ drain region has a doping of $5 \times 10^{19}/cm^3$. The source and drain contacts consist of a Ti/Pt/Au (20/30/100 nm) metal stack deposited by e-beam evaporation and a liftoff process. A 10-nm-thick film of alumina (Al_2O_3) deposited via ALD at 300 °C conformally coats the mesa sidewall to form the gate dielectric. The next section discusses the temperature-dependent characteristics of this vertical $In_{0.53}Ga_{0.47}As$ TFET.

III. Temperature-Dependent Characteristics

Fig. 2(a) shows the output characteristics (I_D–V_{DS}) of the fabricated TFET for temperatures ranging from 150 to 300 K at gate voltage $V_{GS} = 2$ V. Gate-modulated negative

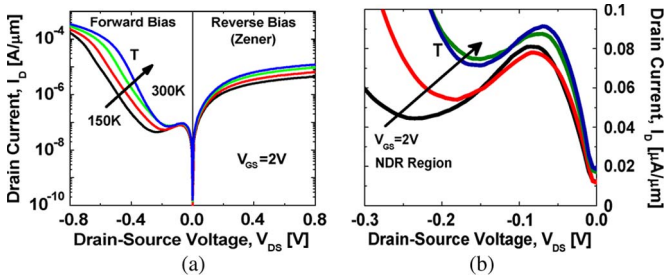

Fig. 2. (a) Output characteristics (I_D–V_{DS}) of the fabricated vertical $In_{0.53}Ga_{0.47}As$ TFET at $V_{GS} = 2$ V for temperatures ranging from 150 to 300 K in steps of 50 K. (b) Temperature dependence of NDR region in the forward-bias region.

differential resistance (NDR) characteristics are visible in the forward-bias regime (negative drain-to-source voltages), followed by regular diode turn-on at more negative drain-to-source voltages. In the NDR region, the conduction occurs at the oxide–semiconductor interface via direct band-to-band tunneling (BTBT) from the conduction band in the channel to the valence band in the p^+ source region. While the BTBT current in the pre-NDR region shows very little temperature dependence, the valley current [Fig. 2(b)] or the excess current is sensitive to the temperature, increasing with rise in temperature and suppressing the peak-to-valley current ratio. A maximum peak-to-valley ratio of two is obtained at 150 K, which progressively degrades at higher temperatures. The origin of excess current is attributed to trap-assisted tunneling at the oxide–semiconductor interface [8]. The diode turn-on at higher negative drain-to-source voltage shows a strong temperature dependence, as expected for thermionic emission over the barrier. In the positive drain-to-source voltage region, the transport is related to reverse-biased BTBT, and the temperature dependence of drain current arises due to bandgap reduction with rising temperature. Fig. 3(a) shows the measured transfer characteristics (I_D–V_{GS}) of the vertical $In_{0.53}Ga_{0.47}As$ TFET for temperatures ranging from 150 to 300 K at $V_{DS} = 50$ mV. The temperature dependence of the transfer characteristics is a strong function of the gate bias, indicating onset of various conduction mechanisms. Based on a 2-D numerical simulation with drift–diffusion transport, a nonlocal tunneling model [2]–[4], and physics-based analytical modeling, we identify four distinct regions of operation in the TFET transfer characteristics, as shown in Fig. 3(a).

In region I, the drain current is constant and shows no modulation with gate voltage. It sets the leakage floor (I_{OFF}) of the TFET. I_{OFF} increases exponentially with rising temperature and is determined by the Shockley–Read–Hall (SRH) generation–recombination current of the reverse-biased p^+-i-n^+ diode. The main contribution to the temperature dependence of this SRH-dominated leakage floor arises from the intrinsic carrier concentration n_i which is proportional to $\exp(-E_g/2\,\mathrm{kT})$, where E_g is the bandgap, k is the Boltzmann constant, and T is the temperature. This is confirmed from the Arrhenius plot in Fig. 4(a), where an activation energy of 0.36 eV is extracted down to 200 K, which is consistent with half the bandgap of $In_{0.53}Ga_{0.47}As$. Below 200 K, the current is higher than that predicted by SRH and originates from the background thermal radiation effect [9]. The off current I_{OFF} is

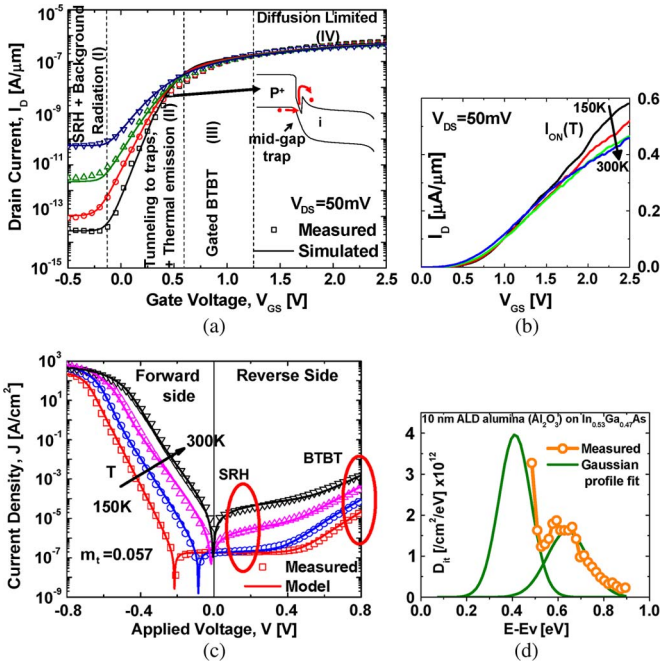

Fig. 3. (a) Transfer (I_D–V_{GS}) characteristics of the fabricated TFET, showing four regions with uniquely different temperature dependences in the range of 150–300 K. Each region identifies a distinct temperature-dependent transport process. (b) Transfer characteristics in linear scale, showing the reduction in ON current with rising temperature in region IV. (c) Ungated $In_{0.53}Ga_{0.47}As$ p^+-i-n^+ diode I–V characteristics. (d) Extracted interface-state-density profile from n-type $In_{0.53}Ga_{0.47}As$ MOSFET using split CV measurement.

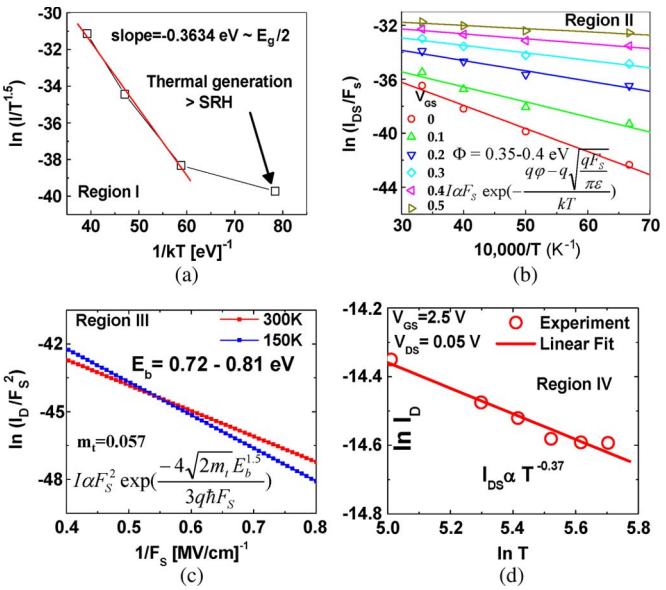

Fig. 4. (a) Activation energy of $E_g/2$ extracted from region I confirms SRH generation–recombination current. (b) PF barrier height extracted from region II highlights a dominant mid-gap trap. (c) Direct BTBT barrier height that is equal to the bandgap in region III indicates negligible contribution from traps. (d) In region IV, the ON current exhibits negative temperature dependence ($\sim T^{-0.37}$), indicating a carrier-diffusion-limited transport in the channel.

proportional to the bulk p^+-i-n^+ mesa area, and hence, the mesa area needs to be minimized to reduce the leakage floor in future ultrathin-body TFETs. In region II, the drain current increases exponentially with gate voltage and represents the subthreshold region of the transfer characteristics. The average SS is not

sub-kT/q or sub-60 mV/dec and progressively degrades from 100 mV/dec at 150 K to 216 mV/dec at 300 K. This strong positive temperature coefficient cannot be explained from the temperature dependence of the bandgap alone and warrants a more careful investigation. We modeled the transport in this regime as a Poole–Frenkel (PF) mechanism [10, p. 403] which involves field-enhanced thermal excitation of carriers from the trap states located within the bandgap into the conduction band. Assuming a PF transport mechanism, Fig. 4(b) extracts an effective thermal barrier height for trapped carriers, which turns out to be located at 0.4 eV from the conduction band edge within the bandgap of $In_{0.53}Ga_{0.47}As$. For numerical simulation purposes, this is approximated as a potential well of depth 0.4 eV immediately adjacent to the p^+ $In_{0.53}Ga_{0.47}As$ source region, as shown in the inset of Fig. 3(a). This notch in the conduction band edge profile is used to artificially simulate the effect of carriers tunneling into mid-gap trap states from the p^+ $In_{0.53}Ga_{0.47}As$ source region and their subsequent thermal emission into the conduction band and is found to explain the experimental data quite well [Fig. 3(a)] at all temperatures. Thus, the physical transport mechanism in the subthreshold region can be understood as tunneling of carriers from the valence band in the p^+ source region to mid-gap traps and a subsequent thermal emission into the conduction band. It is this inherent thermal emission process that gives rise to the strong temperature dependence and dilution in SS.

To understand the origin and location (bulk versus surface) of these mid-gap traps, we fabricated and characterized ungated bulk p^+-i-n^+ diode and n-type MOSFETs on $In_{0.53}Ga_{0.47}As$ with 10-nm Al_2O_3 as the gate dielectric. The reverse-biased bulk p^+-i-n^+ diode characteristics shown in Fig. 3(c) could be explained by SRH generation–recombination currents at low voltages and BTBT at higher voltages with negligible contribution from mid-gap traps. On the other hand, the interface state density extracted from the admittance data obtained using split CV measurements and shown in Fig. 3(d) clearly indicates a large interface state density peaking near the middle of the bandgap. This confirms the participation of mid-gap traps at the oxide–semiconductor interface in the tunneling process, causing dilution in the SS and its strong temperature dependence. An improved surface passivation chemistry suppressing these dominant mid-gap traps will improve SS in future TFETs. In region III, the temperature sensitivity of the drain current is weak, indicating the presence of direct BTBT current. Fig. 4(c) shows an effective tunneling barrier height using Kane's direct BTBT model [10, p. 403]. The barrier height E_b varies from 0.81 eV at 150 K to 0.72 eV at 300 K, which directly corresponds to the temperature variation of the $In_{0.53}Ga_{0.47}As$ bandgap [11]. Here, the junction electric field F_s is extracted from the 2-D numerical simulation of TFETs. In region IV, the TFET drain current dependence on temperature changes sign [Fig. 3(b)]. Fig. 4(d) shows the drain current I_D for different temperatures (T), showing a $T^{-0.37}$ dependence. Numerical simulation indicates that the lateral electric field in the TFET channel is very small, causing the BTBT-generated carriers near the source to primarily diffuse through the channel toward the drain. This diffusion current can be expressed as $(kT/q) \times \mu \times dn/dx$, where μ is the electron mobility in the $In_{0.53}Ga_{0.47}As$ channel with a temperature (T) dependence of $T^{-1.5}$ due to LO phonon scattering and dn/dx is the carrier concentration gradient in the channel. Thus, the experimentally observed temperature dependence of $T^{-0.37}$ is close to the expected value of $T^{-0.5}$.

IV. Conclusions

In summary, we have presented the temperature-dependent characteristics of a 100-nm-channel-length vertical $In_{0.53}Ga_{0.47}As$ TFET. Based on different types of temperature dependence, the transfer characteristic was partitioned into four distinct regions: 1) leakage floor is determined by SRH generation–recombination current; 2) a strong temperature-dependent subthreshold region is dominated by mid-gap trap-assisted tunneling and thermal emission; 3) an intermediate gate bias region, where direct BTBT dominates transport; and d) finally, high-gate-bias region characterized by carrier-diffusion-dominated transport. The $In_{0.53}Ga_{0.47}As$ TFET transfer characteristic and leakage floor can be improved with a robust surface passivation chemistry reducing the mid-gap traps, by minimizing the ungated p^+-i-n^+ diode mesa area and by scaling of the gate dielectric.

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