Non-Silicon Logic Elements on Silicon for Extreme Voltage Scaling

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Abstract

Continued miniaturization of transistors has resulted in unprecedented increase in device count leading to high compute capability albeit with increase in energy consumption. Here, we present our research on advanced non silicon electronic material systems and novel device architectures – quantum-well FETs, inter-band tunnel FETs and tunnel-coupled nanodot devices - for heterogeneous integration on Si substrate. The goal is to demonstrate a compelling information processing platform that allows very aggressive scaling of supply voltage, thereby reducing energy consumption in future computing systems.

Introduction

More than 40 years later, Moore's Law is alive and well with transistor count in integrated circuits doubling every eighteen months. Today, the transistor physical gate length is less than 35 nm; further scaling of conventional silicon devices faces fundamental challenges like gate leakage, channel mobility degradation, exponentially increasing source to drain leakage, rising switching power dissipation from non scaled supply voltages, high source-drain external resistance from arising from scaled contact areas. The industry has already addressed many of these challenges by modifying the silicon transistor though innovations such as highly strained-Si channels for electron and hole mobility enhancement, high-κ/metal-gate stacks for higher drive current and lower gate leakage, the non-planar multiple-gate CMOS transistor architecture (Tri-Gate transistors) to mitigate short channel effects. In the research labs, the focus has now shifted to developing heterogeneous systems that will complement silicon–based digital CMOS with new nanoscale device architectures harnessing quantum mechanical effects, novel materials and, possibly, even entirely new classes of information processing systems. Our ongoing device research entails three novel device configurations such as the quantum-well FETs, the inter-band tunnel FETs and the coupled nanodot devices with a goal towards extreme supply voltage scaling to hundred millivolt (Fig.1).

Quantum-Well Transistors

While silicon based CMOS transistors will continue to be the workhorse of high performance VLSI digital electronics, there have been significant research breakthroughs in the demonstration of quantum-well field effect transistors (QWFETs) using ultra high mobility compound semiconductors such as InGaAs (indium gallium arsenide), InAs (indium arsenide) and InSb (indium antimonide) [1,2]. The quantum-well transistor architecture differs from the conventional surface channel silicon MOSFETs in several ways: (a) remote doped strained quantum-well is used to lower impurity scattering, modify band structure and enhance both electron and hole mobility (b) high dielectric is used to reduce gate leakage (c) self aligned contacts directly contact the quantum-well reducing the access resistance (d) implant-less architecture reduces stochastic fluctuation effects allowing aggressive Vcc scaling. Fig. 2a shows the cross-section schematic of a generic enhancement mode (i.e. normally OFF) quantum well transistor on silicon substrate. High mobility $In_{0.7}Ga_{0.3}As$ epitaxial QW transistor structures have been grown on 4 degrees off-axis (100) p-type Si substrates using metamorphic GaAs and $In_xAl_{1-x}As$ buffer layers grown using solid source molecular beam epitaxy (MBE) [2]. The significance of using wide band-gap materials for the buffer layers is to reduce the residual carrier concentration, provide high resistivity buffer for device isolation, and reduce junction leakage. The metamorphic buffer layers were engineered to have low dislocation density at the end of the graded region and an atomically smooth surface template over which the active device layer growth was achieved resulting in high performance

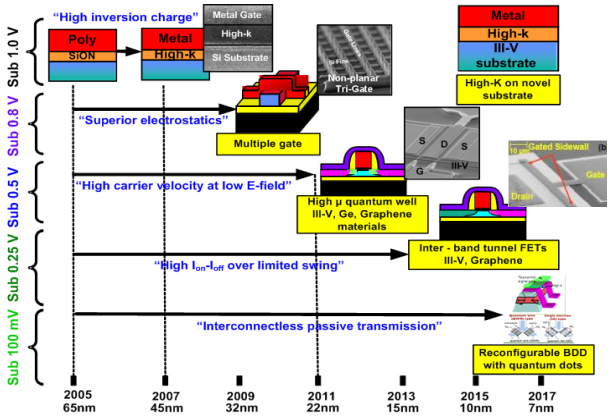

Fig. 1 Device architecture progression to enable scaling of supply voltage of operation

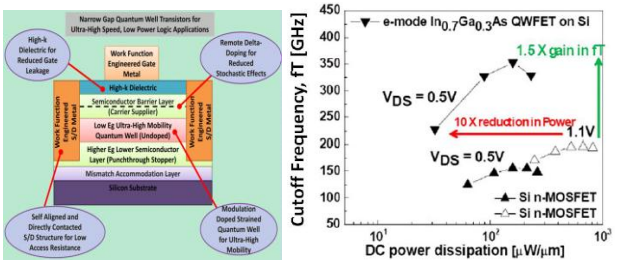

Fig. 2 (a) III-V quantum-well transistor (QWFET) architecture on Silicon (b) Cutoff frequency, Ft, vs DC power consumption of In0.7Ga0.3As n-QWFET (L_G = 80nm) benchmarked against a Si n-MOSFET based RF amplifier (L_G = 65nm)

$In_{0.7}Ga_{0.3}As$ epitaxial QWFETs to be successfully demonstrated on silicon substrate (Fig. 2(b)), thereby proving the feasibility of heterogeneously integrating the InGaAs, InAs or InSb-based QWFETs alongside the Si CMOS transistors in a monolithic fashion. These recent developments are significant in the context of logic transistors operating with high performance at 0.5V supply voltage due to the excellent transport properties of the electrons under low electric field.

Inter-band Tunnel Transistors

For continued Vcc scaling to 0.25V or below, the MOSFET or QWFET architecture may not be suitable due to the non-scalability of the threshold voltage arising from the fundamental kT/q limit of the sub-threshold slope. Thus, we have initiated investigation of III-V based inter-band Tunnel FETs to demonstrate transistors with steep (sub kT/q) switching characteristics (Fig. 3a). In tunnel transistors, a reverse biased tunnel junction that controls the transistor on and off states. This scheme fundamentally eliminates the high-energy tail present in the Fermi–Dirac

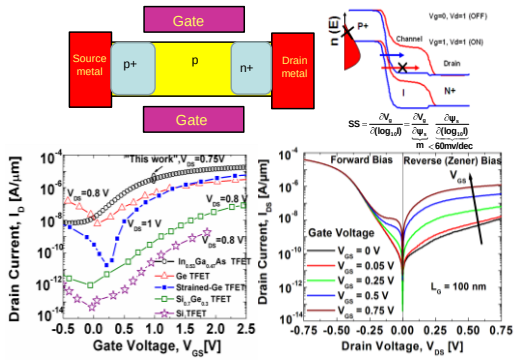

Fig.3 a) Tunnel transistor schematic and energy band diagram b) Transfer and c) output characteristics of an experimental InGaAs tunnel transistor [3]

distribution of the valence band electrons in the p+ source region and allows sub-kT/q subthreshold slope device operation near the OFF state. This allows Tunnel FETs to achieve, in principle, a much higher Ion−Ioff ratio over a specified gate voltage swing compared to MOSFETs, making the former attractive for low-V_{DD} operation. To ensure that the tunnel junctions are highly doped and abrupt and the inter-band tunneling is efficient we employed a vertical tunnel FET architecture to realize high performance tunnel FETs. We have experimentally demonstrated vertical $In_{0.53}Ga_{0.47}As$ tunnel field effect transistors (Fig. 3b) with 100nm channel length and high-k dielectric / metal gate stack are with high Ion/Ioff ratio (>10^4). Here, a conformal gate stack wraps the sidewall of the mesa structure and current conduction occurs along the sidewall in a vertical direction from the source to the drain. At drain bias, V_{DS} = 0.75V, a record on-current of 20μA/μm was achieved due to the higher tunneling rate in narrow tunnel gap $In_{0.53}Ga_{0.47}As$ compared to other conventional semiconductors such as germanium and silicon (Fig. 3b). Two distinct regions of operation are evident from the output characteristics (Fig. 3c) a reverse biased Zener diode and a forward biased Esaki diode as a function of the gate voltage. In the reverse biased direction, the channel region inverts with positive Vg and the band to band tunneling ensues turning on the transistor. When a forward bias is applied across the drain and source, a negative differential resistance region appears in the I-V characteristics. This is a direct evidence of direct quantum mechanical tunneling between the drain and channel. This intrinsic gate controlled NDR behavior is a unique feature of tunnel FETs which provides opportunity for us to implement embedded SRAM memory elements out of tunnel FETs with fewer device count.

Tunnel-coupled Nanodots

Reducing supply voltage of operation to 100mV or below eventually affects the voltage transfer gain in CMOS logic. Further, reduced device transconductance at very low supply voltage together with higher percentage of

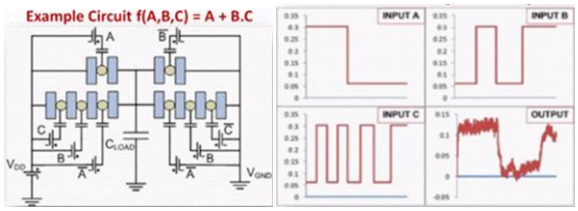

Fig.4 A BDD representation of an arbitrary logic function: f(A,B,C) = A + B.C using tunnel based coupled SETs along with Monte Carlo simulation of an example circuit operating at RT

interconnect and contact resistance effects become an impediment to effectively exploit the benefits of traditional CMOS device scaling. To circumvent the interconnect related issues, we are exploring a novel binary decision diagram based logic architecture where computation proceeds via passive transmission of carriers through a network of tunnel coupled nanodots [5]. At each decision node, transmission through left or right branches is determined by the Coulomb potential of the nanodot. Further, this logic architecture produces a) lower device count than conventional Boolean CMOS logic, b) reduces wiring related energy loss, and c) maintains logic functionality under millivolt of supply voltage, thereby operating with a record low power-delay product (Fig. 4).

Conclusions

In summary, it is believed that, in the future, a multitude of non-silicon logic elements needs to be integrated with the conventional Si CMOS transistor technology to continue aggressive supply voltage scaling and significantly reduce energy consumption.

References: [1]S. Datta *et al*, IEDM Tech. Digest, pp 763 (2005); [2]T. Ashley, S. Datta *et al*, Electr. Lett. (2007); [3]S. Datta *et al*, IEEE Electr. Dev. Lett. pp 685 (2007); [4]S. Mookerjea, S. Datta, *et al*, IEDM Tech. Digest (2009); [5]V. Saripalli, S. Datta *et al*, IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 333 (2008)