International Journal of High Speed Electronics and Systems
Vol. XX, No. X (2010) 1–7

World Scientific
www.worldscientific.com

COMPOUND SEMICONDUCTOR BASED TUNNEL TRANSISTOR LOGIC

SUMAN DATTA

Department of Electrical Engineering, The Pennsylvania State University, University Park, PA 16802, USA[*]
sdatta@engr.psu.edu

Received (Day Month Year)
Revised (Day Month Year)
Accepted (Day Month Year)

We introduce a new transistor architecture based on inter-band tunneling mechanism as a step towards exploring steep switching transistors for energy efficient logic applications. While there have been reports on tunnel transistors in Si, Ge material system and their alloys, we focus specifically on narrow gap compound semiconductor (CS) systems to develop tunnel transistors. We address the following topics regarding the CS-based tunnel transistor architecture: a) the choice of appropriate materials to tune the transfer characteristics over a specified gate voltage swing b) the characteristic screening lengths in these device essential for scaling, c) an effective way to estimate the switching speed of tunnel transistors, d) digital circuit design methodologies utilizing tunnel transistors.

Keywords: Tunnel FET; InGaAs; logic; SRAM

1. Introduction

Continued miniaturization of the silicon CMOS transistor technology, has resulted in an unprecedented increase in single-core and multi-core performance of modern-day microprocessors. However, the exponentially rising transistor count has also increased the overall power consumption, making performance per watt of energy consumption the key figure-of-merit for today's high-performance microprocessors. Today, energy efficiency serves as the central tenet of high performance microprocessor technology at the system architecture level as well as the transistor level ushering in the era of energy efficient nanoelectronics. Aggressive supply voltage scaling while maintaining the transistor performance is a direct approach towards reducing the energy consumption since it reduces the dynamic power quadratically and the leakage power linearly. To that effect, narrow gap compound semiconductor-based (e.g. indium antimonide, indium arsenide and $In_xGa_{1-x}As$) inter-band tunnel transistor (TFET) architecture could enable the next generation of logic transistors operating below 0.5 V supply voltage. In this invited paper, we present a comprehensive study of the basic TFET architecture, the optimum materials choice to improve TFET performance, the advanced TFET

[*] State completely without abbreviations, the affiliation and mailing address, including country. Typeset in 8 pt Times Italic.

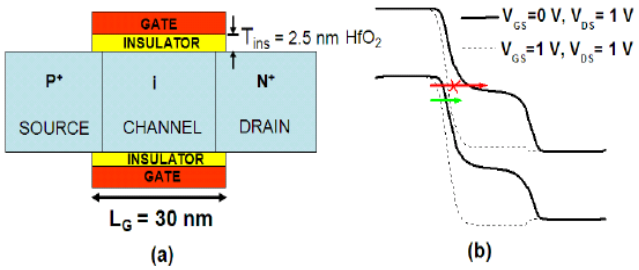


Fig. 1. (a) Schematic of a double gate inter-band tunnel transistor (TFET) architecture; (b) Energy band diagram illustrating the TFET ON and OFF state conditions

architectures, the transient response of the TFETs in a digital circuit configuration, and, finally, embedded memory design strategy with TFET.

2. Inter-band Tunnel Transistor

Inter-band tunnel field effect transistors (TFETs) with a gate modulated zener tunnel junction at the source have recently attracted a great deal of interest, both theoretically and experimentally [1]-[4]. Figure 1 shows a schematic of an n-channel TFET architecture which incorporates a highly doped p+ source region, a near intrinsic channel region and n+ drain region. The n-channel TFET operates on the principle of band to band tunneling of electrons across the source to channel tunnel junction under the influence of a gate electric field. The major advantage of the TFETs in comparison with the metal-oxide-semiconductor field-effect transistors (MOSFETs) is that the reverse biased tunnel junction in the former eliminates the high energy tail present in the Fermi-Dirac distribution of the valence band electrons in the p+ source region and allows sub-kT/q sub-threshold slope device operation over a certain gate bias range near the off-state. This allows TFETs to achieve, in principle, much higher I_{ON}-I_{OFF} ratio over a given gate voltage swing compared to the MOSFETs, making the TFET architecture an attractive vehicle to implement low supply voltage (V_{DD}) digital logic circuits. Figure 2

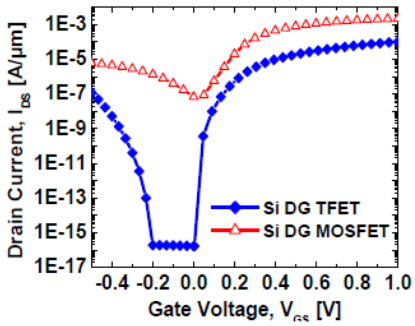


Fig. 2. Transfer characteristics of 30nm gate length double gate silicon TFET and MOSFET at 1V supply voltage [4]

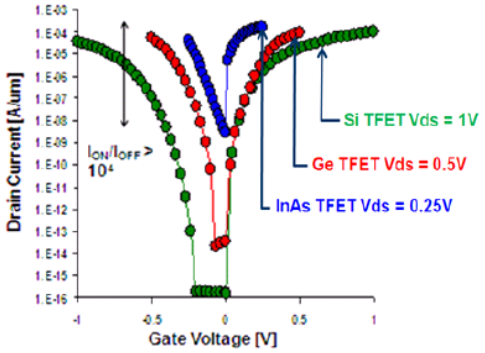


Fig. 3. Transfer characteristics of double gate TFETs in Si, Ge and InAs semiconductors under various supply voltages [4]

shows the transfer characteristics of a silicon (Si) double gate 30 nanometer gate length TFET benchmarked against a Si MOSFET of identical dimensions, both operating under 1V supply voltage. The very low off-state current of the TFET is set by the reverse bias saturation current of the p-i-n diode. Near the off-state, the TFET clearly exhibits < 60mV/decade which results in a vastly superior I_{ON}-I_{OFF} ratio compared to the MOSFETs. However, the on current in a TFET is significantly lower than its MOSFET counterpart being limited by the low transmission rate of electrons across the reverse biased tunnel junction between the source and the channel. It is evident that narrow gap semiconductors such as Ge and InAs can significantly enhance the source side tunneling rate due to the combined effect of reduced barrier height and shorter tunneling distance in addition to the reduced tunneling mass. Figure 3compares the transfer characteristics of Si, Ge and InAs TFETs under various supply voltages. The InAs TFET shows the highest on current (275 µA/µm) at the lowest supply voltage of 0.25V with an I_{ON}/I_{OFF} ratio exceeding $4x10^4$. However, the InAs TFETs also exhibit strong ambipolar characteristics due to the tunneling of carriers from the drain into the channel at negative gate voltages. This warrants the need for other advanced tunnel transistor architecture in addition to introducing the narrow bandgap semiconductors to enhance its overall performance and its energy efficiency. We have recently fabricated a vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET by using a side gated structure. Figure 4 shows the SEM images of fabricated $In_{0.53}Ga_{0.47}As$ vertical TFET featuring gate air-bridge and conformal high-k dielectric and metal gate stack on the sidewall. Figure 5 shows the measured transfer and output characteristics of the 100nm channel length tunnel transistors at room temperature. The minimum current ("leakage floor") at V_{DS} = 50mV is only 40 pA/µm increasing to 6nA/µm at VDS = 0.75V. The corresponding on currents are 0.5µA/µm (linear) and 20µA/µm (saturation). This translates to an I_{ON}/I_{OFF} ratio of ~ 10^4 and $3x10^3$, respectively. Two distinct regions of operation are evident from the output characteristics – a reverse biased zener diode and a forward biased Esaki diode as a function of the gate voltage. Gated negative differential resistance (NDR) behavior in TFET output characteristics during drain-to-source forward bias operation confirm the inter-band tunneling process.

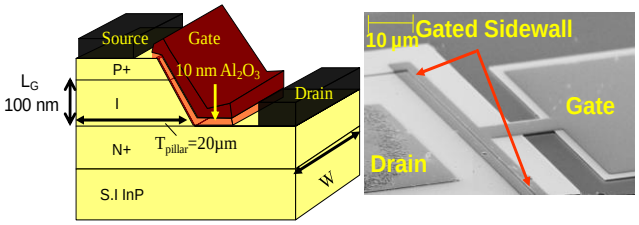


Fig. 4. Schematic and tilted view SEM of a fabricated InGaAs Tunnel FET with gate length of 100 nm. [5]

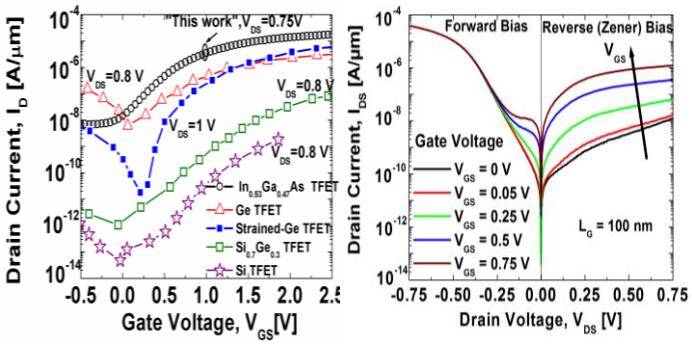


Fig. 5. Experimental transfer (left) and output (right) characteristics of fabricated 100nm Lg InGaAs Tunnel FET (showing gated NDR effect) [5]

3. Heterojunction Tunnel Transistor

Careful benchmarking with the state-of-the art double gated Si NMOS transistors indicate that, the homojunction InGaAs Tunnel FETs of similar dimensions (Tsi, Tox) will still fall short in terms of performance. This is illustrated in Fig. 6, where our fabricated device as well as projected TFET performance is compared with both high V_T and low V_T CMOS transistors. In order to enhance the tunnel transistor performance, we propose two advanced TFET device architectures: (a) δ-TFET with a 2nm thin heavily doped n-type (δ-n+) layer adjoining the source and (b) δ-HTFET with a thin (3nm) layer of narrow band-gap material (p+-InAs) at the tunneling junction (Hetero-junction) with an adjoining δ-N+ layer as used for δ-TFET. For 3nm InAs, quantized band-gap of 0.5eV and conduction band offset of 0.1eV (Type-I) with $In_{0.53}Ga_{0.47}As$ were considered. Fig. 6 shows transfer characteristics (I_D-V_{GS}) for each of them along with same EOT single gate intrinsic channel InGaAs tunnel FET (SG-i-TFET) and Si MOSFETs with low and high threshold voltages (V_T). Clearly, tunnel FETs have significant I_{ON} advantage at lower gate voltages due to their inherent steep slope switching. I_{ON} in i-TFET and SG-i-TFET is lower than high V_T MOSFET, while, δ-TFET and δ-HTFET show higher I_{ON} for the entire gate voltage range. The presence of a depleted δ-N+ layer reduces tunneling width and presence of lower band-gap InAs reduces tunneling barrier. With an additive effect of both, δ-HTFET shows maximum I_{ON} surpassing the CMOS transistors.

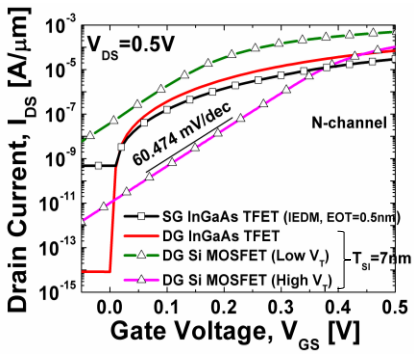
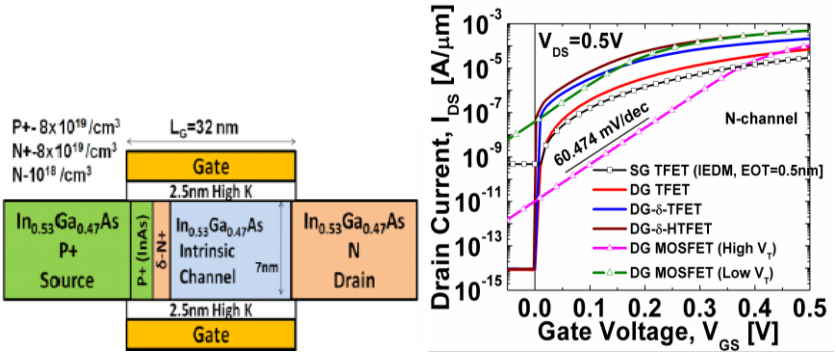


Fig. 6. Transfer characteristics of fabricated and projected homojunction InGaAs TFET benchmarked against high and low Vt CMOS transistors



(a) (b)

Fig. 7. (a) Schematic of an ultra-thin body (UTB), double gate (DG) delta doped heterojunction TFET (δ-HTFET) (b) Simulated transfer characteristics for the three different UTB-DG-TFET structures, SG-i-TFET and Si MOSFETs with high and low VT at V_{DS}=0.5V

4. SRAM Circuit Utilizing Tunnel Transistor

Due to its inherent asymmetric source and drain design and a built in p-i-n diode, bidirectional current conduction is not possible in TFETs. This makes TFET based pass transistor implementation impossible resulting in 6T TFET SRAM with degraded read or write margins (Fig. 8). When the Tunnel FET access transistors face inward, the read margin is excellent and can be tuned by changing the relative strength of the pull down transistor and the access transistor. However, the margin suffers since the inward facing access TFET cannot discharge the storage node while writing a zero. When the Tunnel FET access transistors face outward, the opposite happens i.e. write margin is excellent and can be tuned by varying the relative strengths of the pull-up and access device, but read margin suffers. 7T and 8T TFET SRAM implementations with separate read and write port have been proposed compromising cell size. We implement a novel 6T TFET

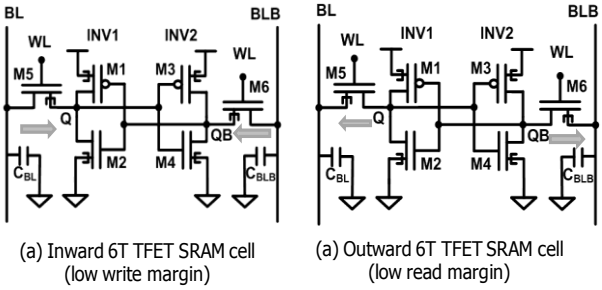


Fig. 8. 6T TFET SRAM cell using TFET pass transistors pointing (a) inward and (b) outward. Inward 6T TFET SRAM has good read margin but poor write margin whereas the outward TFET SRAM exhibits excellent write margin but poor read margin [8].

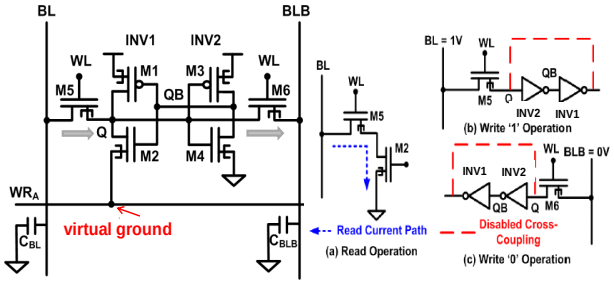


Fig. 9. Novel 6T TFET SRAM is designed where M5 and M6 TFETs are used to write "1" and "0", respectively, at node Q. During write, the cell is weakened by disabling the inverter pair cross-coupling via virtual ground. Read operation is similar to inward 6T TFET SRAM [8]

SRAM where inward M5 and outward M6 TFETs are used to write "1" and "0", respectively, at the same node Q (Fig. 9). During writing, the cell is weakened by disabling the inverter pair cross-coupling via virtual ground. Excellent read and write noise margins are achieved in this novel 6T TFET SRAM configuration.

5. Conclusions

We have demonstrated 100nm L_G vertical homojunction $In_{0.53}Ga_{0.47}As$ TFET with 10^4 I_{ON}-I_{OFF} ratio and 20μA/um on current. This is the highest performance Tunnel FET demonstrated till date in any material system. We have also designed more advanced TFET transistor incorporating heterojunction tunnel source architecture to boost on-current. Further, we have shown how to design a 6T SRAM cell using asymmetric source-drain TFET with excellent noise margin down to 0.3V supply voltage. We believe that compound semiconductor based inter-band tunneling FET is promising device architecture for future ultra low power digital logic applications

6. Acknowledgments

The author gratefully acknowledges the support of the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND) and Intel.

References

1. W. M. Reddick and G.A.J. Amaratunga, Silicon surface tunnel transistor Applied Physics Letters, vol 67, pp. 494 (1995)
2. K. K. Bhuwalka, S. Sedlmaier, A. K. Ludsteck, C. Toksdorf, J. Schulze and I. Eisele, Vertical tunnel field-effect transistor, IEEE Transactions on Electron Devices, vol. 51, pp. 279 (2004)
3. P. F. Wang, Complementary tunneling fets (ctfet) in cmos technology, Ph.D. dissertation, TU Munchen, Munich, Germany, May (2003)
4. Ph.D. dissertation, TU Munchen, Munich, Germany, May 2003 S. Mookerjea and S. Datta, Comparative Study of Si, Ge and InAs Based Steep Subthreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications, Proc. 66th Dev. Res. Conference Digest, pp. 47 (2008)
5. S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu and S. Datta, Experimental Demonstration of 100nm Channel Length $In_{0.53}Ga_{0.47}As$-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications Technical Digest of International Electron Devices Meeting (IEDM), December, 2009
6. S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, S. Datta, Temperature-Dependent Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET, IEEE Electron Device Letters, vol. 31, no. 6, pp. ,June Oct (2009)
7. S. Mookerjea, R. Krishnan, S. Datta and V. Narayanan, Effective Capacitance and Drive Current for Tunnel-FET (TFET) CV/I Estimation, IEEE Transactions on Electron Devices, vol. 56, no. 9, pp. 2092-2098, September (2009)
8. J. Singh, R. Krishnan, S. Mookerjea, S. Datta, V. Narayanan, A Novel Si TFET Based SRAM design for Ultra Low-Power 0.3V V_{DD} Applications, 15th Asia Pacific Design Automation Conference, ASP-DAC (2010)