Scalability Study of In$_{0.7}$Ga$_{0.3}$As HEMTs for 22nm node and beyond Logic Applications

E. Hwang$^1$, S. Mookerjea$^1$, M. K. Hudait$^2$ and S. Datta$^1$

$^1$The Pennsylvania State University, PA 16802,  $^2$Virginia Tech University, VA 24061, USA
Phone: (814) 865 0519, Fax: (814) 865 7065, E-mail: euh125@psu.edu

Compound semiconductor high electron mobility transistors (HEMTs) have recently gained a lot of interest for future high-speed, low-power logic applications due to their high mobility and high effective carrier velocity [1]. Conventional In$_{0.7}$Ga$_{0.3}$As HEMTs with 50 to 150nm gate-length ($L_G$) have been experimentally demonstrated [2] with excellent device performance. In this paper, (i) we use two-dimensional numerical drift-diffusion simulations [3] to model the conventional In$_{0.7}$Ga$_{0.3}$As HEMTs with different $L_G$ from 15 to 200nm and investigate its scalability for future logic applications. (ii) An accurate estimation of effective mobility ($\mu_{eff}$) and effective carrier velocity (injection) is presented, highlighting the relevance of ballistic mobility in these short-channel HEMTs. (iii) Due to degradation in performance of the conventional scaled In$_{0.7}$Ga$_{0.3}$As HEMT at $L_G$=15nm, three novel HEMT device architectures are studied and the design for the ultimate scaled transistor is proposed.

Fig. 1 shows the simulated In$_{0.7}$Ga$_{0.3}$As HEMT device structure with a composite channel consisting of 3/8/4nm of In$_{0.53}$Ga$_{0.47}$As/In$_{0.7}$Ga$_{0.3}$As/In$_{0.53}$Ga$_{0.47}$As and buried Pt gate electrode on In$_{0.52}$Al$_{0.48}$As barrier layer. Fig. 2 compares the transfer characteristics of the simulated and the experimental [2] 50nm composite In$_{0.7}$Ga$_{0.3}$As HEMTs. The simulated characteristics agree very well with the experimental data and thus the model parameters are calibrated. In simulation we use the Canali mobility model with $\mu_{lowfield}$=12,000 and 10,000cm$^2$/Vs for In$_{0.53}$Ga$_{0.47}$As and In$_{0.7}$Ga$_{0.3}$As, respectively, and $\alpha$=0, $\beta$=1. To analyze the scaling behaviour, $L_G$ in Fig. 1 is varied from 15 to 200nm and subthreshold-slope (SS), drain-induced barrier lowering (DIBL), threshold voltage ($V_T$) roll-off, $I_{ON}$/I$_{OFF}$ ratio and gate-delay (CV/I) are compared to the experimental data in Fig. 3 and Fig. 4. In addition to $L_G$ scaling, side-spacing ($L_{SIDE}$) is also decreased from 80 to 15nm and its impacts on the device performance are shown in table 1. One can find that the lateral scaling causes the overall electrostatic integrity to deteriorate due to severe short-channel effects (SCE). In order to ensure $L_G$ scaling down to 15nm and beyond, the vertical scaling of the conventional In$_{0.7}$Ga$_{0.3}$As HEMT is, therefore, the only remaining option. The insulator thickness, $T_{INS}$ and channel thickness, $T_{CH}$ are reduced from 7 to 4nm and 15 to 7nm, respectively and the simulation results are shown in table I. Vertical scaling results in better gate control and, thereby, SS, DIBL, $I_{ON}$/I$_{OFF}$ ratio are significantly improved. Further, the effect of increasing the buffer layer doping ($N_A$) from 1x10$^{17}$ to 5x10$^{17}$ cm$^{-3}$ is investigated and table 1 shows that as $N_A$ is increased, SCE improves, but $I_{ON}$/I$_{OFF}$ ratio degrades due to pinch-off of the access region.

As the device scales down, the short-channel HEMTs are believed to be operating in the ballistic regime [4] and this ballistic effect causes $\mu_{eff}$ to decrease significantly compared to long-channel HEMTs (Fig. 5). To investigate the effect of this ballistic mobility in our simulation, $\mu_{eff}$ for 50, 100 and 150nm $L_G$ In$_{0.7}$Ga$_{0.3}$As HEMTs are extracted from the $I_D$-$V_G$ at low-drain bias [5] as shown in Fig. 6 (a). $\mu_{eff}$ is extracted from equation in Fig. 6 (a) which is fitted to our simulation data. In this equation, $C_{eq}$ is a combination of barrier capacitance and centroid capacitance and, $\theta$ and $\beta$ are the fitting parameters to reflect the dependence of gate electric field on the channel transport. From Fig. 6 (a), it is clear that $\mu_{eff}$ reduces as $L_G$ is decreased. The extracted short channel mobility is compared with the calculated mobility ($\mu_{ballistic}=2qL/\pi\mu_{bulk}$) in Fig. 6 (b) which directly arises from the transmission factor being the ratio of the mean free path to the physical $L_G$. This indicates that the mobility reduction in short-channel HEMTs is directly related to the ballistic effect. Fig. 7 plots the effective carrier velocity vs DIBL for 15 to 200nm $L_G$ In$_{0.7}$Ga$_{0.3}$As HEMTs. This shows that the effective carrier velocity increases as the electrostatic integrity worsens. Compared to the strained Si n-MOSFETs, In$_{0.7}$Ga$_{0.3}$As HEMTs show ~4-5 times higher effective carrier velocity. Thus, in spite of the mobility reduction with $L_G$, In$_{0.7}$Ga$_{0.3}$As HEMTs still look very promising because we can achieve higher effective carrier velocity near the source end due to its lower conductivity effective mass and higher ballistic injection efficiency. To achieve higher drive current, ~4-5 X higher effective velocity in In$_{0.7}$Ga$_{0.3}$As HEMT is a necessity because it is expected to have ~2-3 X lower channel charge compared to Si MOSFETs at comparable operating bias [6].

Finally, based on the scaling behavior analysis of In$_{0.7}$Ga$_{0.3}$As HEMTs (Fig. 3, Fig. 4 and Table 1), we study 3 novel device architectures for future logic applications. Device structures for Double-Gate HEMT (DG-HEMT), Inverted HEMT (i-HEMT) and HEMT with twin-delta doping layer (HEMT with TDD) and higher buffer layer doping are shown in Fig. 8. Twin delta doping is incorporated to mitigate the access resistance problem. Their performance (SS, DIBL, $V_T$, $I_{ON}$/I$_{OFF}$ ratio, CV/I, $V_{th}$) are compared to non-planar Si n-MOSFETs in Fig. 9. In this case, $L_G$ and $L_{SIDE}$ are aggressively scaled down to 15nm. Fig. 9 shows that Double-Gate In$_{0.7}$Ga$_{0.3}$As HEMT has the best performance in terms of SCE, thus making it a strong candidate for the design of the ultimate scaled transistor.

In0.53Ga0.47As Cap

6nm InP Stopper

Source

Drain

6nm InP Stopper

8nm In0.53Al0.48As Barrier layer

3nm In0.52Al0.48As Spacer layer

3nm In0.52Al0.48As Channel layer

4nm In0.52Al0.48As Barrier layer

500nm In0.52Al0.48As Buffer layer

Fig. 1 Simulated device structure [2]

---

Table 1. Performance improvement with vertical scaling

<table>
<thead>
<tr>
<th>L_G [nm]</th>
<th>TCH=15nm</th>
<th>TCH=7nm</th>
<th>TCH=4nm</th>
<th>TCH=7nm</th>
<th>TCH=4nm</th>
<th>TCH=7nm</th>
<th>TCH=4nm</th>
<th>TCH=7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIBL [mV/V]</td>
<td>339.9</td>
<td>468.9</td>
<td>255.5</td>
<td>146.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SS [mV/dec]</td>
<td>114.8</td>
<td>134.9</td>
<td>102.4</td>
<td>97.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_t sat [V]</td>
<td>-0.54</td>
<td>-0.67</td>
<td>-0.27</td>
<td>0.05</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{ON}/I_{OFF}</td>
<td>2.42x10^3</td>
<td>1.91x10^3</td>
<td>5.70x10^2</td>
<td>2.92x10^3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>\mu_{ballistic} [cm^2/Vs]</td>
<td>9.57x10^5</td>
<td>8.50x10^5</td>
<td>1.36x10^5</td>
<td>6.28x10^5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

Fig. 2 Calibration of I_{D}-V_{G} of In_{0.53}Ga_{0.47}As HEMT for device in Fig.1

---

Fig. 3 FOM comparison for device in Fig.1

---

Fig. 4 CV/I vs L_G for device in Fig.1

---

\[ I_D = \frac{W}{L_{eff}} \rho_{eff} (V_G - V_F) \left( 1 + \left( \frac{\rho_{eff}}{\rho_{bulk}} \right)^2 \right) \frac{V_D}{V} \]

---

Fig. 5 \( \mu_{ballistic} = \frac{2qL}{n m} \)

---

Fig. 6 (b) \( \mu_{eff} \) vs L_G

---

Fig. 7 \( V_{t sat} \) vs DIBL

---

Fig. 8 (b) Schematic of Inverted (i) In_{0.7}Ga_{0.3}As HEMT

---

Fig. 8 (c) Schematic of In_{0.7}Ga_{0.3}As HEMT with TDD

---

Fig. 9 Device performance for 3 new design schemes of In_{0.7}Ga_{0.3}As HEMT