Scalability Study of $In_{0.7}Ga_{0.3}As$ HEMTs for 22nm node and beyond Logic Applications

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Compound semiconductor high electron mobility transistors (HEMTs) have recently gained a lot of interest for future high-speed, low-power logic applications due to their high mobility and high effective carrier velocity [1]. Conventional $In_{0.7}Ga_{0.3}As$ HEMTs with 50 to 150nm gate-length (L_G) have been experimentally demonstrated [2] with excellent device performance. In this paper, (i) we use two-dimensional numerical drift-diffusion simulations [3] to model the conventional $In_{0.7}Ga_{0.3}As$ HEMTs with different L_G from 15 to 200nm and investigate its scalability for future logic applications. (ii) An accurate estimation of effective mobility (μ_{eff}) and effective carrier velocity (injection) is presented, highlighting the relevance of ballistic mobility in these short-channel HEMTs. (iii) Due to degradation in performance of the conventional scaled $In_{0.7}Ga_{0.3}As$ HEMT at L_G=15nm, three novel HEMT device architectures are studied and the design for the ultimate scaled transistor is proposed.

Fig. 1 shows the simulated $In_{0.7}Ga_{0.3}As$ HEMT device structure with a composite channel consisting of 3/8/4nm of $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ and buried Pt gate electrode on $In_{0.52}Al_{0.48}As$ barrier layer. Fig. 2 compares the transfer characteristics of the simulated and the experimental [2] 50nm composite $In_{0.7}Ga_{0.3}As$ HEMTs. The simulated characteristics agree very well with the experimental data and thus the model parameters are calibrated. In simulation we use the Canali mobility model with $\mu_{lowfield}$=12,000 and 10,000cm^2/Vs for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$, respectively, and α=0, β=1. To analyze the scaling behaviour, L_G in Fig. 1 is varied from 15 to 200nm and subthreshold-slope (SS), drain-induced barrier lowering (DIBL), threshold voltage (V_t) roll-off, I_{ON}/I_{OFF} ratio and gate-delay (CV/I) are compared to the experimental data in Fig. 3 and Fig. 4. In addition to L_G scaling, side-spacing (L_{SIDE}) is also decreased from 80 to 15nm and its impacts on the device performance are shown in table 1. One can find that the lateral scaling causes the overall electrostatic integrity to deteriorate due to severe short-channel effects (SCE). In order to ensure L_G scaling down to 15nm and beyond, the vertical scaling of the conventional $In_{0.7}Ga_{0.3}As$ HEMT is, therefore, the only remaining option. The insulator thickness, T_{INS} and channel thickness, T_{CH} are reduced from 7 to 4nm and 15 to 7nm, respectively and the simulation results are shown in table I. Vertical scaling results in better gate control and, thereby, SS, DIBL, I_{ON}/I_{OFF} ratio are significantly improved. Further, the effect of increasing the buffer layer doping (N_A) from $1x10^{17}$ to $5x10^{17}$ cm^{-3} is investigated and table I shows that as N_A is increased, SCE improves, but I_{ON}/I_{OFF} ratio degrades due to pinch-off of the access region.

As the device scales down, the short-channel HEMTs are believed to be operating in the ballistic regime [4] and this ballistic effect causes μ_{eff} to decrease significantly compared to long-channel HEMTs (Fig. 5). To investigate the effect of this ballistic mobility in our simulation, μ_{eff} for 50, 100 and 150nm L_G $In_{0.7}Ga_{0.3}As$ HEMTs are extracted from the I_D-V_G at low-drain bias [5] as shown in Fig. 6 (a). μ_{eff} is extracted from equation in Fig. 6 (a) which is fitted to our simulation data. In this equation, C_{gg} is a combination of barrier capacitance and centroid capacitance and, θ and β are the fitting parameters to reflect the dependence of gate electric field on the channel transport. From Fig. 6 (a), it is clear that μ_{eff} reduces as L_G is decreased. The extracted short channel mobility is compared with the calculated mobility ($1/\mu_{eff} = 1/\mu_{ballistic}+1/\mu_{bulk}$, $\mu_{ballistic}=2qL/\pi m v_{th}$) in Fig. 6 (b) which directly arises from the transmission factor being the ratio of the mean free path to the physical L_G. This indicates that the mobility reduction in short-channel HEMTs is directly related to the ballistic effect. Fig. 7 plots the effective carrier velocity vs DIBL for 15 to 200nm L_G $In_{0.7}Ga_{0.3}As$ HEMTs. This shows that the effective carrier velocity increases as the electrostatic integrity worsens. Compared to the strained Si n-MOSFETs, $In_{0.7}Ga_{0.3}As$ HEMTs show ~ 4-5 times higher effective carrier velocity. Thus, in spite of the mobility reduction with L_G, $In_{0.7}Ga_{0.3}As$ HEMTs still look very promising because we can achieve higher effective carrier velocity near the source end due to its lower conductivity effective mass and higher ballistic injection efficiency. To achieve higher drive current, ~4-5 X higher effective velocity in $In_{0.7}Ga_{0.3}As$ HEMT is a necessity because it is expected to have ~2-3 X lower channel charge compared to Si MOSFETs at comparable operating bias [6].

Finally, based on the scaling behavior analysis of $In_{0.7}Ga_{0.3}As$ HEMTs (Fig. 3, Fig. 4 and Table 1), we study 3 novel device architectures for future logic applications. Device structures for Double-Gate HEMT (DG-HEMT), Inverted HEMT (i-HEMT) and HEMT with twin-delta doping layer (HEMT with TDD) and higher buffer layer doping are shown in Fig. 8. Twin delta doping is incorporated to mitigate the access resistance problem. Their performance (SS, DIBL, V_t, I_{ON}/I_{OFF} ratio, CV/I, v_{eff}) are compared to non-planar Si n-MOSFETs in Fig. 9. In this case, L_G and L_{SIDE} are aggressively scaled down to 15nm. Fig. 9 shows that Double-Gate $In_{0.7}Ga_{0.3}As$ HEMT has the best performance in terms of SCE, thus making it a strong candidate for the design of the ultimate scaled transistor.

[1] R. Chau et al., *IEEE Trans. Nanotechnol.,* vol 4, pp. 153-158 (2005) [2] D.H. Kim et al., *IEEE Trans. Elec. Dev.,* vol 54, pp. 2606-2613 (2007) [3] Sentaurus Version Z-2007.03 [4] M.S. Shur *IEEE Elect. Dev. Lett.,* vol. 23, no. 9, pp. 511-513 (2002) [5] K. Huet et al., *Proc.ESSDERC Conf.,* pp. 382-385 (2007) [6] G. Dewey *IEEE Elect. Dev. Lett,.* vol. 29, no. 10, pp. 1094-1097 (2008)

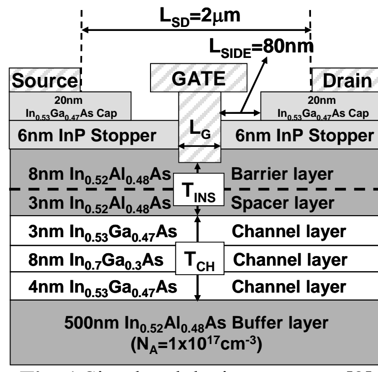


Fig. 1 Simulated device structure [2]

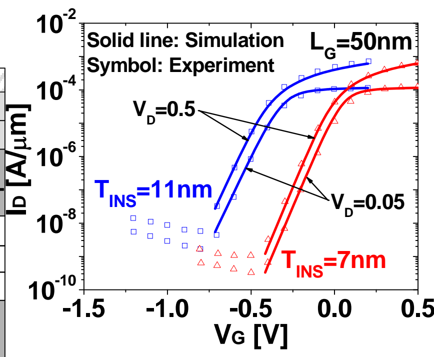


Fig. 2 Calibration of I_D-V_G of $In_{0.7}Ga_{0.3}As$ HEMT for device in Fig.1

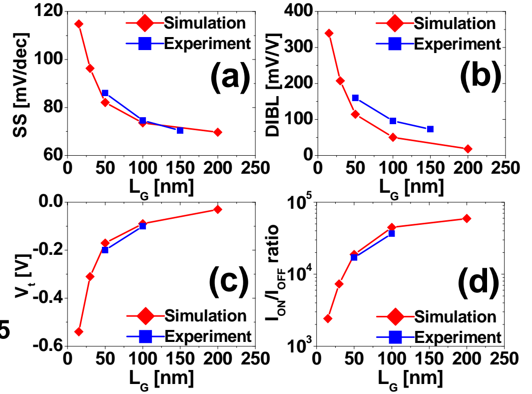


Fig. 3 FOM comparison for device in Fig. 1

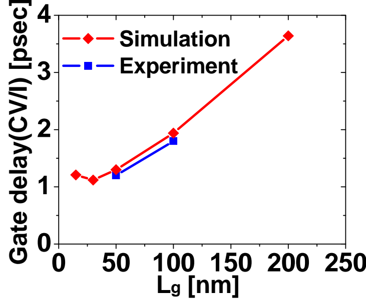


Fig. 4 CV/I vs L_G for device in Fig.1

Table 1. Performance improvement with vertical scaling

L_G=15nm (V_{CC}=0.5)	T_{INS}=7nm T_{CH}=15nm L_{SIDE}=80nm N_a=1X10^{17}cm^{-3}	T_{INS}=7nm T_{CH}=15nm L_{SIDE}=15nm N_a=1X10^{17}cm^{-3}	T_{INS}=4nm T_{CH}=7nm L_{SIDE}=15nm N_a=1X10^{17}cm^{-3}	T_{INS}=4nm T_{CH}=7nm L_{SIDE}=15nm N_a=5X10^{17}cm^{-3}
DIBL [mV/V]	339.9	468.9	253.5	146.4
SS [mV/dec]	114.8	134.9	102.4	97.9
$V_{t.sat}$ [V]	-0.54	-0.67	-0.27	0.05
I_{ON}/I_{OFF}	2.42x10^3	1.01x10^3	5.70x10^3	2.92x10^3
I_{ON}	9.57x10^{-5}	6.55x10^{-5}	1.36x10^{-4}	6.28x10^{-5}

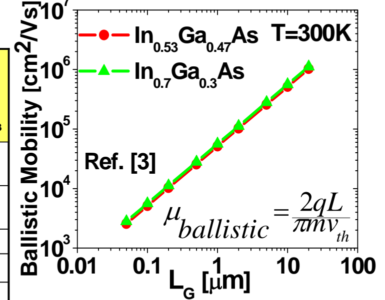
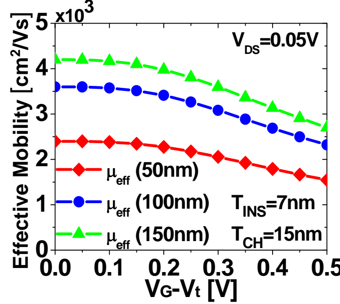


Fig. 5 μ_{ball} vs L_G



$$I_D = C_{gg} \frac{W}{L_{eff}} (V_G - V_t) \frac{\mu_{low}}{(1 + (\theta(V_G - Vt))^{\beta})^{1/\beta}} V_D$$

Fig. 6(a) μ_{eff} vs (V_G-Vt)

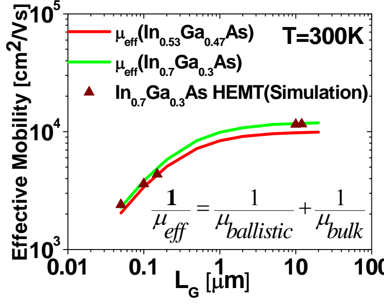


Fig. 6 (b) μ_{eff} vs L_G

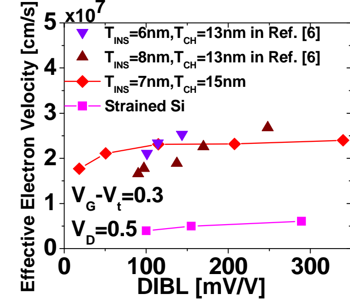


Fig. 7 v_{eff} vs DIBL

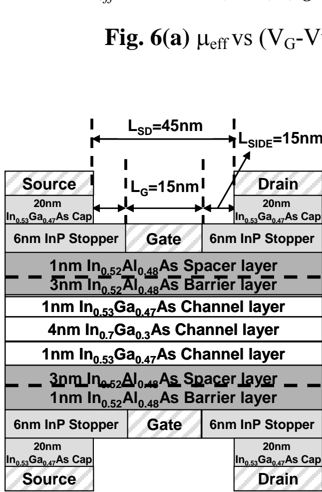


Fig. 8 (a) Schematic of Double-Gate (DG) $In_{0.7}Ga_{0.3}As$ HEMT

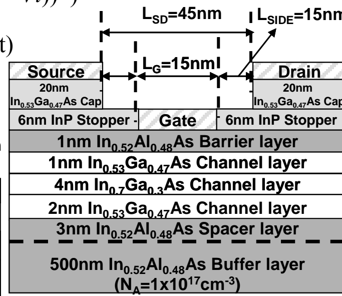


Fig. 8 (b) Schematic of Inverted (i) $In_{0.7}Ga_{0.3}As$ HEMT

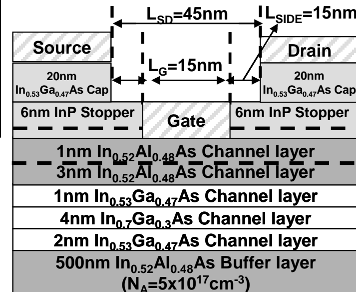


Fig. 8 (c) Schematic of $In_{0.7}Ga_{0.3}As$ HEMT with TDD

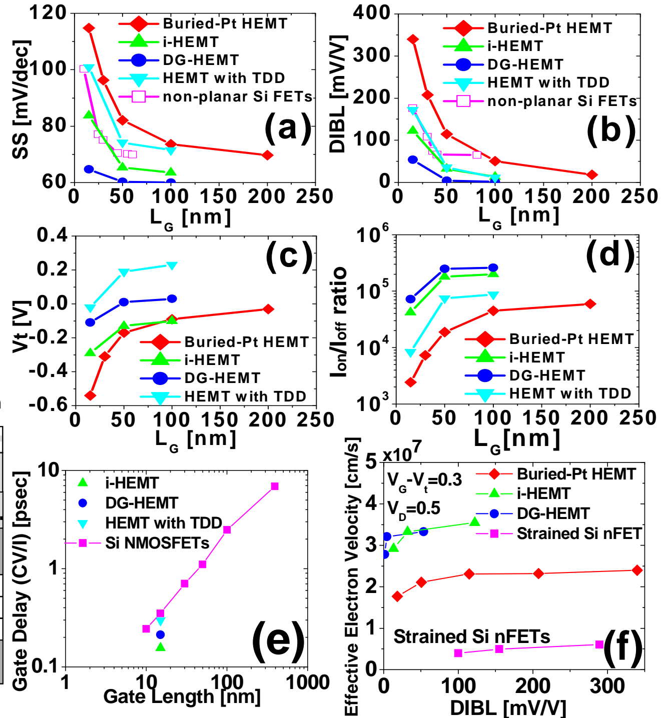


Fig. 9 Device performance for 3 new design schemes of $In_{0.7}Ga_{0.3}As$ HEMT